EK79202B

Rev. 1.1

PRELIMINARY DATA SHEET

2052CH Source Driver with TCON LVDS Interface

fitipower integrated technology Inc.

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Single Chip 2052 Channel Source Driver With Timing Controller for TFT LCD

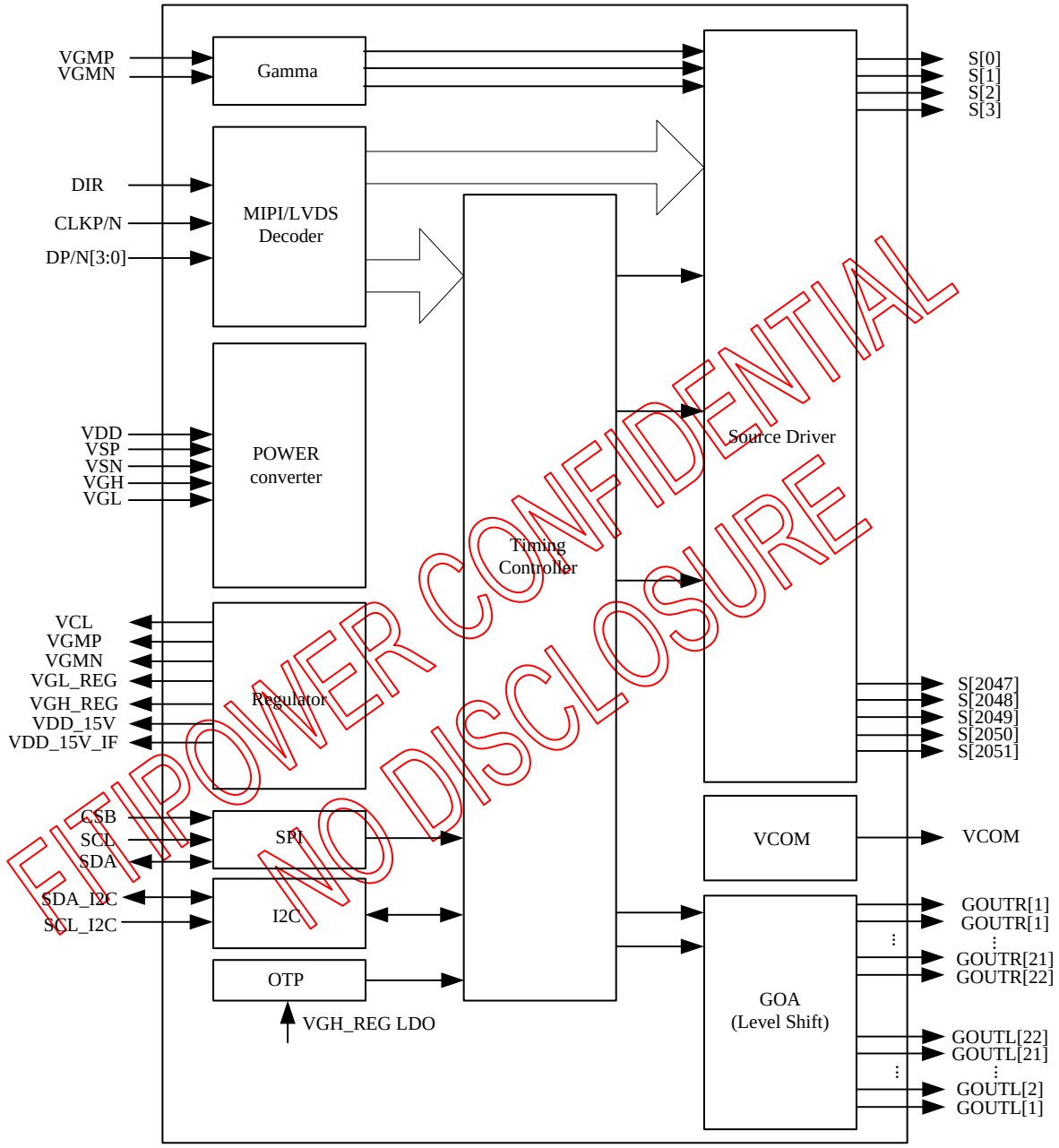
1.General Description

The EK79202 is a highly integrated solution for small size to middle size α-Si TFT-LCD panels. This chip integrates 2052 channel source driver a timing controller for color TFT LCD panel. The chip support LVDS interface. And support the function setting through R/W SPI/3-wie serial interface

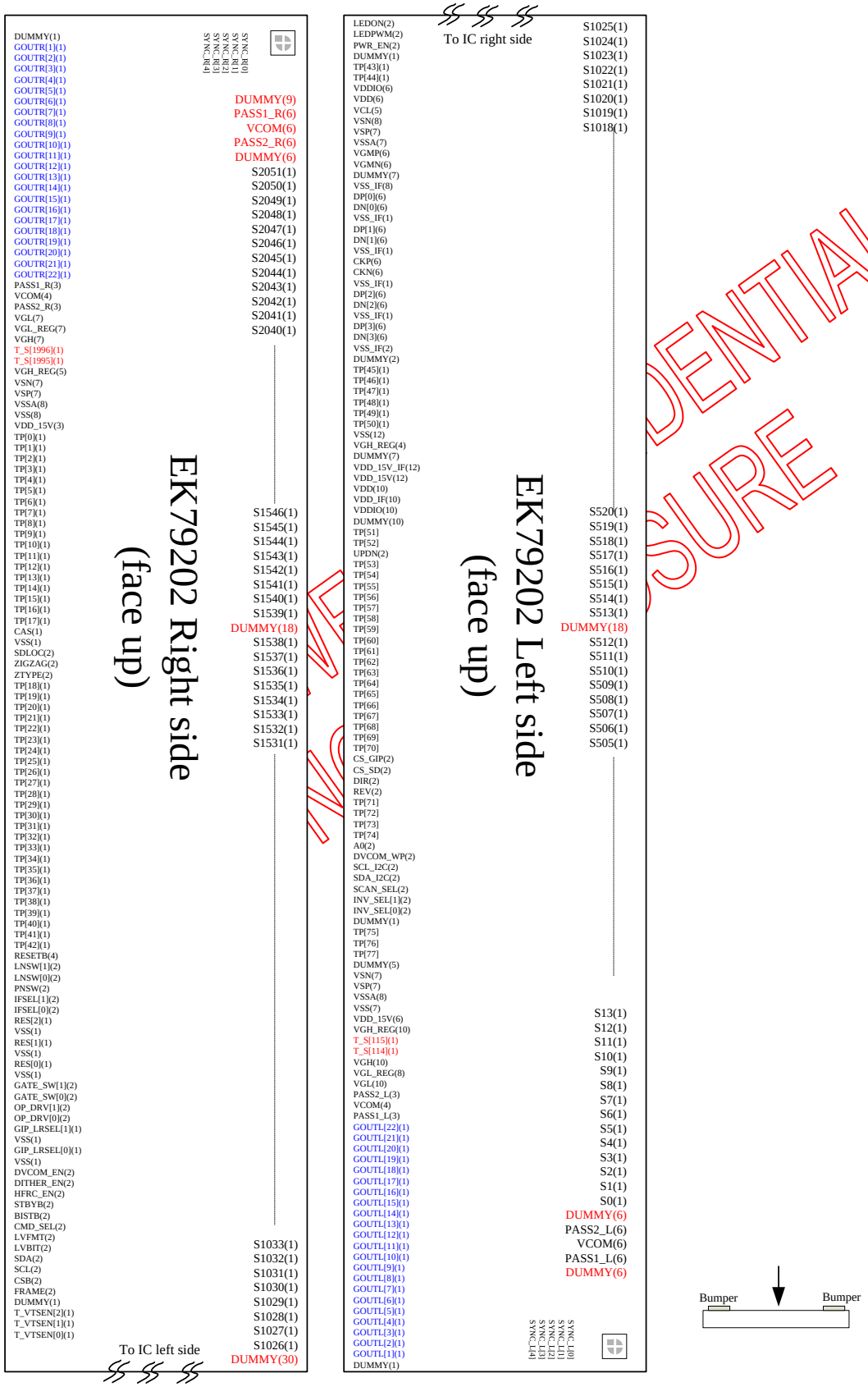
2. Features

- Single chip solution for a WXGA a-Si type LCD display
- Integrate 2052 channel source driver and timing controller
- Display Resolution :
  - 1366 RGB x 768
  - 1280 RGB x 800
  - 1280 RGB x 720
  - 1024 RGB x 600
  - 960 RGB x 640
  - 800 RGB x 600
- System Interfaces:
  - LVDS interface (6/8 bit)
- Integrate 2052 channel source driver and timing controller
- Support for Programming Gamma correction
- OTP memory to store initialization register settings
- Support SPI/I2C interface
- Supports Zigzag /Column inversion
- Gate driver control signals for GIP
- Internal level shifter for Gate driver control
- Built-In VCOM generator
- Built-In Enhanced BIST pattern
- Built-In OTP (6Times) to store VCOM calibration
- Built-In OTP (3Times) to store gamma calibration
- COG package
- Input voltage ranges:
  - I/O and interface power supply (VDDIO): 2.3V to 3.6V
  - High speed interface power supply (VDD_IF): 2.3V to 3.6V
  - Power for digital circuit(VDD): 2.3V~3.6V
  - OTP programming voltage (VOTP): 8.25V+/- 0.25V
  - Analog voltage range for VSP: 4.5V to 6.0V
  - Analog voltage range for VSN: -4.5V to -6.0V
  - Analog voltage range for VGH: 11V to 24V
  - Analog voltage range for VGL: -6V to -17V
  - VGH,VGL: VGH-(VGL)<32V
- Output voltage ranges:
  - Analog voltage range for VCL : VSN+2.4V
  - Positive source output voltage level: VGMP= 3.5V to 5.8V
  - Negative source output voltage level: VGMN= -3.5V to -5.8V
  - Positive gate driver output voltage level: VGH_REG= 5.5V
  - Negative gate driver output voltage level: VGL_REG= -4.5V to -15V
  - VCOM= -0.5V to -2.405V , step=15mV (7-bit resolution)

3. Chip Function Block Diagram



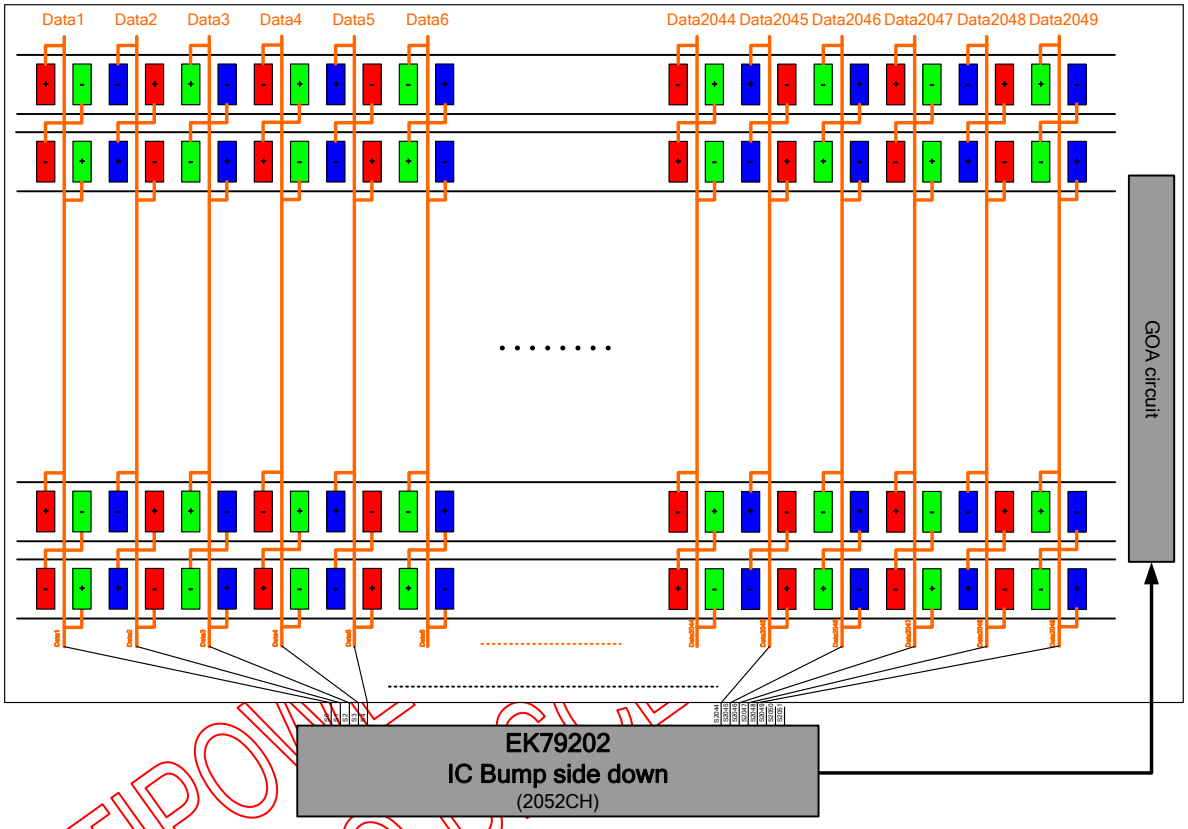
4. Pad Arrangement



5. Application Diagram with Panel

5.1 GIP Application_1366RGBx768 (Normal Dual Gate Driving)

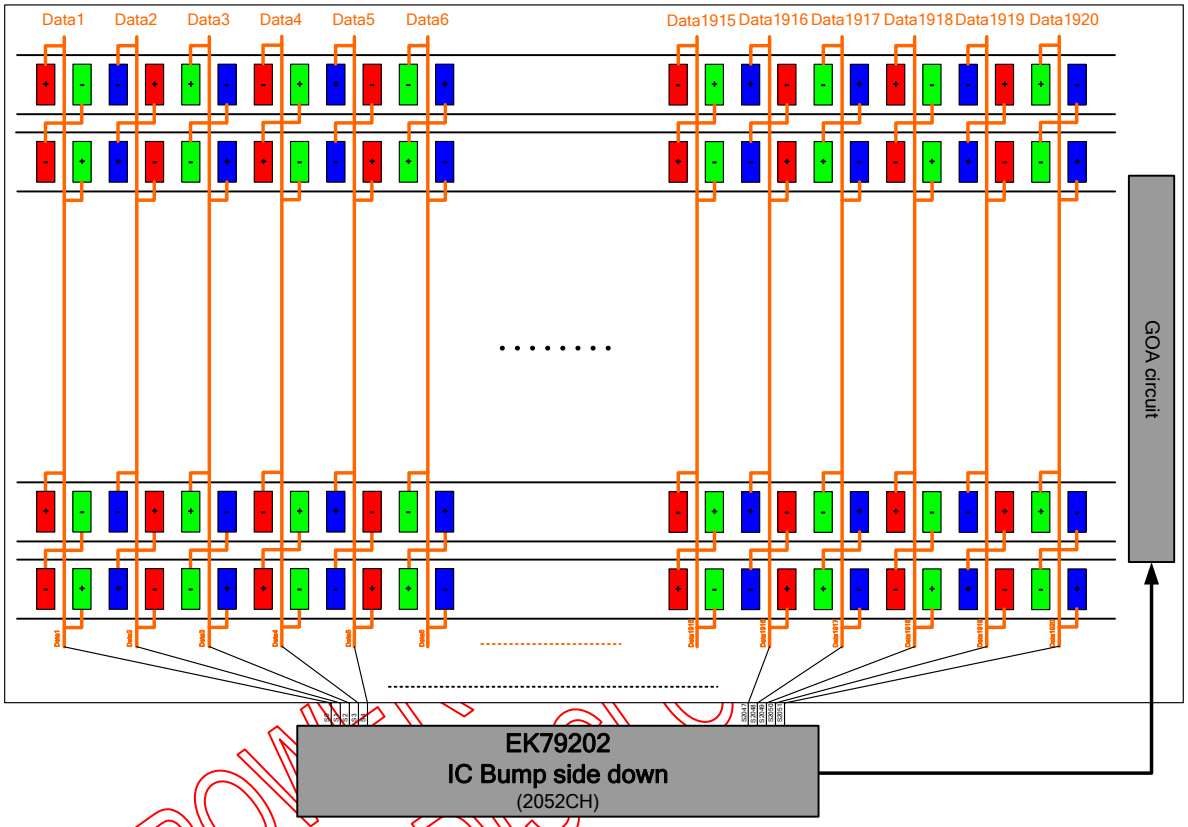
Driving method : Cascade=0



Resolution	Source channel	Disable channel
1366RGBx768	S[2051:0]	-

5.2 GIP Application_1280RGBx800 (Normal Dual Gate Driving)

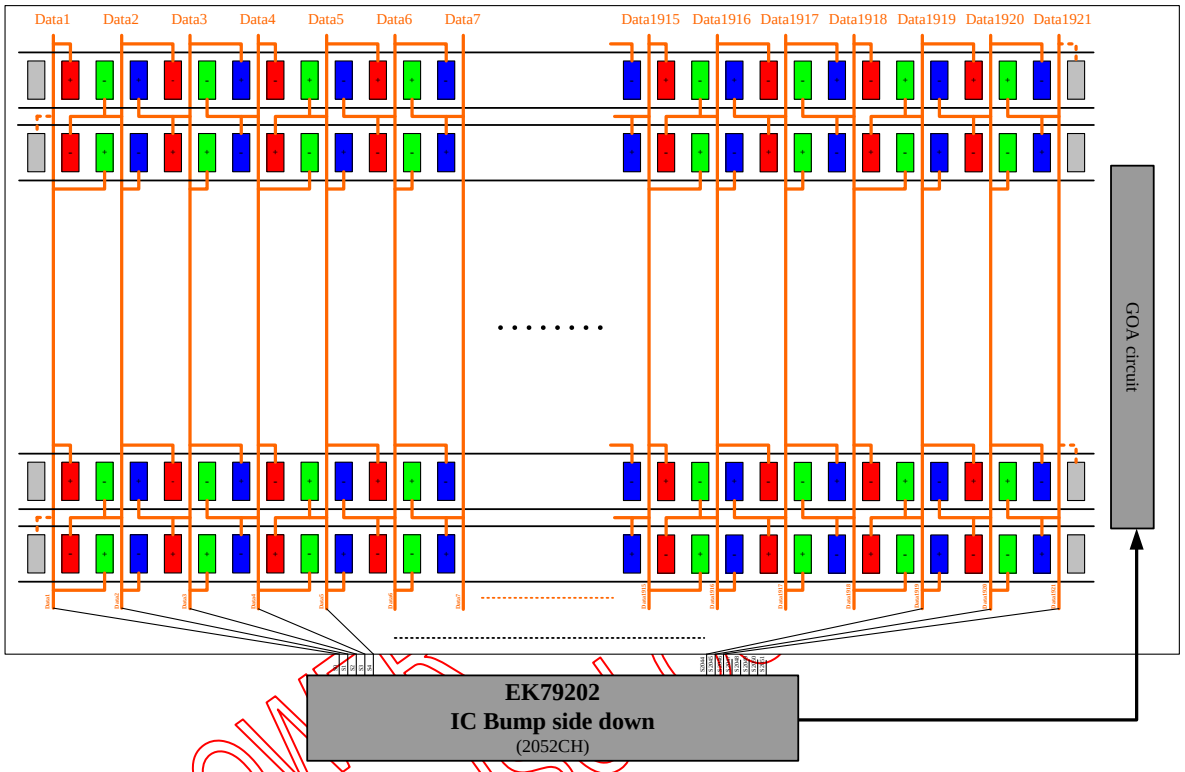
Driving method : Cascade=0



Resolution	Source channel	Disable channel
1280RGBx800	S[959:0] and S[2051:1092]	S[1091:960]

5.3 GIP Application_1280RGBx800 ((Dual Gate+Zigzag Driving)

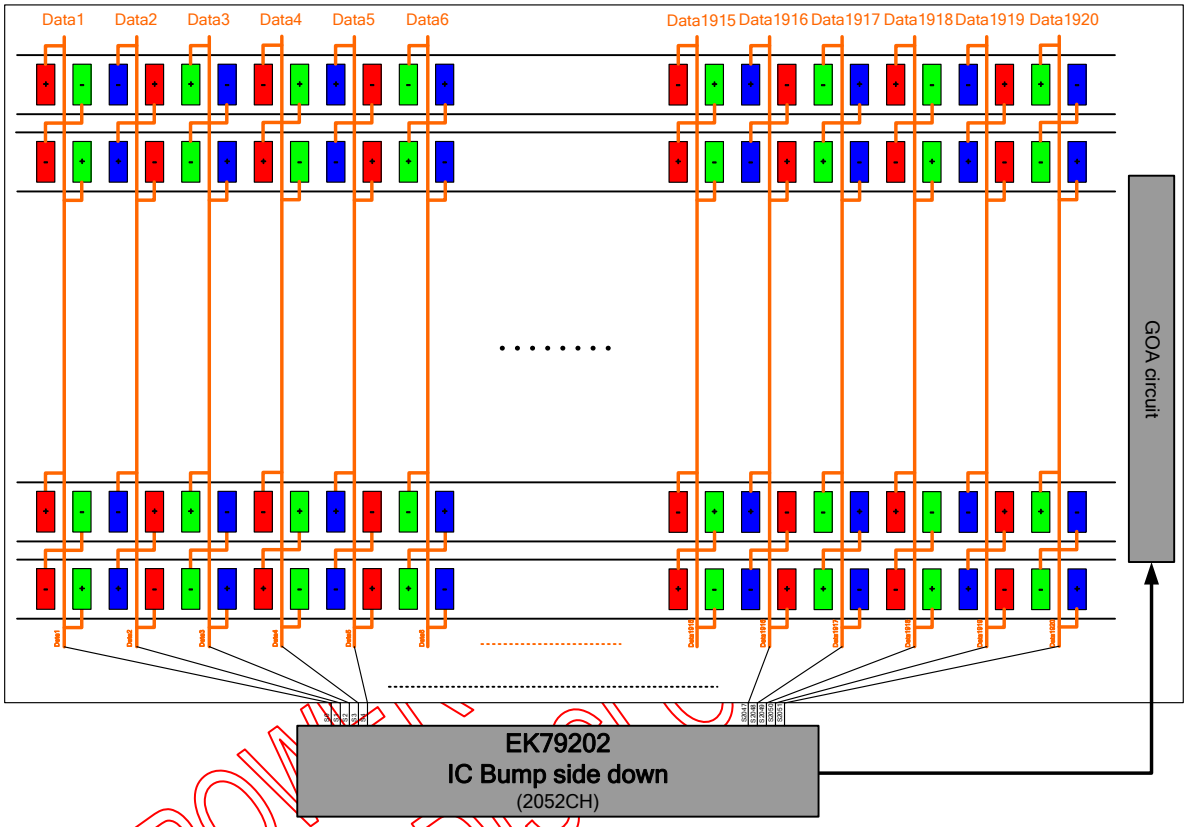
Driving method : Cascade=0



Resolution	Source channel	Disable channel
1280RGBx800	S[960:0] and S[2051:1091]	S[1090:961]

5.4 GIP Application_1024RGBx768 (Normal Dual Gate Driving)

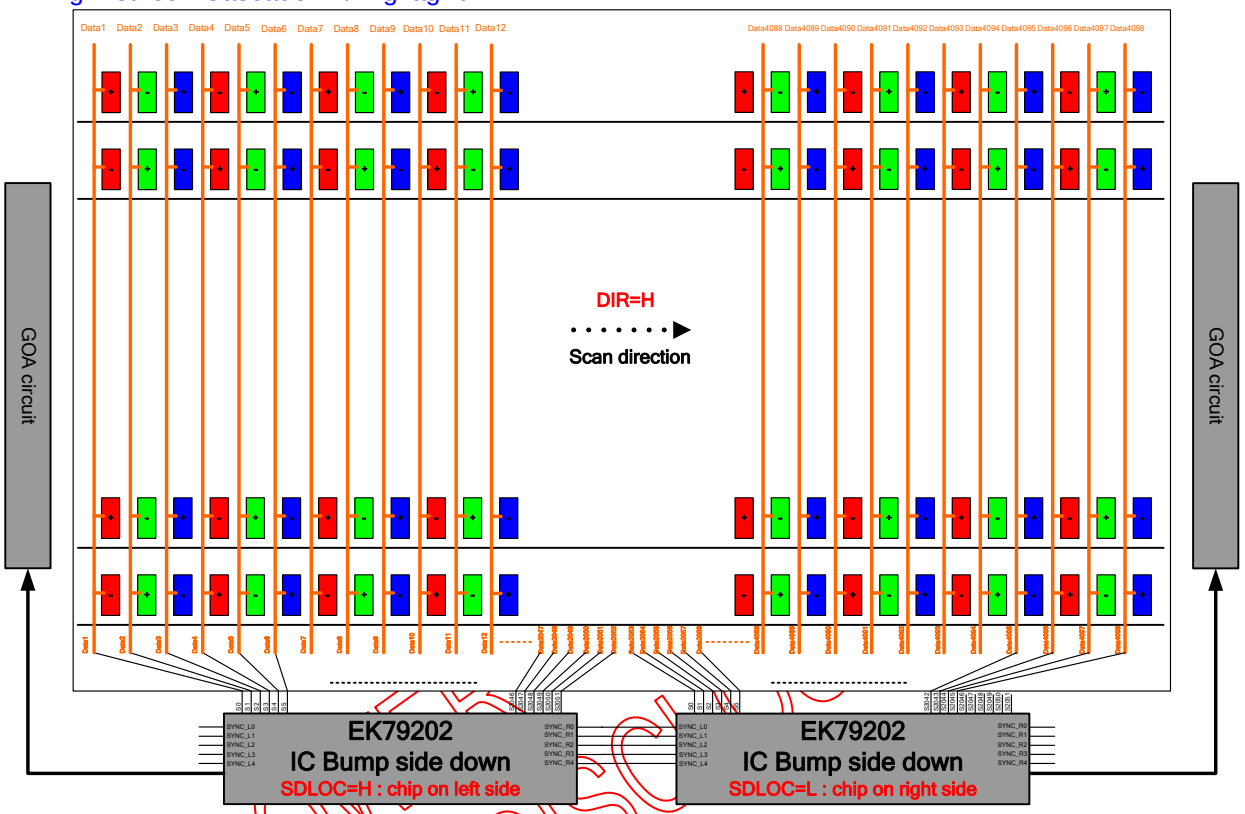
Driving method : Cascade=0



Resolution	Source channel	Disable channel
1024RGBx768	S[767:0] and S[2051:1284]	S[1283:768]

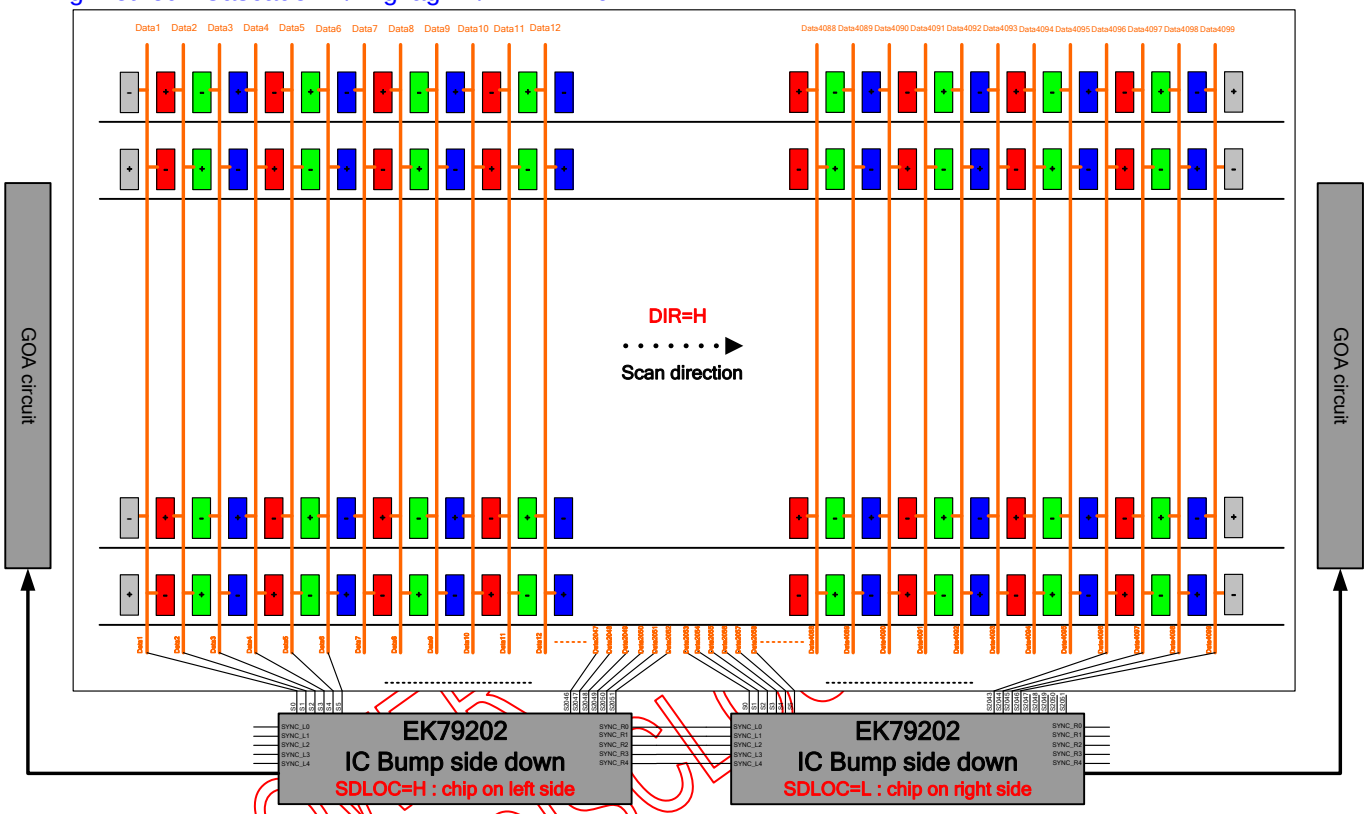
5.5 Cascade Application1_1366RGBx768

Driving method : Cascade=1 / Zigzag=0



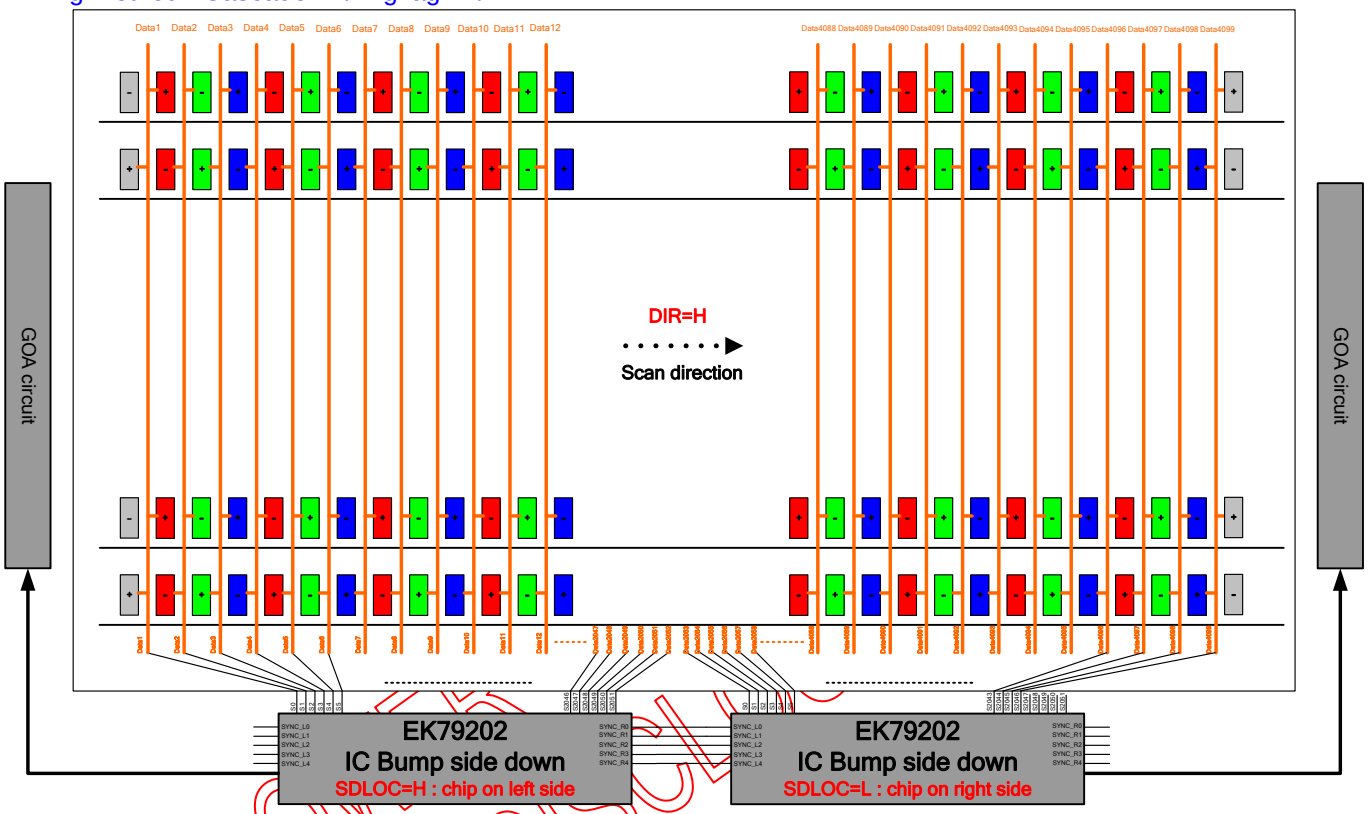
5.6 Cascade Application2_1366RGBx768

Driving method : Cascade=1 / Zigzag=1 / ZTYPE=0



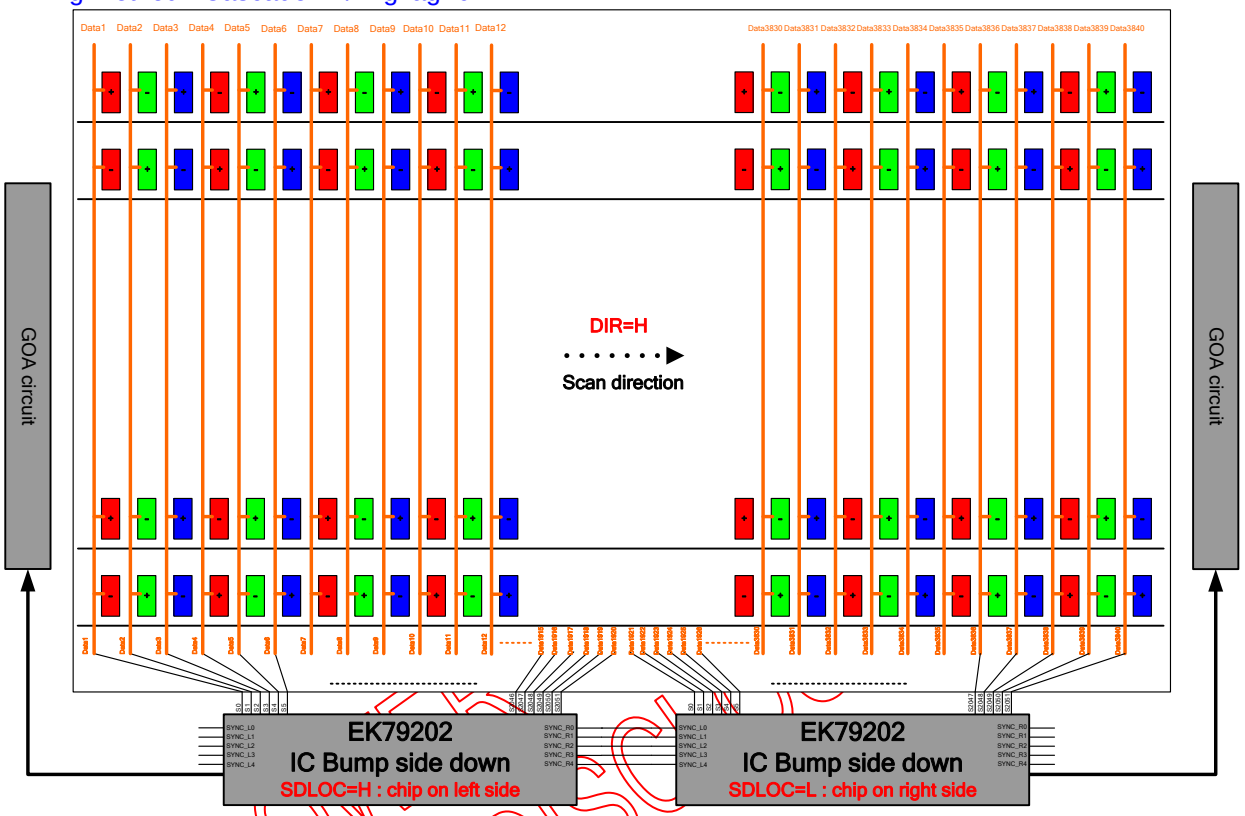
5.7 Cascade Application3_1366RGBx768

Driving method : Cascade=1 / Zigzag=1 / ZTYPE=1



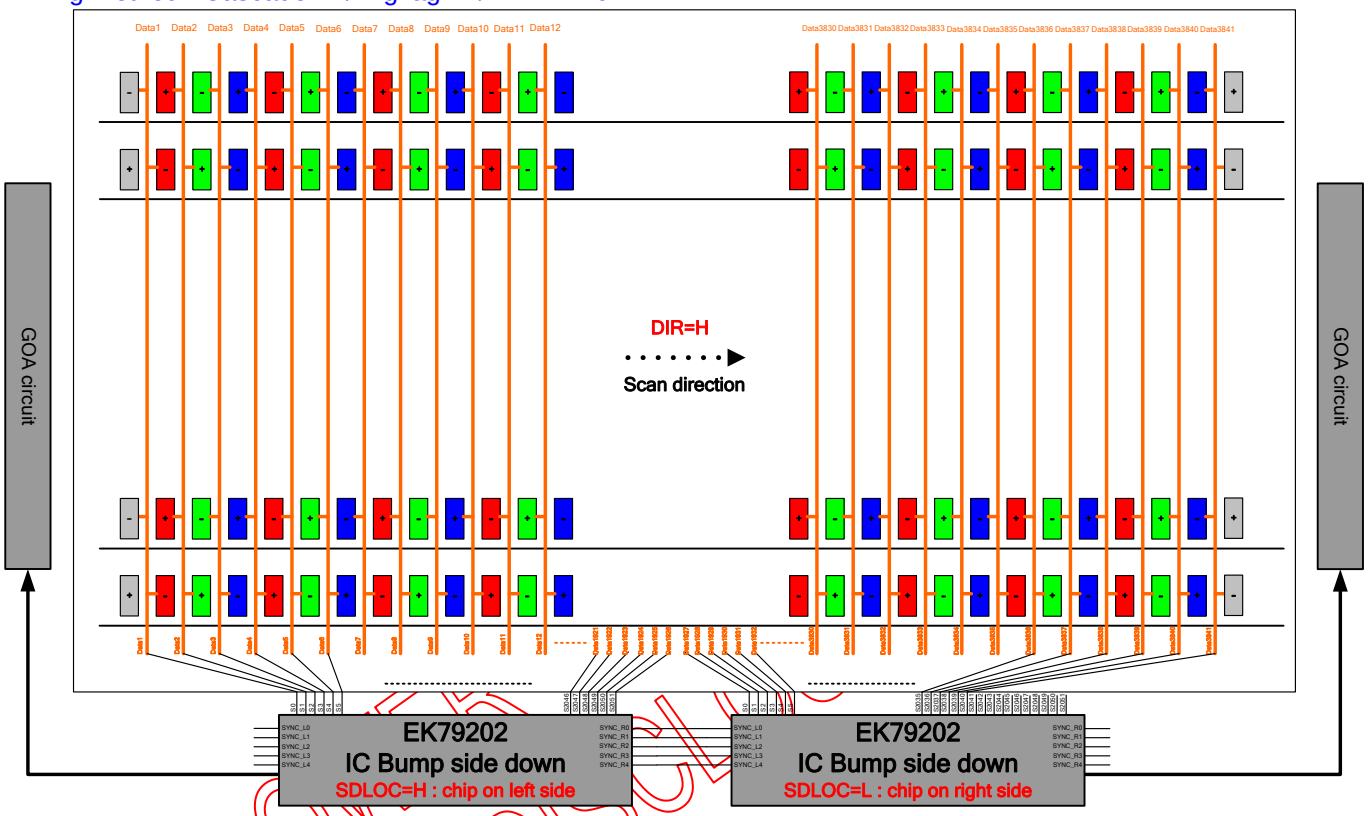
5.8 Cascade Application4_1280RGBx800

Driving method : Cascade=1 / Zigzag=0



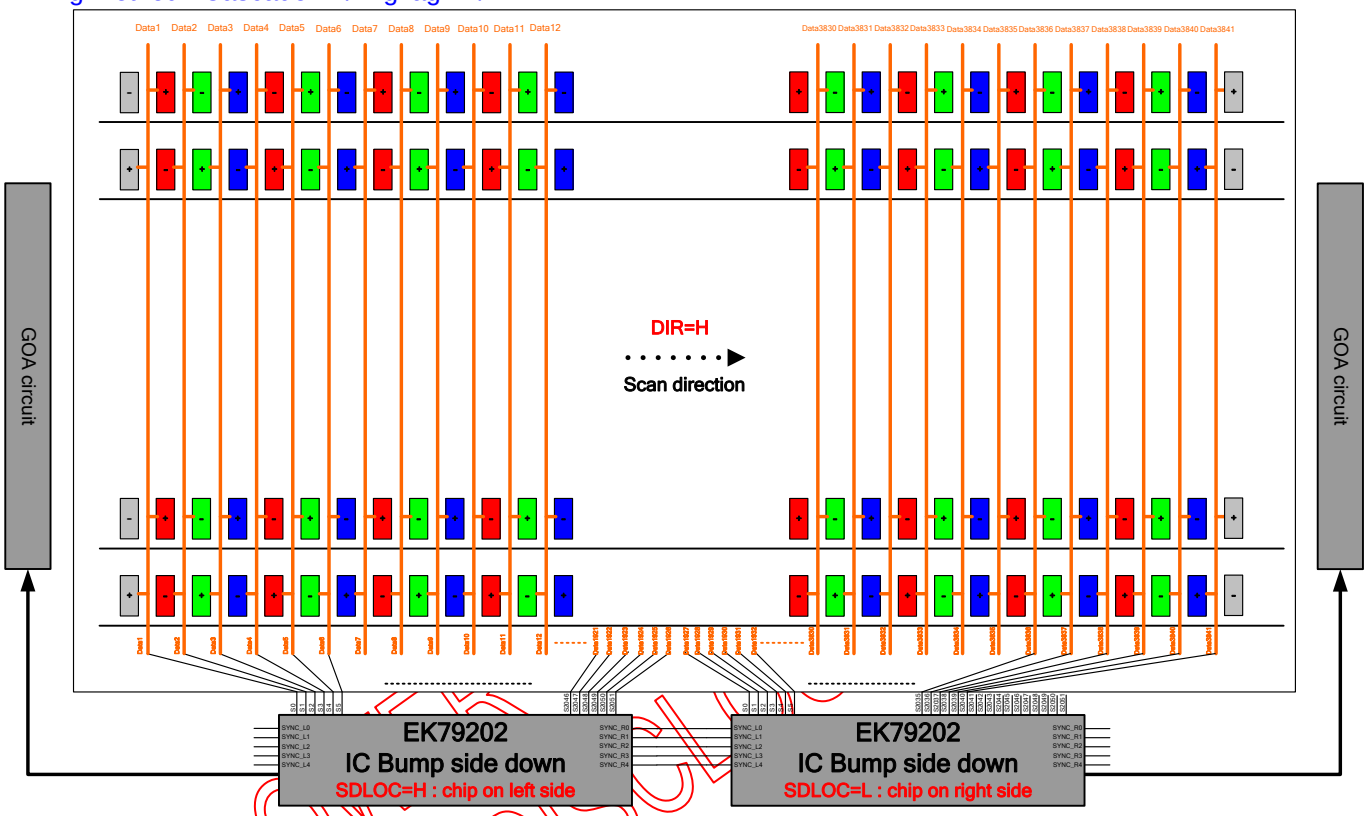
5.9 Cascade Application5_1280RGBx800

Driving method : Cascade=1 / Zigzag=1 / ZTYPE=0

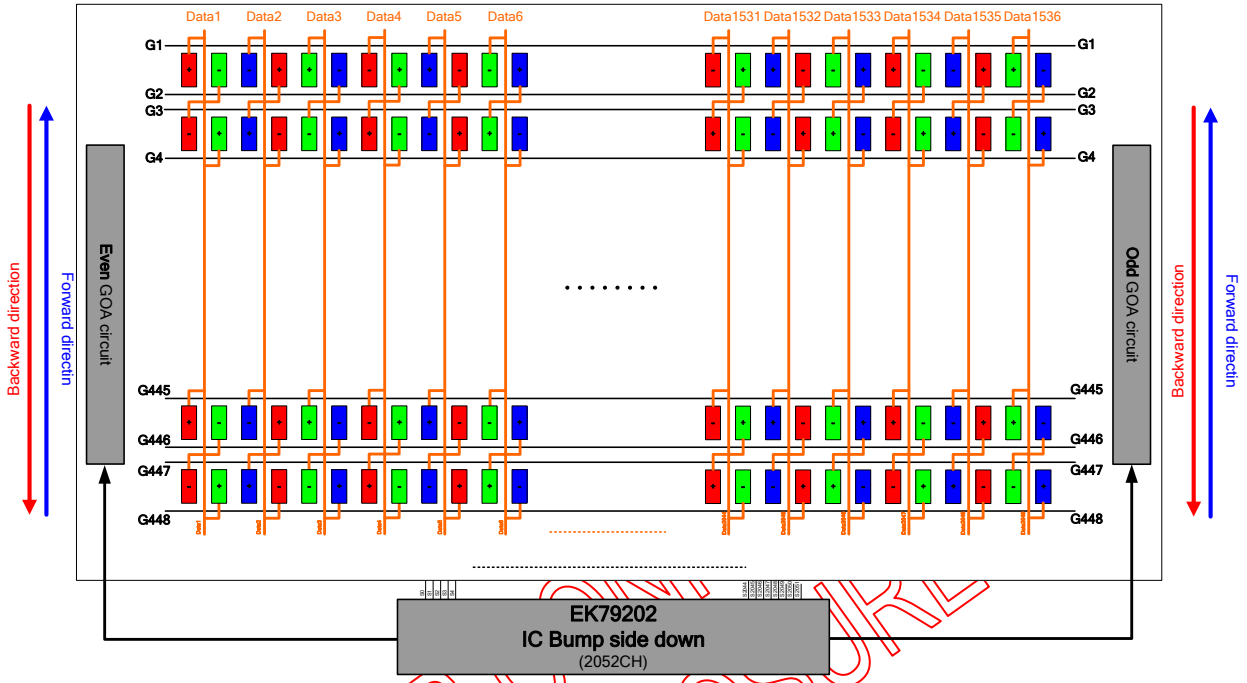


5.10 Cascade Application6_1280RGBx800

Driving method : Cascade=1 / Zigzag=1 / ZTYPE=1

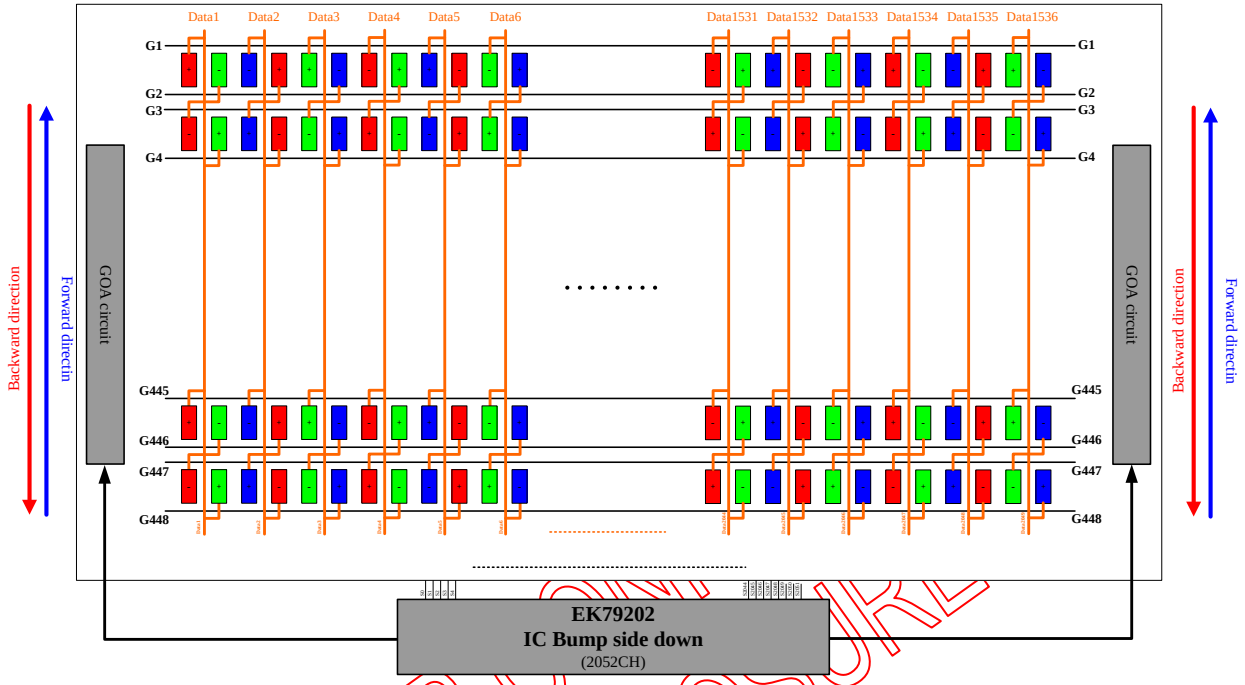


5.11 Dual gate & GOA Application note



		UPDN=L	UPDN=H
Backward direction	Source	**Data1 :** R>G>R>G	**Data1 :** G>R>G>R
	GOA	G1>G2>G3>G4・・・	G2>G1>G4>G3・・・
Forward direction	Source	**Data1 :** R>G>R>G	**Data1 :** G>R>G>R
	GOA	G447>G448>G445>G446・・・	G448>G447>G446>G445・・・

5.12 Normal Dual gate & GOA Application note



Backward direction	UPDN=L	Source	**Data1 :** R>G>R>G
		GOA	G1>G2>G3>G4 • • •
Forward direction	UPDN=H	Source	**Data1 :** G>R>G>R
		GOA	G448>G447>G446>G445 • • •

6. Pin Function Description

6.1 Pin define

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td colspan="3">Interface and Control</td></tr>
<tr><td>DP[0]/DN[0]
DP[1]/DN[1]
DP[2]/DN[2]
DP[3]/DN[3]</td><td>Input</td><td>data Input.
Select by IFSEL[1:0] pin</td></tr>
<tr><td>CKP/CKN</td><td>Input</td><td>LVDS clock Input.</td></tr>
<tr><td>IFSEL[1:0]
(VDDIO)</td><td>Input</td><td>LVDS Interface selection. Normally pull high.
<table>
<tr><th>IFSEL1</th><th>IFSEL0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>LVDS</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>LNSW[1:0]
(VDDIO)</td><td>Input</td><td>LVDS data/clk lane swapping selection pins:
<table>
<tr><th rowspan="2">LNSW[1:0]</th><th colspan="5">LVDS Lane Mapping</th></tr>
<tr><th>D0(PAD)</th><th>D1(PAD)</th><th>CLK(PAD)</th><th>D2(PAD)</th><th>D3(PAD)</th></tr>
<tr><td>00</td><td>D0</td><td>D1</td><td>CLK</td><td>D2</td><td>D3</td></tr>
<tr><td>01</td><td>D0</td><td>D1</td><td>D2</td><td>CLK</td><td>D3</td></tr>
<tr><td>10</td><td>D3</td><td>D2</td><td>CLK</td><td>D1</td><td>D0</td></tr>
<tr><td>11</td><td>D3</td><td>CLK</td><td>D2</td><td>D1</td><td>D0</td></tr>
</table>
Note: (1) LVDS data lane sequence are used when IFSEL[1:0]=[0:1]
(2) Refer to Note2</td></tr>
<tr><td>PNSW
(VDDIO)</td><td>Input</td><td>LVDS polarity selection pins. Normally pull low.
<table>
<tr><th rowspan="2">PNSW</th><th colspan="5">Lane Mapping</th></tr>
<tr><th>D0P/N</th><th>D1P/N</th><th>CLKP/N</th><th>D2P/N</th><th>D3P/N</th></tr>
<tr><td>0</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
<tr><td>1</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D2N/P</td><td>D3N/P</td></tr>
</table></td></tr>
<tr><td>RES[2:0]
(VDDIO)</td><td>Input</td><td>Panel resolution setting selection: Normally pull high
<table>
<tr><th>RES[2]</th><th>RES[1]</th><th>RES[0]</th><th>Description</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>800RGBx600</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>960RGBx640</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1024RGBx600</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1280RGBx800</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1280RGBx800</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1366RGBx768</td></tr>
</table>
Note:
LVDS mode : RES[2:0] setting only for resolution function,
Zigzag panel structure setting depend on ZIGZAG & ZTYPE pin selection(Select by pin or OTP)
Vertical display line set by internal OTP.</td></tr>
<tr><td>DIR
(VDDIO)</td><td>Input</td><td>The shift direction of device internal shift register is controlled by this as shown below : Normally pull high
<table>
<tr><th>DIR</th><th>Function</th></tr>
<tr><td>H</td><td>OUT[0,1,2]→・・・→OUT[2049,2050,2051]</td></tr>
<tr><td>L</td><td>OUT[2049,2050,2051]→・・・→OUT[0,1,2]</td></tr>
</table>
Cascade=H + RES[2:0]=1366x768 only support DIR=H</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>REV
(VDDIO)</td><td>Input</td><td>Controls whether the data of D0~D2 are inverted or not, Normally pull low.
When “REV”=1 these data will be inverted. EX. “00”→“ 3F”, “07”→“ 38”,
“15”→“2A”, and so on.</td></tr>
<tr><td>OP_DRV[1:0]
(VDDIO)</td><td>Input</td><td>Source OP driving selection:
<table>
<tr><th>OP_DRV[1]</th><th>OP_DRV[0]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>75%</td></tr>
<tr><td>0</td><td>1</td><td>100%</td></tr>
<tr><td>1</td><td>0</td><td>125%</td></tr>
<tr><td>1</td><td>1</td><td>133%</td></tr>
</table></td></tr>
<tr><td>DVCOM_WP
(VDDIO)</td><td>Input</td><td>Write protection for internal OTP. Normally High-Z
<table>
<tr><th>DVCOM_WP</th><th>Function</th></tr>
<tr><td>H</td><td>Enable write protect (default)</td></tr>
<tr><td>L</td><td>Disable write protect</td></tr>
</table></td></tr>
<tr><td>DVCOM_EN
(VDDIO)</td><td>Input</td><td>DVCOM selection: Normally pull low
<table>
<tr><th>DVCOM_EN</th><th>Function</th></tr>
<tr><td>H</td><td>Enable DVCOM (internal VCOM output)</td></tr>
<tr><td>L</td><td>Disable DVCOM (VCOM input from external power)</td></tr>
</table></td></tr>
<tr><td>GIP_LRSEL[1:0]
(VDDIO)</td><td>Input</td><td>GIP Level shift selection : Normally pull high
<table>
<tr><th>GIP_LRSEL[1]</th><th>GIP_LRSEL [0]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Disable GIP level shift function</td></tr>
<tr><td>0</td><td>1</td><td>Enable GIP level shift on left side(right off)</td></tr>
<tr><td>1</td><td>0</td><td>Enable GIP level shift on right side(left off)</td></tr>
<tr><td>1</td><td>1</td><td>Enable GIP level shift on left and right side</td></tr>
</table>GATE_SW[1:0]=[0:0] disable GIP level shift.(GIP signal pull low)</td></tr>
<tr><td>GATE_SW[1:0]</td><td>Input</td><td>Pin normally pull high
<table>
<tr><th>GATE_SW [1]</th><th>GATE_SW [0]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>Internal GIP</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>INV_SEL[1:0]
(VDDIO)</td><td>Input</td><td>Inversion mode selection: Normally pull low.
<table>
<tr><th rowspan="2">INV_SEL
[1:0]</th><th colspan="4">LVDS</th></tr>
<tr><th colspan="2">Cascade mode
(CAS=1)</th><th colspan="2">Dual gate
(CAS=0)</th></tr>
<tr><th>Normal type
(ZIGZAG=0)</th><th>Zigzag type
(ZIGZAG=1)</th><th>Normal type
(ZIGZAG=0)</th><th>Zigzag type
(ZIGZAG=1)</th></tr>
<tr><td>00</td><td>1 line</td><td>Column</td><td>1+2dot</td><td>Column</td></tr>
<tr><td>01</td><td>2 line</td><td>Column</td><td>2dot</td><td>Column</td></tr>
<tr><td>10</td><td>1+2line</td><td>Column</td><td>2line2dot</td><td>Column</td></tr>
<tr><td>11</td><td>Column</td><td>Column</td><td>-</td><td>Column</td></tr>
</table>Note : Four line inversion select by OTP</td></tr>
<tr><td>SCAN_SEL</td><td>Input</td><td>
<table>
<tr><th>SCAN_SEL</th><th>Function</th></tr>
<tr><td>H</td><td>Inverse Z scan : G→R→G→R</td></tr>
<tr><td>L</td><td>Z scan : R→G→R→G(default)</td></tr>
</table>Note: (Only for Normal dual gate type driving)
Source mapping depend on external gate signal</td></tr>
<tr><td>FRAME</td><td>Input</td><td>Frame inverse or not select. Normally pull low
<table>
<tr><th>FRAME</th><th>Function</th></tr>
<tr><td>H</td><td>Uniform</td></tr>
<tr><td>L</td><td>Frame inverse(default)</td></tr>
</table>Note: (Only for Normal dual gate type driving)
INV_SEL[1:0]=[1:1] : FRAME pin function is ignored</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>CAS</td><td>Input</td><td>Cascade mode selection: Normally pull high
<table>
<tr><th>Cascade</th><th>Function</th></tr>
<tr><td>H</td><td>Cascade mode(default)</td></tr>
<tr><td>L</td><td>Dual gate mode</td></tr>
</table>
Refer to application Block diagram</td></tr>
<tr><td>SDLOC</td><td>Input</td><td>Source driver location definition pin. Normally pull high
<table>
<tr><th>SDLOC</th><th>Function</th></tr>
<tr><td>H</td><td>Source driver locate on left side</td></tr>
<tr><td>L</td><td>Source driver locate on right side</td></tr>
</table>
Refer to application Block diagram
Note : internal default Master/Slave follow TP[52:51] setting</td></tr>
<tr><td>ZIGZAG</td><td>Input</td><td>Zigzag driving method setting. Normally pull high
<table>
<tr><th>ZIGZAG</th><th>Function</th></tr>
<tr><td>H</td><td>Zigzag driving method</td></tr>
<tr><td>L</td><td>Normal driving method</td></tr>
</table>
Refer to application Block diagram</td></tr>
<tr><td>ZTYPE</td><td>Input</td><td>Zigzag panel layout type selection. Normally pull low
<table>
<tr><th>ZTYPE</th><th>Function</th></tr>
<tr><td>H</td><td>Zigzag layout type1</td></tr>
<tr><td>L</td><td>Zigzag layout type0</td></tr>
</table>
Refer to application Block diagram(only for CAS=H and Zigzag=H)</td></tr>
<tr><td>RESETB
(VDDIO)</td><td>Input</td><td>Global reset pin. Normally pull high.
<table>
<tr><th>RESETB</th><th>Function</th></tr>
<tr><td>H</td><td>Normal operation (default)</td></tr>
<tr><td>L</td><td>The controller is in reset state</td></tr>
</table>
Suggest to connecting with an RC reset circuit for stability.</td></tr>
<tr><td>STBYB
(VDDIO)</td><td>Input</td><td>Standby mode. Normally pull high. STBYB = L, timing controller, source driver will turn off, all output are High-Z.
STBYB = H, normal operation. (Default)</td></tr>
<tr><td>BISTB
(VDDIO)</td><td>Input</td><td>Normal Operation/BIST pattern select. Normally pull high.
<table>
<tr><th>BISTB</th><th>Function</th></tr>
<tr><td>H</td><td>Normal operation (default)</td></tr>
<tr><td>L</td><td>BIST mode</td></tr>
</table></td></tr>
<tr><td>LVFMT
(VDDIO)</td><td>Input</td><td>8-bit input format select for LVDS mode. Normally pull high.
(only for LVDS)
<table>
<tr><th>LVFMT</th><th>Function</th></tr>
<tr><td>H</td><td>VESA format (default)</td></tr>
<tr><td>L</td><td>JEIDA format</td></tr>
</table></td></tr>
<tr><td>LVBIT
(VDDIO)</td><td>Input</td><td>6-bit / 8-bit input select for LVDS mode. Normally pull high.
(only for LVDS)
<table>
<tr><th>LVBIT</th><th>Function</th></tr>
<tr><td>H</td><td>8-bit (default)</td></tr>
<tr><td>L</td><td>6-bit</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>DITHER_EN
(VDDIO)</td><td>Input</td><td>Dithering function enable control. Normally pull low
In LVDS 6-bit mode, IC don’t care DITHER and HFRC setting.
<table><tr><th>DITHER_EN</th><th>Function</th></tr><tr><td>H</td><td>Enable internal dithering function</td></tr><tr><td>L</td><td>Disable internal dithering function</td></tr></table></td></tr>
<tr><td>HFRC_EN
(VDDIO)</td><td>Input</td><td>H-FRC selection. Normally pull low
HFRC = H : H-FRC enable
If “DITHER”=”L”,disable dithering function(HFRC and FRC disable)</td></tr>
<tr><td>CMD_SEL
(VDDIO)</td><td>Input</td><td>Command interface selection. Normally pull high.
<table><tr><th>CMD_SEL</th><th>Function</th></tr><tr><td>H</td><td>I2C (default)</td></tr><tr><td>L</td><td>3-Wire</td></tr></table>3-wire/I2C command can’t receive at the same time.</td></tr>
<tr><td>UPDN
(VDDIO)</td><td>Input</td><td>Setting flexible GOA scan function. Normally pull low.
If “UPDN”=“H”, support backward scan
If “UPDN”=“L”, support forward scan
(Forward/Backward Flexible GOA setting by Reg.)</td></tr>
<tr><td>A0</td><td>Input</td><td>Serial interface (I2C) Compatible Device Address Bit 0 input.
Normally pull high.</td></tr>
<tr><td>LEDON</td><td>Output</td><td>Back-light enable signal.
Note:
Available at normal display
unused floating.</td></tr>
<tr><td>CSB
(VDDIO)</td><td>Input</td><td>Serial communication enables. Normally pull high
Note: unused floating</td></tr>
<tr><td>SCL
(VDDIO)</td><td>Input</td><td>Serial communication clock input.
Note: unused floating</td></tr>
<tr><td>SDA
(VDDIO)</td><td>I/O</td><td>Serial communication data input.
Note: unused floating</td></tr>
<tr><td>SCL_I2C
(VDDIO)</td><td>Input</td><td>Serial communication clock input.
Note: unused floating</td></tr>
<tr><td>SDA_I2C
(VDDIO)</td><td>I/O</td><td>Serial communication data input.
Note: unused floating</td></tr>
<tr><td>PWR_EN</td><td>Output</td><td>Enable power for external power IC
Note: unused floating</td></tr>
</table>

<table>
<tr><td colspan="3">Panel driver output</td></tr>
<tr><td>S[2051:0]</td><td>Output</td><td>Source output mapping with different resolution.2051
Source output control by RES[2:0] pin define
On Dual gate mode : CAS=0
<table>
<tr><th>Resolution</th><th>Source channel</th><th>Disable channel</th></tr>
<tr><td>1366RGBx768</td><td>S[2051:0]</td><td>-</td></tr>
<tr><td>1280RGBx800</td><td>S[959:0] and S[2051:1092]</td><td>S[1091:960]</td></tr>
<tr><td>1024RGBx600</td><td>S[767:0] and S[2051:1284]</td><td>S[1283:768]</td></tr>
<tr><td>960RGBx640</td><td>S[719:0] and S[2051:1332]</td><td>S[1331:720]</td></tr>
<tr><td>800RGBx600</td><td>S[599:0] and S[2051:1452]</td><td>S[1451:600]</td></tr>
</table>
On Cascade mode : CAS=1(single gate)
<table>
<tr><td rowspan="2">Resolution</td><td colspan="2">Chip on left side</td><td colspan="2">Chip on right side</td></tr>
<tr><td>Source channe</td><td>Disable channel</td><td>Source channel</td><td>Disable channel</td></tr>
<tr><td>1366RGBx768</td><td>S[2051:0]</td><td>-</td><td>S[2051:0]</td><td>-</td></tr>
<tr><td>1280RGBx800</td><td>S[959:0] and S[2051:1092]</td><td>S[1091:960]</td><td>S[959:0] and S[2051:1092]</td><td>S[1091:960]</td></tr>
<tr><td>1024RGBx600</td><td>S[767:0] and S[2051:1284]</td><td>S[1283:768]</td><td>S[767:0] and S[2051:1284]</td><td>S[1283:768]</td></tr>
<tr><td>960RGBx640</td><td>S[719:0] and S[2051:1332]</td><td>S[1331:720]</td><td>S[719:0] and S[2051:1332]</td><td>S[1331:720]</td></tr>
<tr><td>800RGBx600</td><td>S[599:0] and S[2051:1452]</td><td>S[1451:600]</td><td>S[599:0] and S[2051:1452]</td><td>S[1451:600]</td></tr>
</table>
Note:
Chip position refer to application Block diagram</td></tr>
<tr><td>GOUTL[1]~ GOUTL[22]</td><td>Output</td><td>These pins are used for Panel gate control signals. If not used, let it open.</td></tr>
<tr><td>GOUTR[1]~ GOUTR[22]</td><td>Output</td><td>These pins are used for Panel gate control signals. If not used, let it open.</td></tr>
<tr><td colspan="3">Power</td></tr>
<tr><td>VDD</td><td>PI</td><td>A power supply for analog circuit. VDD=2.3V to 3.6V</td></tr>
<tr><td>VDDIO</td><td>PI</td><td>A power supply for the I/O circuit. VDDIO=2.3V to 3.6V</td></tr>
<tr><td>VDD_15V</td><td>PO</td><td>Internal power supply for logic circuits. Connect to a stabilizing capacitor.</td></tr>
<tr><td>VDD_15V_IF</td><td>PO</td><td>Internal power supply for LVDS circuits. Connect to a stabilizing capacitor.</td></tr>
<tr><td>VDD_IF</td><td>PI</td><td>Interface and I/O power supply for the LVDS power regulator circuits. VDDIO=2.3V to 3.6V. .</td></tr>
<tr><td>VSS</td><td>PI</td><td>GND for the internal logic. VSS=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.</td></tr>
<tr><td>VSS_IF</td><td>PI</td><td>Ground for interface.</td></tr>
<tr><td>VSSA</td><td>PI</td><td>Analog ground. VSS=0V. When using the COG method, connect to VSS on the FPC to prevent noise.</td></tr>
<tr><td>VSP</td><td>PI</td><td>Input voltage from the set-up circuit (4.5V to 6.0V).</td></tr>
<tr><td>VSN</td><td>PI</td><td>Input voltage from the set-up circuit (-4.5V to -6.0V).</td></tr>
<tr><td>VGMP</td><td>PO</td><td>Positive regulated voltage output (3.728V to 5.76V)</td></tr>
<tr><td>VGMN</td><td>PO</td><td>Negative regulated voltage output (-3.728V to -5.76V)</td></tr>
<tr><td>VGH</td><td>PI</td><td>Connect to stabilizing capacitor between VSSA and VGH.</td></tr>
<tr><td>VGL</td><td>PI</td><td>Connect to stabilizing capacitor between VSSA and VGL.</td></tr>
<tr><td>VGH_REG</td><td>PO</td><td>Regulator output voltage generated from VGH. Connect to a stabilizing capacitor between VSSA and VGH_REG. If not used, please open.</td></tr>
<tr><td>VGL_REG</td><td>PO</td><td>Regulator output voltage generated from VGL. Connect to a stabilizing capacitor between VSSA and VGL_REG. If not used, please open.</td></tr>
<tr><td>VCL</td><td>PO</td><td>Input voltage from the set-up circuit(VSN+2.4V). It is generated from VSN.</td></tr>
<tr><td>VCOM</td><td>PO</td><td>The power supply of common voltage in DC com driving. The voltage range is set between -0.55V to -2.46V. It must connected a stabilizing capacitor 2.2u to VSS.</td></tr>
</table>

Other pins		
PASS1_R/PASS2_R	-	Pass line
PASS1_L/PASS2_L	-	Pass line
SYNC_L[4:0]	I/O	Sync signal for IC control. **Refer to application Block diagram**
SYNC_R[4:0]	I/O	Sync signal for IC control. **Refer to application Block diagram**
T_S[114]/T_S[115]	O	Source channel output pin.
T_S[1195]/T_S[1196]	O	Source channel output pin.
DUMMY	T	Test pin. Float these pins for normal operation.
TP[77:0]	T	Test pin. Float these pins for normal operation.
T_VTSEN[2:0]	T	Test pin. Float these pins for normal operation.

Note: P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, T: Testing, SH: Shielding, PS: Power Setting, C: Capacitor pin.

6.2 Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Source wiring:

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
VDD	< 5	T_VTSEN[2]	< 100
VDD_IF	< 5	T_VTSEN[1]	< 100
VDDIO	< 5	T_VTSEN[0]	< 100
VDD_15V	< 5	DUMMY	< 100
VDD_15V_IF	< 5	SHIELDING	< 100
VSP	< 5	DP[0]/DN[0]	< 5
VSN	< 5	DP[1]/DN[1]	< 5
VGH	< 5	DP[2]/DN[2]	< 5
VGL	< 5	DP[3]/DN[3]	< 5
VGMP	< 5	CKP/CKN	< 5
VGMN	< 5	DIR	<100
VGH_REG	< 5	GOUTR[1]~GOUTR[22]	< 50
VGL_REG	< 5	GOUTL[1]~GOUTL[22]	< 50
VCOM	< 5	SCL	< 50
VSSA	< 5	SDA	< 50
VSS_IF	< 5	SCL_I2C	< 50
VSS	< 5	SDA_I2C	< 50
RES[2:0]	< 100	VCL	< 5
STBYB	< 100	CMD_SEL	< 100
RESETB	< 100	LNSW[1:0]	< 100
PNSW	< 100	GATE_SW[1:0]	< 100
REV	< 100	SYNC_R[0]~SYNC_R[4]	< 100
LVFMT	< 100	SYNC_L[0]~SYNC_L[4]	< 100
LVBIT	< 100	UPDN	< 100
IFSEL[1:0]	< 100	CSB	< 50
DVCOM_WP	< 100	TP	<100
CS_SD	< 100	ZIGZAG	<100
CS_GIP	< 100	ZTYPE	<100
BISTB	< 100	HFRC_EN	<100
LEDPWM	< 50	FRAME	<100
LEDON	< 50	A0	<100
SDLOC	<100	DVCOM_EN	<100
DITHER_EN	<100	PWR_EN	<100
SCAN_SEL	<100	INV_SEL	<100
T_S[1996:1995]/ T_S[115:114]	<50	CAS	<100
OP_DRV	<100	GIP_LRSEL	<100

6.3 GOUT Power domain for GIP Application

-	Pad Power Domian
GOUTR[1]	VGH~VGL_REG
GOUTR[2]	VGH~VGL_REG
GOUTR[3]	VGH~VGL
GOUTR[4]	VGH~VGL
GOUTR[5]	VGH~VGL
GOUTR[6]	VGH~VGL
GOUTR[7]	VGH~VGL
GOUTR[8]	VGH~VGL
GOUTR[9]	VGH~VGL
GOUTR[10]	VGH~VGL
GOUTR[11]	VGH~VGL
GOUTR[12]	VGH~VGL
GOUTR[13]	VGH~VGL
GOUTR[14]	VGH~VGL
GOUTR[15]	VGH~VGL
GOUTR[16]	VGH~VGL
GOUTR[17]	VGH~VGL
GOUTR[18]	VGH~VGL
GOUTR[19]	VGH~VGL
GOUTR[20]	VGH~VGL
GOUTR[21]	VGH~VGL
GOUTR[22]	VGH~VGL

-	Pad Power Domian
GOUTL[1]	VGH~VGL_REG
GOUTL[2]	VGH~VGL_REG
GOUTL[3]	VGH~VGL
GOUTL[4]	VGH~VGL
GOUTL[5]	VGH~VGL
GOUTL[6]	VGH~VGL
GOUTL[7]	VGH~VGL
GOUTL[8]	VGH~VGL
GOUTL[9]	VGH~VGL
GOUTL[10]	VGH~VGL
GOUTL[11]	VGH~VGL
GOUTL[12]	VGH~VGL
GOUTL[13]	VGH~VGL
GOUTL[14]	VGH~VGL
GOUTL[15]	VGH~VGL
GOUTL[16]	VGH~VGL
GOUTL[17]	VGH~VGL
GOUTL[18]	VGH~VGL
GOUTL[19]	VGH~VGL
GOUTL[20]	VGH~VGL
GOUTL[21]	VGH~VGL
GOUTL[22]	VGH~VGL

7. Register Command Format

The EK79202 supports set internal register by I2C interface. I2C interface use different register address.. The SPI and I2C must be ignored its. “SPI/I2C address” showed in register table.

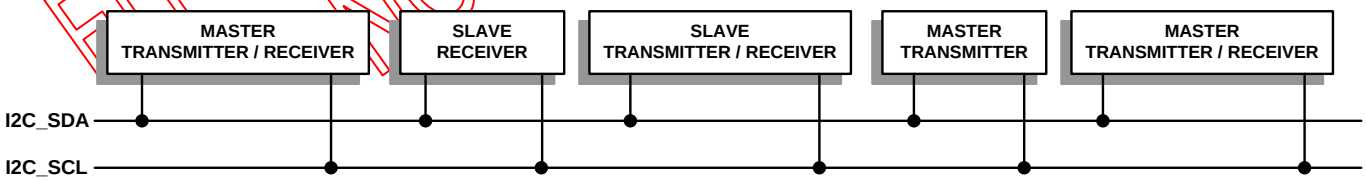
7.1 I2C format

The I^{2}C-bus is for bi-directional, two-line communication between different Ics or modules. The two lines are the Serial Data line (I^{2}C_SDA) and the Serial Clock Line (I^{2}C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

I^{2}C-Bus Protocol:

Before any data is transmitted on the I^{2}C-bus, the device which should respond is addressed first. There are four slave address can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

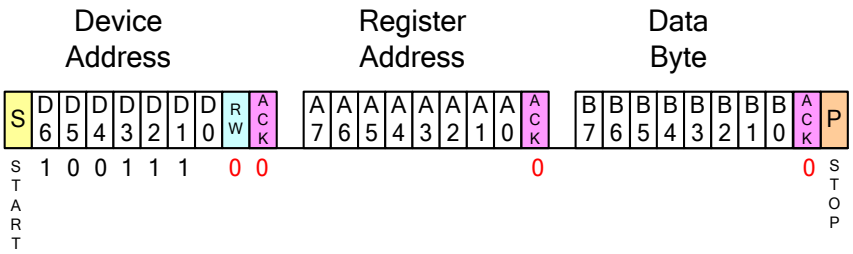
Definitions:
- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



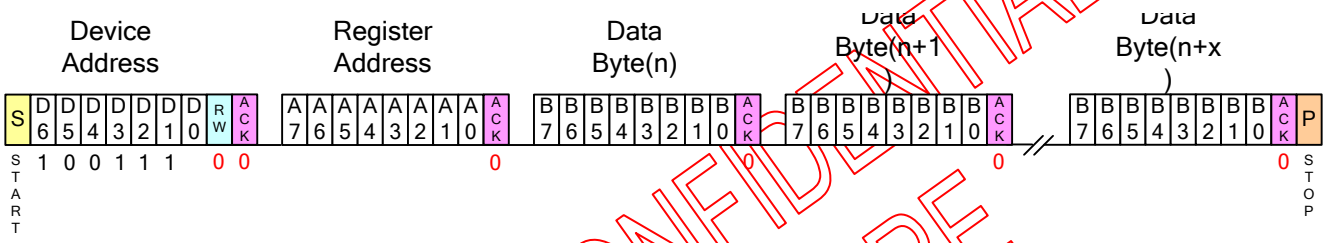
7.1.1 Register Write Sequence of I^{2}C Interface

EK79202 supports register write sequence via I^{2}C-bus transfer. The register writing support single register write mode and multi-register write mode. The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in below.
(2) After the START condition (S), a slave address is sent. R/W bit is setting to “0” for WRITE.
(3) The slave issues an ACK to master.
(4) 8 bits register address transfer first then transfer the register data parameter.
(5) A data transfer is always terminated by a STOP condition.
(6) EK79202 DA[6:0]=100_1111 or DA[6:0]=100_1110



Single Register Writing Timing

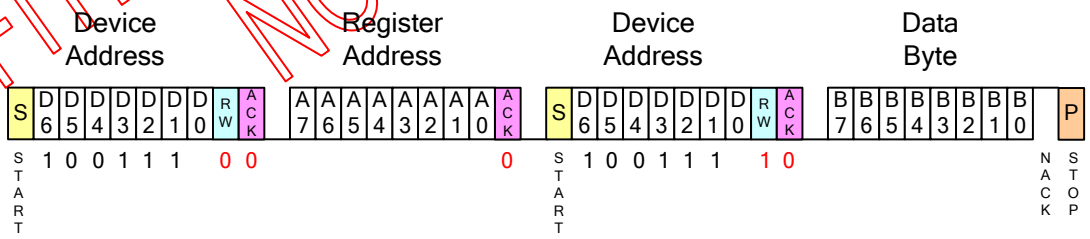


Multi Register Writing Timing

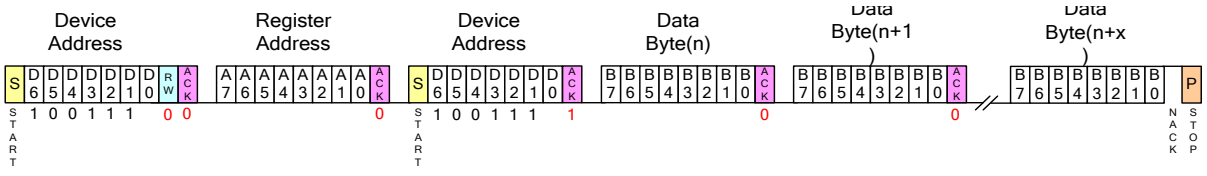
7.1.2 Register Read Sequence of I2C Interface

EK79202 supports register read sequence via I²C-bus transfer. The register reading only support single register read mode.

Register data reading transfers follow the format and is shown in below.



Single Register Reading Timing



Multi Register Reading Timing

7.2 SPI format

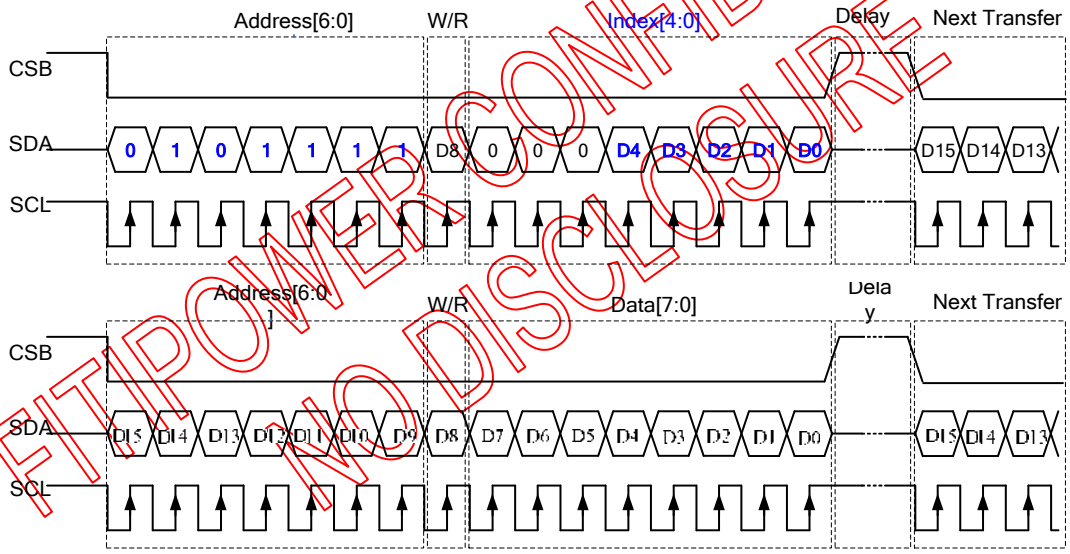
EK79202 use the 3-wire serial port as communication interface for all the function and command setting.

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. EK79202 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.

For prevent from incorrect setting of the internal register. Please refer to the section of “3-Wire Timing. Because the 3-wire only can read/write one address. So we put the “parameter index” at the address 0x2F. When 3-wire command sends, it will refer to the address 0x2F[4:0] as the parameter index value.



3-Wire Command Format:

Bit	Description
D15-D9	Register Address [6:0].
D8	W/R control bit. “0” for Write; “1” for Read
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [6:0]							0	Data (Issue by external controller)							

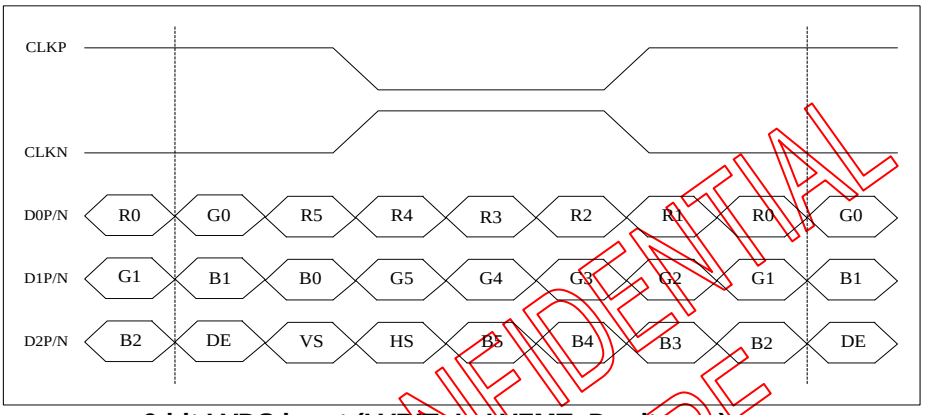
3-Wire Read Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [6:0]							1	Data (Issue by 3-Wire engine)							

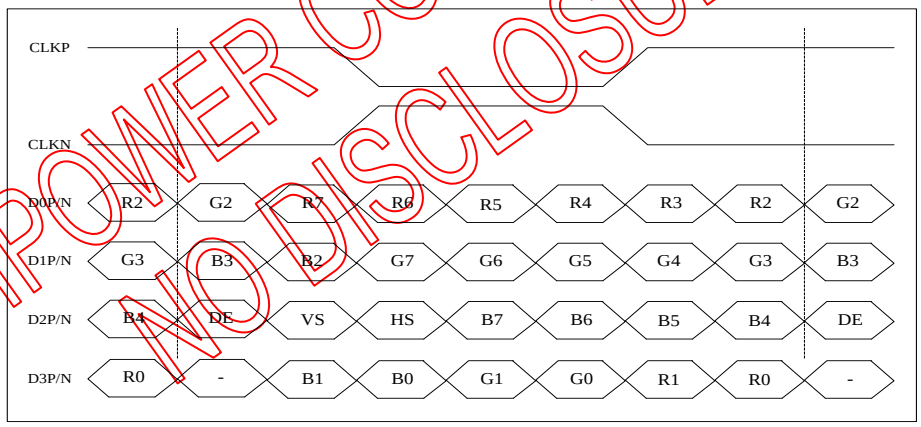
8. Video Interface

8.1 LVDS interface

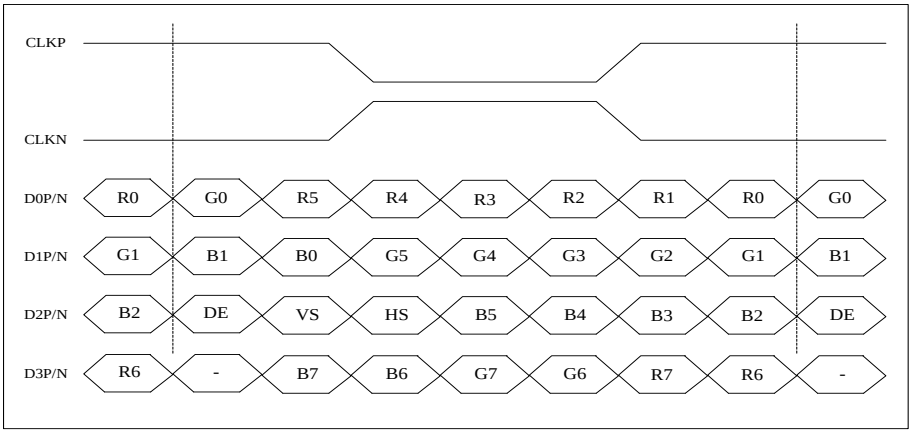
8.1.1 Data input format for LVDS



6-bit LVDS input (LVBIT=L, LVFMT=Don't care)



8-bit LVDS input (LVBIT=H, LVFMT=L)



8-bit LVDS input(LVBIT=H, LVFMT=H)

9. Timing Table

9.1 Input Timing Table

For 1366RGBx768 HV mode

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)		F_{DCLK}	69.7	75	80.9	MHz
HSYNC period time		T_H	1468	1550	1596	DCLK
Horizontal display area		T_{HD}	1366			DCLK
HSYNC pulse width	Min.	T_{HPW}	2			
	Typ.		-			
	Max.		40			
HSYNC back porch(with pulse width)		T_{HBP}	88	88	88	DCLK
HSYNC front porch		T_{HFP}	14	96	142	DCLK
VSYNC period time		T_V	792	806	840	H
Vertical display area		T_{VD}	768			H
VSYNC pulse width	Min.	T_{VPW}	2			H
	Typ.		-			
	Max.		20			
VSYNC back porch(with pulse width)		T_{VBP}	23	23	23	H
VSYNC front porch		T_{VFP}	1	15	49	H

For 1366RGBx768 DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)	F_{DCLK}	69.7	75	80.9	MHz
Horizontal display area	T_{HD}	1366			DCLK
HSYNC period time	T_H	1468	1550	1596	DCLK
HSYNC blanking	$T_{HBP}+T_{HFP}$	102	184	230	DCLK
Vertical display area	T_{VD}	768			H
VSYNC period time	T_V	792	806	840	H
VSYNC blanking	$T_{VBP}+T_{VFP}$	24	38	72	H

For 1280RGBx800

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)		F_{DCLK}	68.2	72.4	78.5	MHz
HSYNC period time		T_H	1380	1440	1500	DCLK
Horizontal display area		T_{HD}		1280		DCLK
HSYNC pulse width	Min.	T_{HPW}		2		
	Typ.			-		
	Max.			40		
HSYNC back porch(with pulse width)		T_{HBP}	88	88	88	DCLK
HSYNC front porch		T_{HFP}	12	72	132	DCLK
VSYNC period time		T_V	824	838	872	H
Vertical display area		T_{VD}		800		H
VSYNC pulse width	Min.	T_{VPW}		2		H
	Typ.			-		
	Max.			20		
VSYNC back porch(with pulse width)		T_{VBP}	23	23	23	H
VSYNC front porch		T_{VFP}	1	15	49	H

For 1280RGBx800 DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)	F_{DCLK}	68.2	72.4	78.5	MHz
Horizontal display area	T_{HD}		1280		DCLK
HSYNC period time	T_H	1380	1440	1500	DCLK
HSYNC blanking	$T_{HBP}+T_{HFP}$	100	160	220	DCLK
Vertical display area	T_{VD}		800		H
VSYNC period time	T_V	824	838	872	H
VSYNC blanking	$T_{VBP}+T_{VFP}$	24	38	72	H

Note:Timing setting base on 60Hz,
Frequency can be adjusted according to needs, as long as it does not affect the display.

For 1280RGBx720

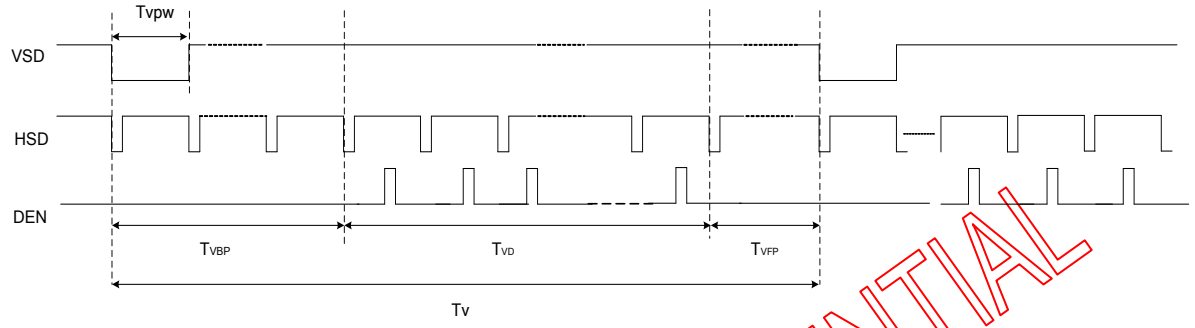
Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)		F_{DCLK}	61.6	65.5	71.3	MHz
HSYNC period time		T_H	1380	1440	1500	DCLK
Horizontal display area		T_{HD}		1280		DCLK
HSYNC pulse width	Min.	T_{HPW}		2		
	Typ.			-		
	Max.			40		
HSYNC back porch(with pulse width)		T_{HBP}	88	88	88	DCLK
HSYNC front porch		T_{HFP}	12	72	132	DCLK
VSYNC period time		T_V	744	758	792	H
Vertical display area		T_{VD}		720		H
VSYNC pulse width	Min.	T_{VPW}		2		H
	Typ.			-		
	Max.			20		
VSYNC back porch(with pulse width)		T_{VBP}	23	23	23	H
VSYNC front porch		T_{VFP}	1	15	49	H

For 1024RGBx768

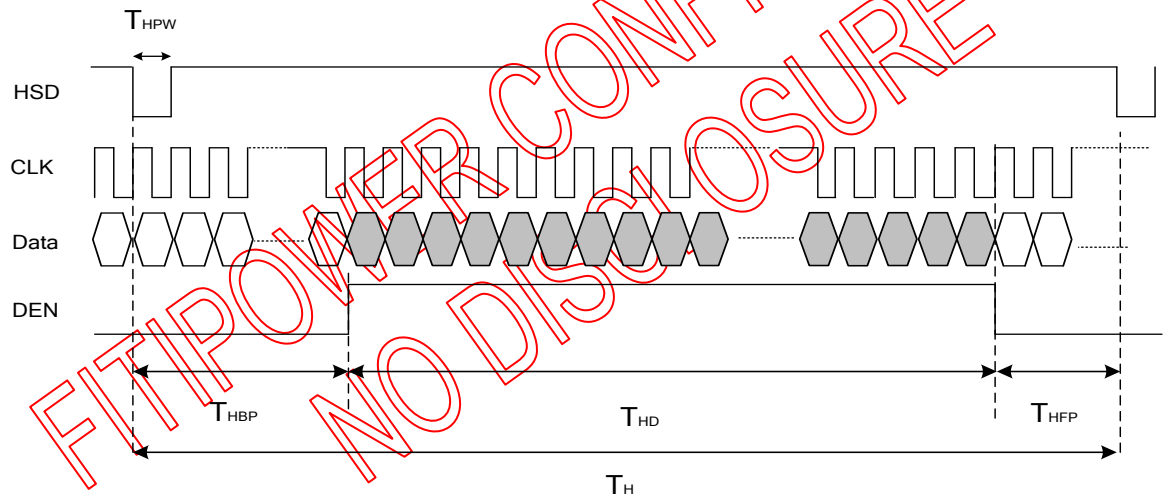
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60hz	F_{DCLK}	52	65	71	Mhz
Horizontal display area	T_{HD}		1024		DCLK
HSYNC period time	T_H	1114	1344	1400	DCLK
HSYNC blanking	$T_{HBP}+T_{HFP}$	90	320	376	DCLK
Vertical display area	T_{VD}		768		H
VSYNC period time	T_V	778	806	845	H
VSYNC blanking	$T_{VBP}+T_{VFP}$	10	38	77	H

Note : Blanking setting must be even numbers.

Vertical timing



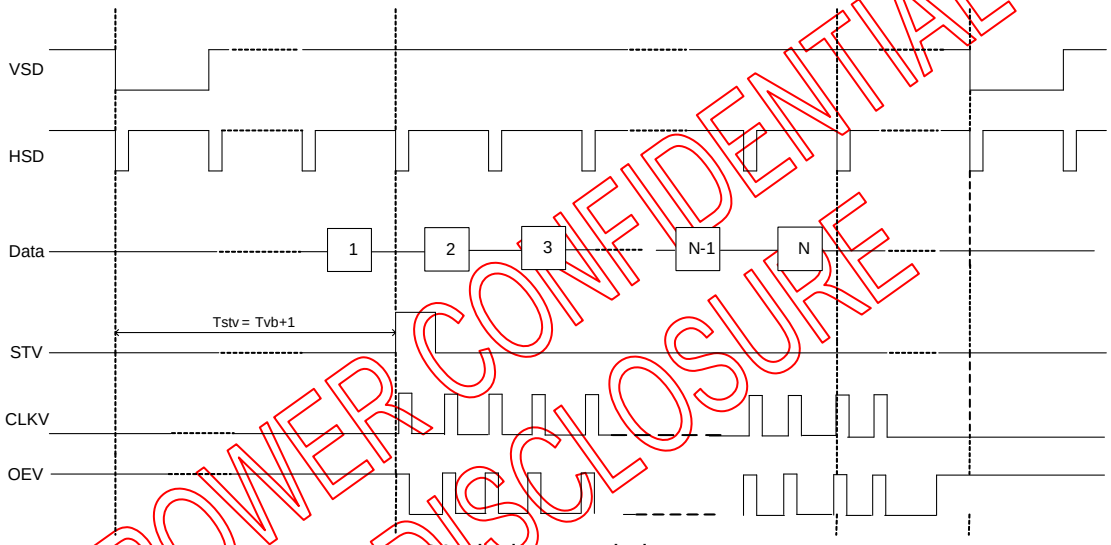
Horizontal timing



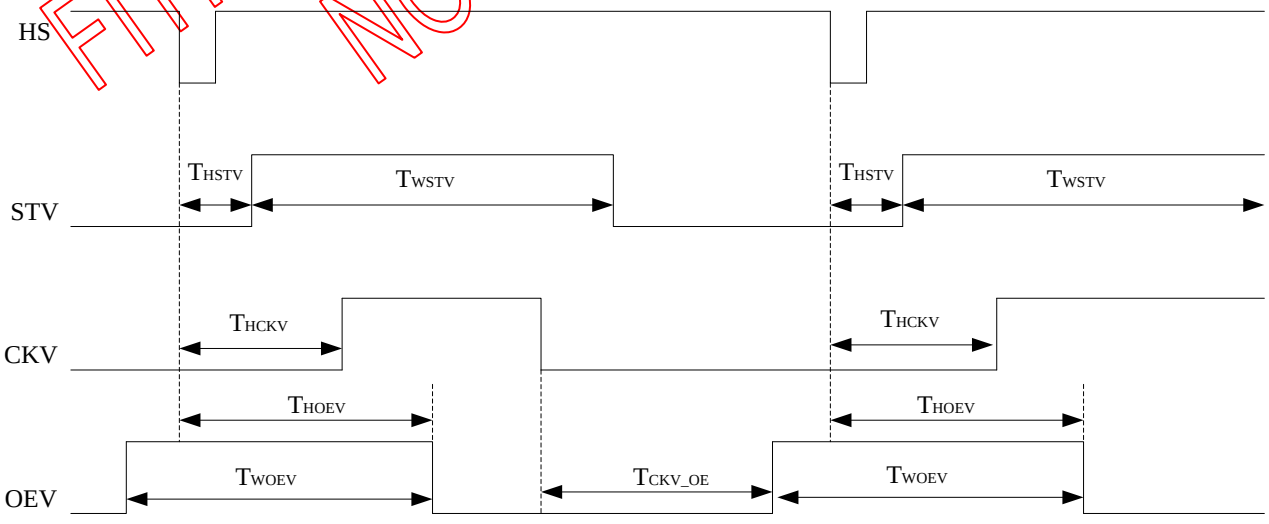
9.2 Gate Output Timing Table

(VDD=2.3 to 3.6V, VSS=VSSA=VSS_IF=0V, TA=-30 to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
STV Pulse Width	T_{WSTV}	-	1	-	H
Time from HSD to STV	T_{HSTV}	-	2	-	DCLK
Time from HSD to CKV	T_{HCKV}	-	25	-	DCLK
Time from HSD to OEV	T_{HOEV}	-	35	-	DCLK
Time from CKV to OEV	T_{CKV_OE}	-	168	-	DCLK
OEV Pulse Width	T_{WOEV}	-	188	-	DCLK



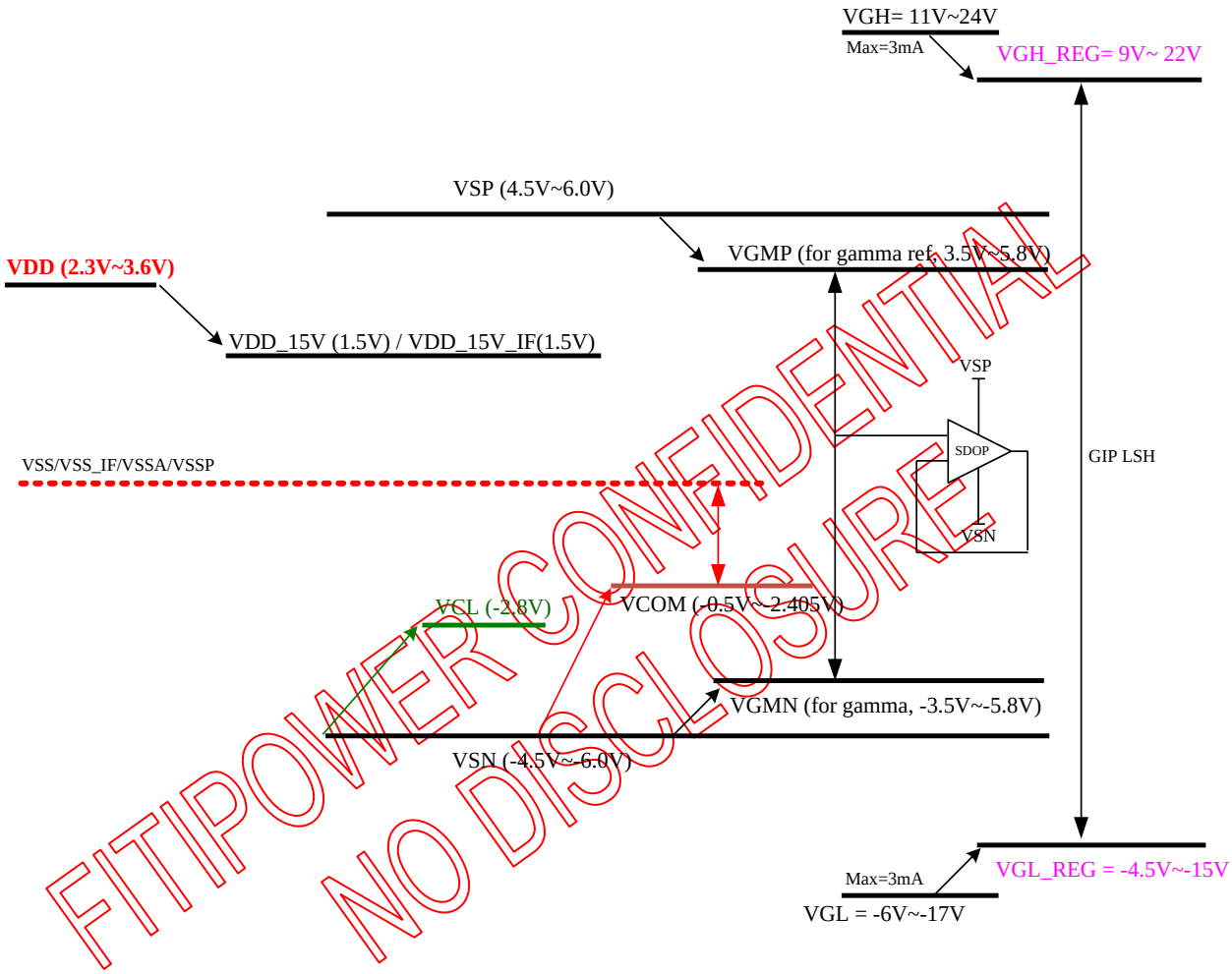
Vertical output timing



Gate output timing

10. Power Sequence and External Power Circuit

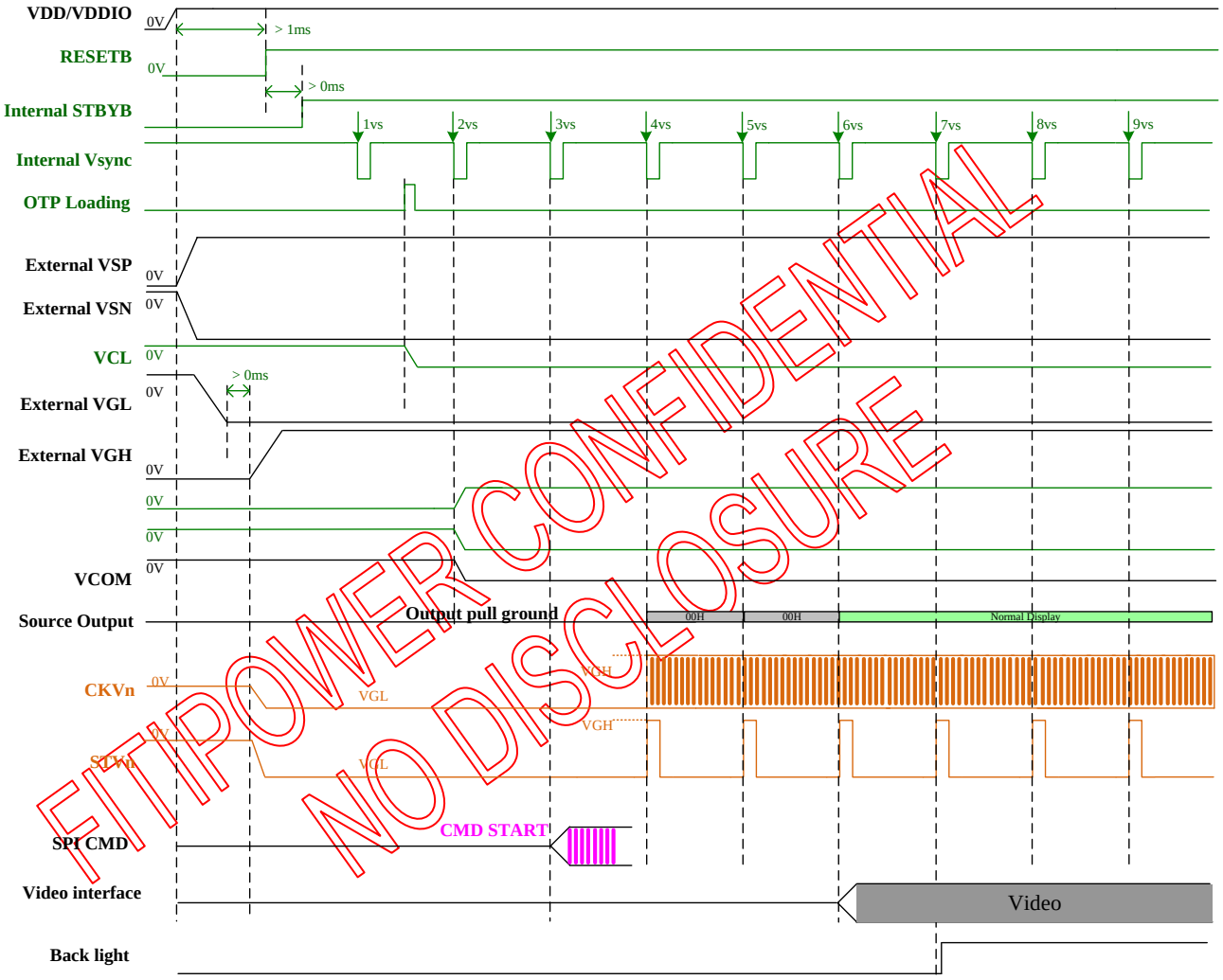
10.1 Power Generation



power generation

10.2 Power on sequence

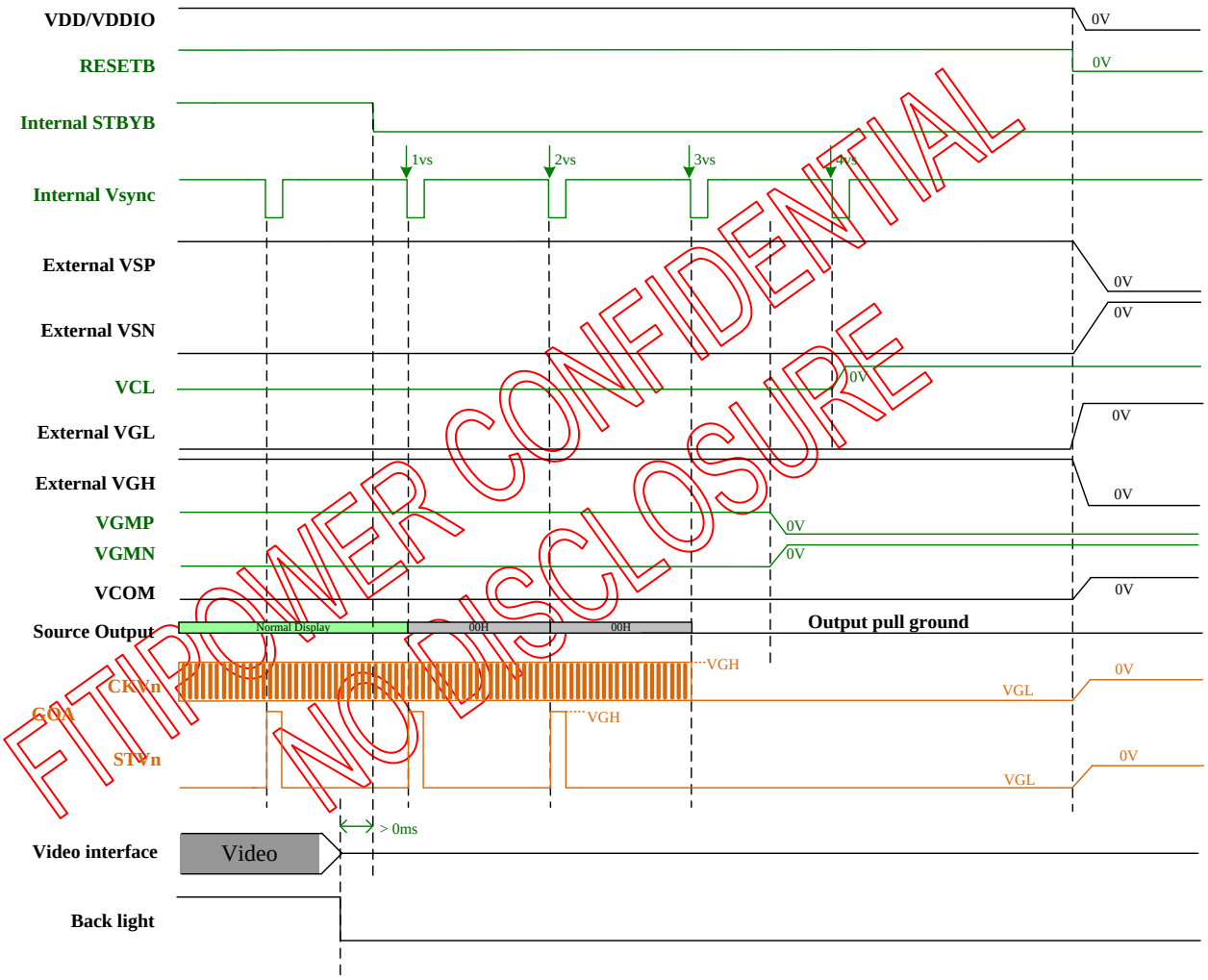
10.2.1 Power on sequence



Note: Before Power on process is have to check all power input of external that is Gnd.

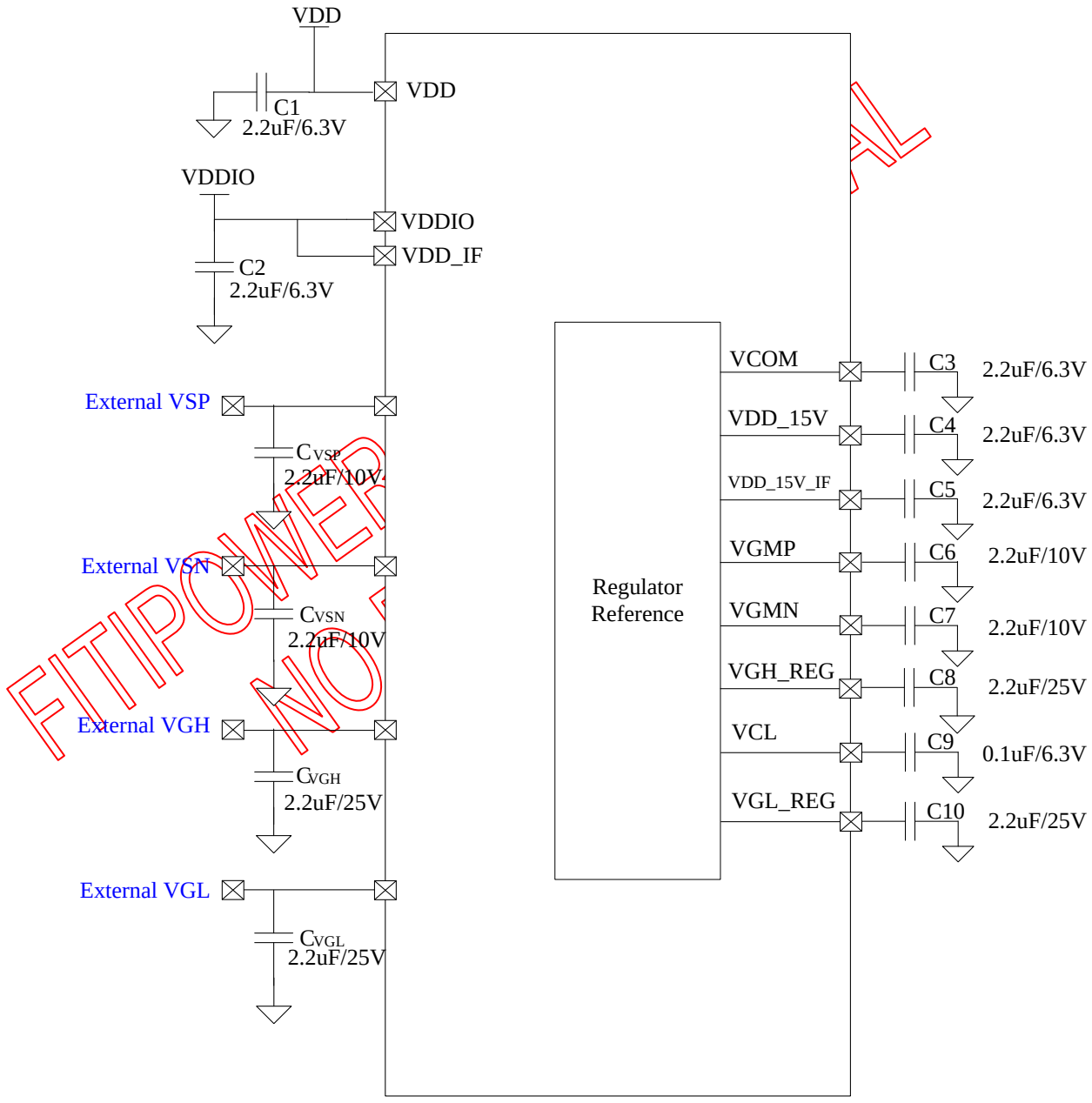
10.2.2 Power off sequence

External VSP/VSN
External VGH/VGL



10.3 Application power circuit

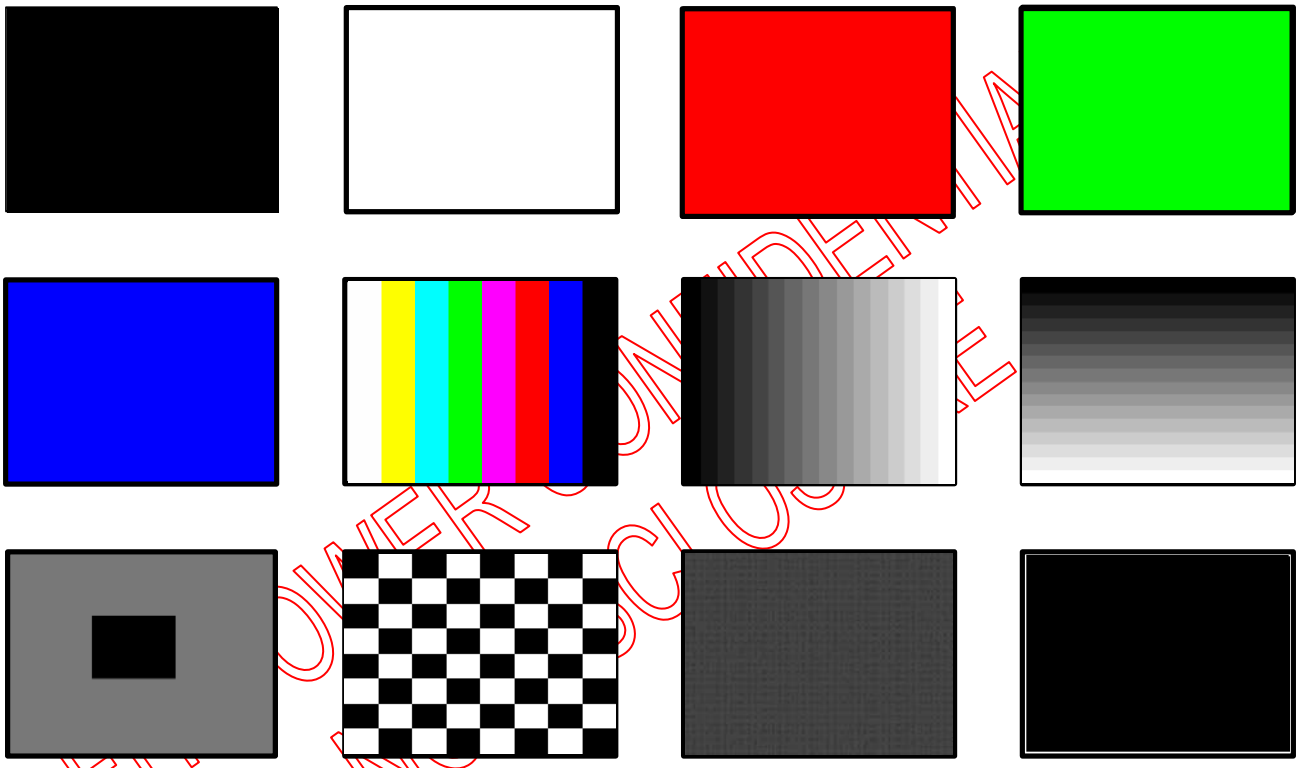
VDD=VDDIO=VDD_IF=2.3~3.6V, VSP=4.5~6.0V, VSN=-4.5~-6.0V.



11. Function Description

11.1 BIST pattern

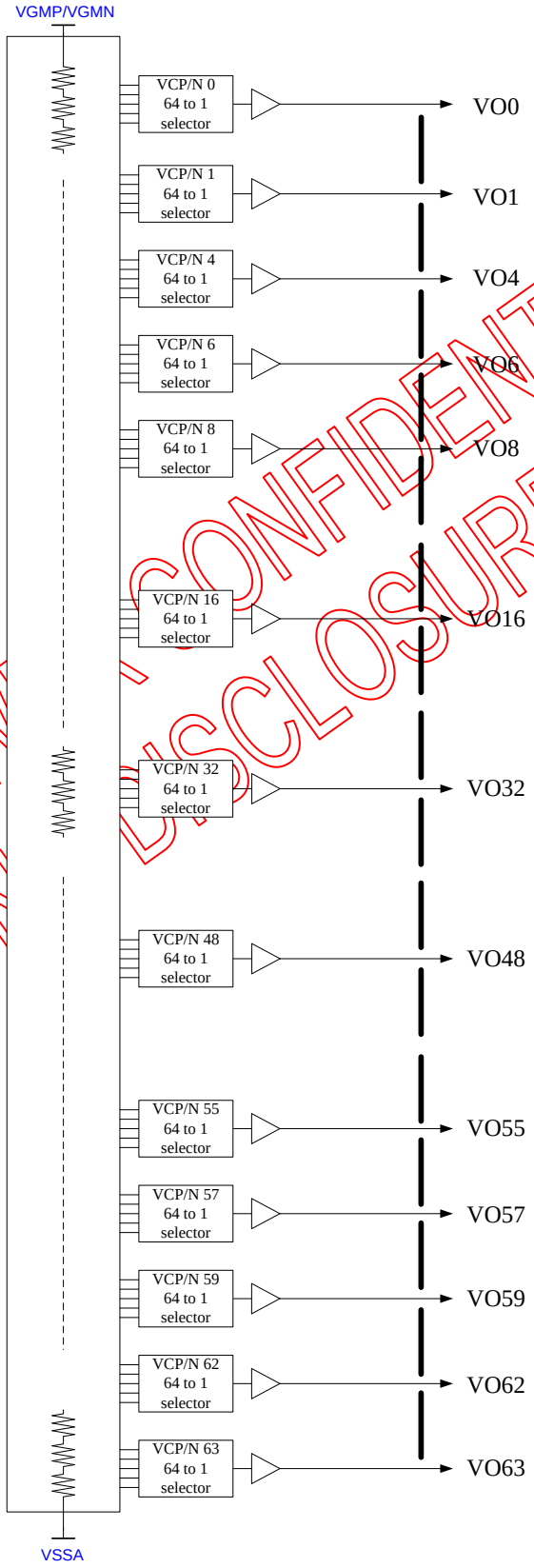
We support the BIST mode to test panel and debug. It can stop pattern at any time while BISTB set to low. The pattern sequence is listed below.



Black→White→R→G→B→Color Bar→Horizontal 256 gray scale→Vertical 256 gray scale→Crosstalk pattern→Chess board (L255/L0)→Flicker pattern→Black background with white out frame

12. Gamma Correction Resistances

We use the gamma resistor stream and 64-to-1 selector to adjust voltage

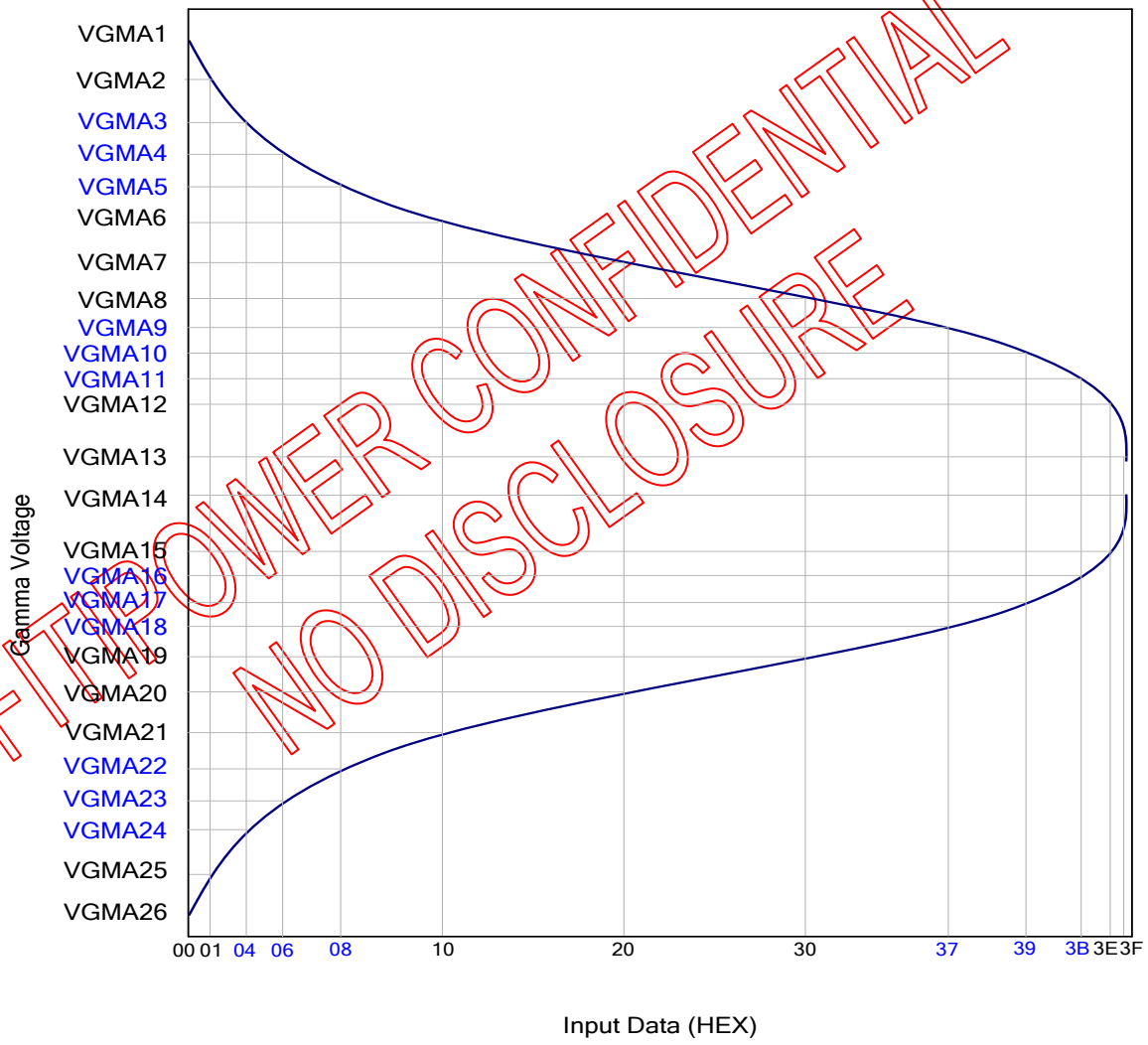


12.1 Relationship between input data and output voltage

The output voltage is determined by the 6-bit digital input data, POL and the 26 gamma corrected reference voltages. Among these gamma corrected reference voltages,VGMA1 ~VGMA13 and VGMA14 ~VGMA26 are for positive polarity voltage output and negative polarity voltage output respectively.

POL	OUT_{2n-1}	OUT_{2n}
H	VGMA14~VGMA26	VGMA1~VGMA13
L	VGMA1~VGMA13	VGMA14~VGMA26

GAMMA Corrected Characteristic Curve



Note:

VSP ≧ VGMP+0.2

VSN ≦ VGMN-0.2

VGMA13-0.2V ≧ GND ≧ VGMA14+0.2V

13. DC Characteristics

13.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
I/O voltage	VDDIO	-0.5	-	4	V	-
Interface supply power	VDD_IF	-0.5	-	4		
Power input	VDD	-0.5	-	4	V	-
VSP supply power	VSP	-0.5	-	6.6	V	-
VSN supply power	VSN	-6.6	-	0.3	V	-
VGH supply power	VGH	-0.5	-	VGL_GIP+32	V	-
VGL supply power	VGL	-17	-	0.3	V	-
Operating temperature	Top	-30	-	85	℃	(1)
Storage temperature	Tstg	-55	-	125	℃	-

Note : 1) Do not let condensation for low temperature

Table 10.1: Absolute maximum rating

13.2 Typical operating condition

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
VDD voltage	VDD	-	3.3	-	V	Analog supply voltage
VDDIO voltage	VDDIO	-	3.3	-	V	I/O Power supply voltage
VSP voltage	VSP	4.5	5.0	6	V	VSP voltage
VSN voltage	VSN	-6	-5.0	-4.5	V	VSN voltage
VGH voltage	VGH	11	18	24	V	VGH voltage
VGL voltage	VGL	-17	-12	-6	V	VGL_ voltage
VGL_REG voltage	VGL_REG	-15	-10	-4.5	V	VGL_REG voltage

Table 10.2: Typical operating conditions

13.3 DC electrical characteristics

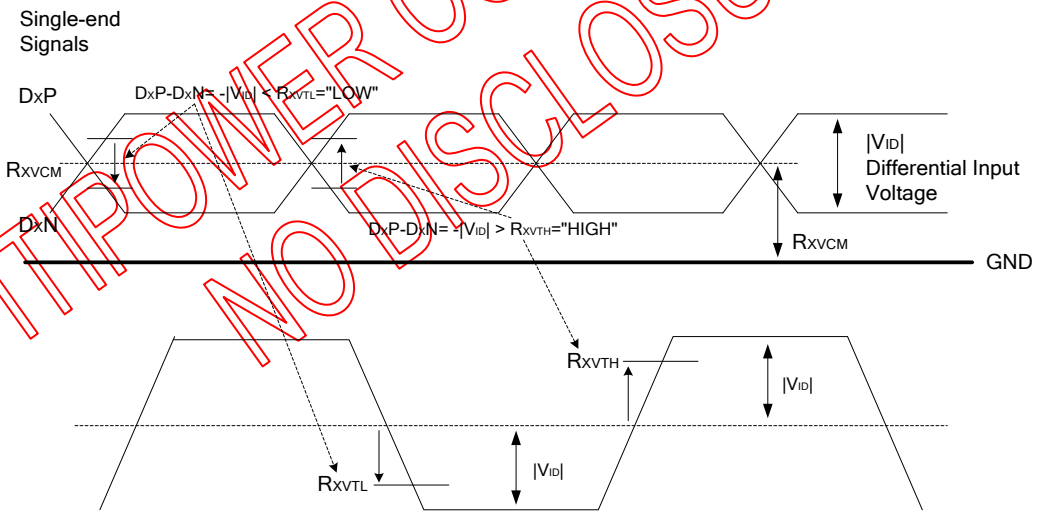
(Test condition: VDD=VDDIO=VDDIF=2.3~3.6V, TA=-30℃~+85℃,VSS=VSSA=0V)

Parameter		Symbol	Spec.			Unit	Note
			Min.	Typ.	Max.		
Input high level voltage		VIH	0.8 x VDDIO		VDDIO	V	
Input low level voltage		VIL	VSS		0.2 x VDDIO	V	
Input Leakage Current		Ileak	(-1)		(+1)	μA	
Output high level voltage		VOH	0.8 x VDDIO		VDDIO	V	
Output low level voltage		VOL	VSS		0.2 x VDDIO	V	
VGH_REG output voltage		VGH_REG	9	16	22	V	
VGL_REG output voltage		VGL_REG	-15	-10	-4.5		
VGMP output voltage		VGMP	3.5	4.24	5.8	V	
VGMN output voltage		VGMN	-5.8	-4.64	-3.5	V	
VGL output voltage		VGL	-17	-12	-6	V	
VGH output voltage		VGH	11	18	24	V	
VCL output voltage		VCL	-3	-2.8	-2.1	V	
VCOM output voltage		VCOM	-2.405	-1.5	-0.5	V	
Input terminal resistance		ZID		100		ohm	
Source output level deviation	Graycode = 0 ~ 14 Graycode = 241 ~ 255			TBD		mV	
	Graycode = 15 ~ 31 Graycode = 208 ~ 240			TBD		mV	
	Graycode = 32 ~ 207			TBD		mV	
Source output offset deviation	Graycode = 0 ~ 14 Graycode = 241 ~ 255	-		TBD		mV	
	Graycode = 15 ~ 31 Graycode = 208 ~ 240	-		TBD		mV	
	Graycode = 32 ~ 207	-		TBD		mV	
Current consumption	Analog Operating	IAOP		TBD		mA	
	Analog Stand-by	IAST		TBD		mA	
Rush current		Ivddpeak		TBD		mA	

13.4 LVDS DC electrical characteristics

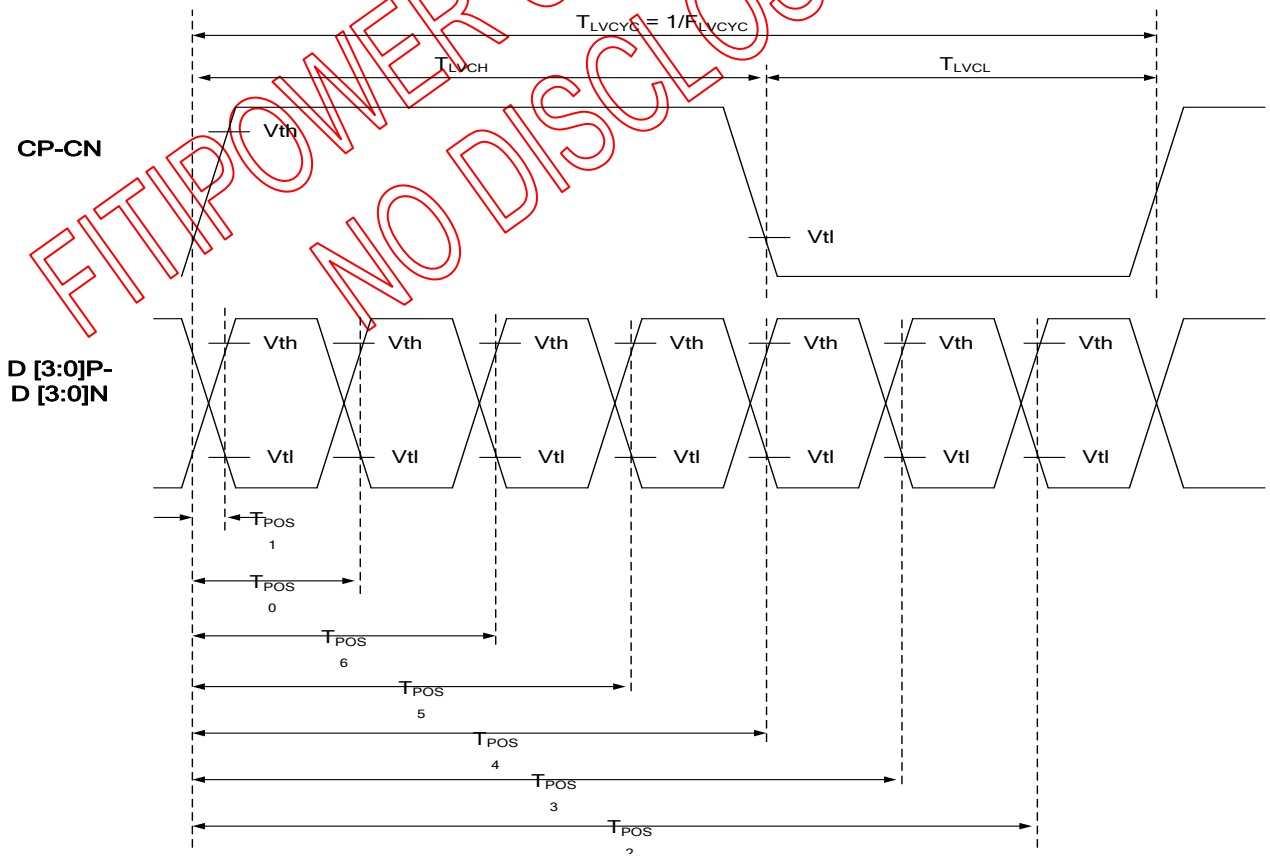
(VDD=VDDIO=VDDIF=2.3 to 3.6V, VSS=VSSA=VSS_IF=0V, TA=-30 to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential input high threshold voltage	R_{XVTH}	-	-	+0.1	V	R_{XVCM}=1.2V
Differential input low threshold voltage	R_{XVTL}	-0.1	-	-	V	
Input voltage range (singled-end)	R_{XVIN}	0.7	-	1.7	V	
Differential input common mode voltage	R_{XVCM}	1	1.2	1.4	V	$\|V_{ID}\|$=0.2
Differential input impedance	Z_{ID}	80	100	125	ohm	
Differential input voltage	$\|V_{ID}\|$	0.2	-	0.6	V	
Differential input leakage current	I_{LCLVDS}	-10	-	+10	uA	
LVDS Digital Operating Current	I_{VDD}	-	15	20	mA	F_{DCLK}=80MHz,VDD=3.3V, Input pattern: 55h->Aah->55h->Aah
LVDS Digital Stand-by Current	I_{ST}	-	-	250	uA	Clock & all Functions are stopped



LVDS signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	F_{LVCYC}	69.7		80.9	MHz
Clock period	T_{LVCYC}			-	ps
1 data bit time	UI	-	1/7	-	T_{LVCYC}
Clock high time	T_{LVCH}	3.9	4	4.1	UI
Clock low time	T_{LVCL}	2.9	3	3.1	UI
Position 1	T_{POS1}	-0.2	0	0.2	UI
Position 0	T_{POS0}	0.8	1	1.2	UI
Position 6	T_{POS6}	1.8	2	2.2	UI
Position 5	T_{POS5}	2.8	3	3.2	UI
Position 4	T_{POS4}	3.8	4	4.2	UI
Position 3	T_{POS3}	4.8	5	5.2	UI
Position 2	T_{POS2}	5.8	6	6.2	UI
Input eye width	T_{EYEW}	0.6		-	UI
Input eye border	T_{EX}	-	-	0.2	UI
LVDS wake up time	T_{ENLVDS}	-	-	150	us



14. AC Characteristics

14.1 LVDS mode AC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Clock frequency	R_{xFCLK}	30	-	TBD	MHz	Refer to input timing table for each display resolution
Input data skew margin	T_{RSKM}	500	-	-	ps	|VID| = 200mV RxVCM = 1.2V RxFCLK = 81MHz
Clock high time	T_{LVCH}	-	4/(7* R_{xFCLK})	-	ns	
Clock low time	T_{LVCL}	-	3/(7* R_{xFCLK})	-	ns	
PLL wake-up time	T_{enPLL}	-	-	150	us	

Table 13.1: LVDS mode AC electrical characteristics

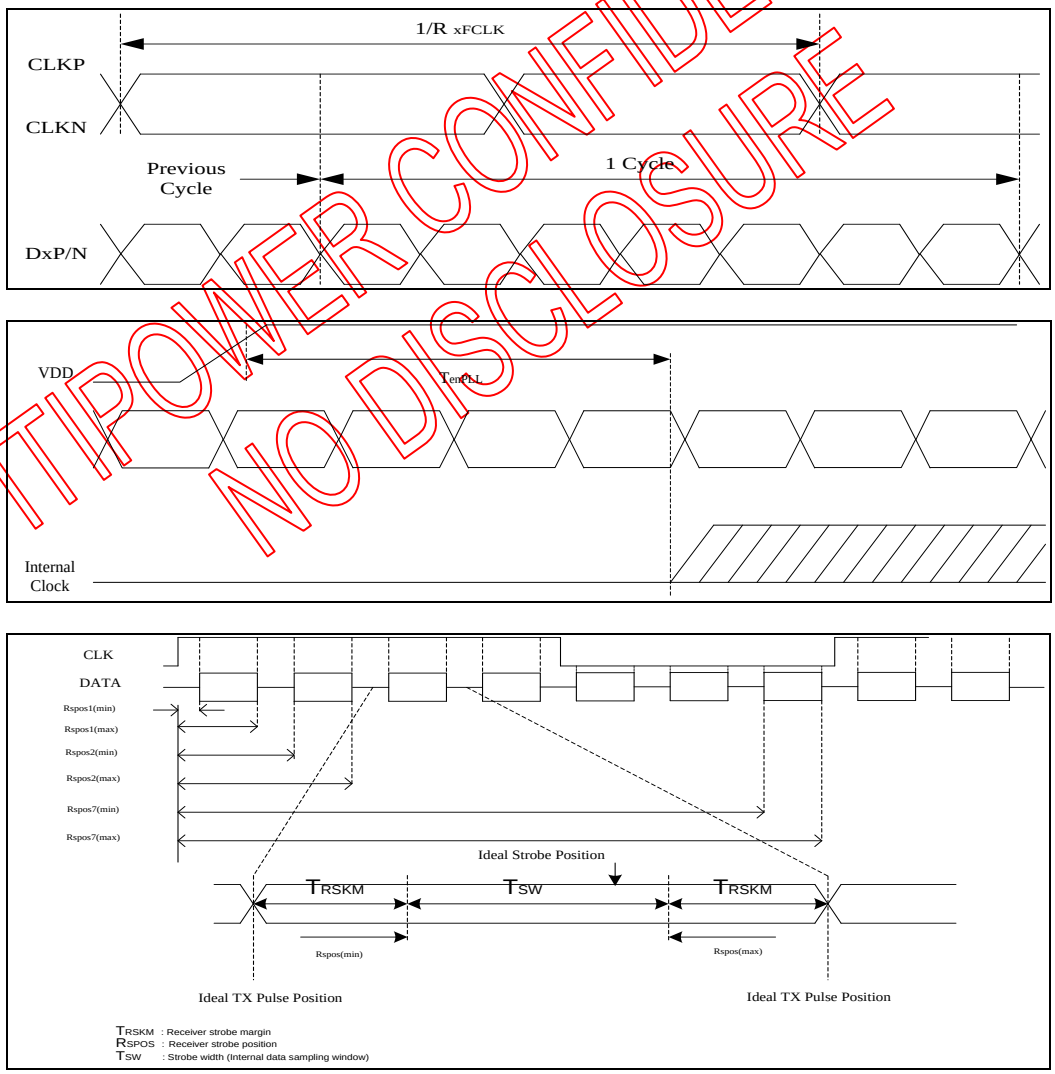
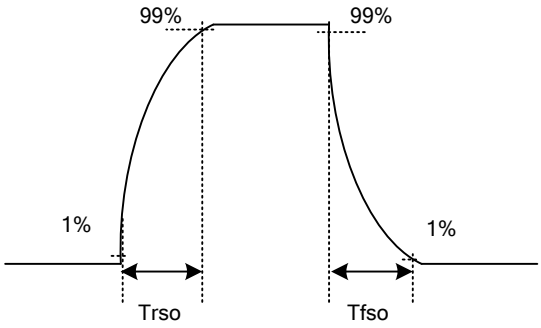
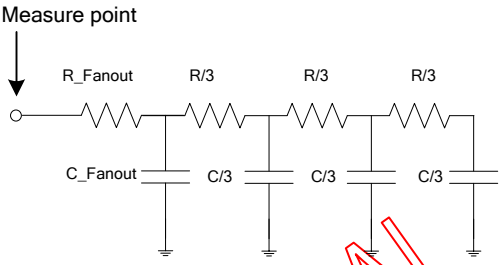


Figure 13.3: LVDS figure

14.2 Source output timing (SOUT0 ~ SOUT2051)



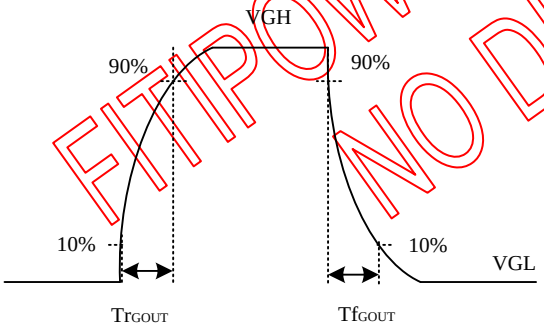


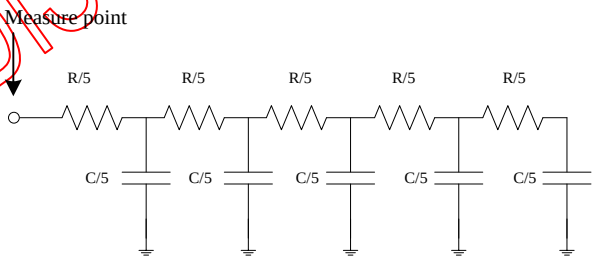
Rdata_total = 25.072k(ohm)
Cdata_total = 83 pF

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Source driver rising time	Trso			3.52		µs
Source driver falling time	Tfso			2.8		µs

Table 13.2: Source output timing

Panel control signal output (GOUTL[1]~GOUTL[22] , GOUTR[1]~GOUTR[22])





Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Panel control signal rising time	T_{rGOUT}	TBD	-	-	TBD	µs
Panel control signal falling time	T_{fGOUT}	TBD	-	-	TBD	µs

Table 13.3: GOA output timing

14.3 Serial interface characteristics

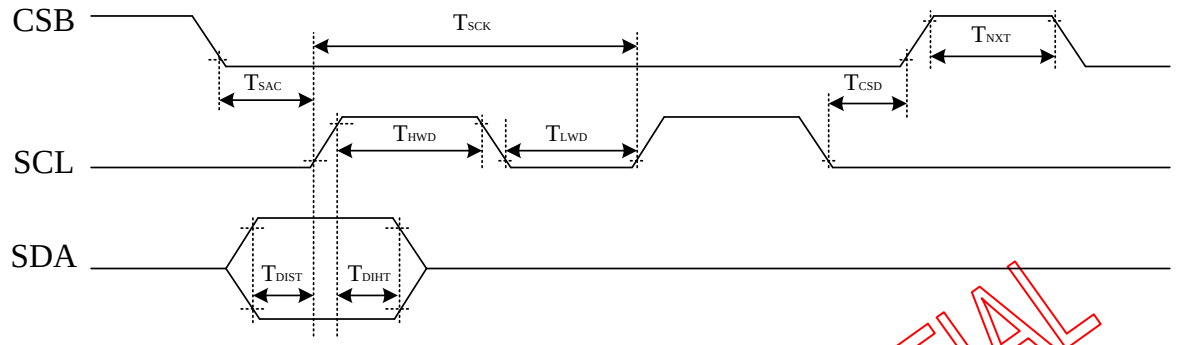
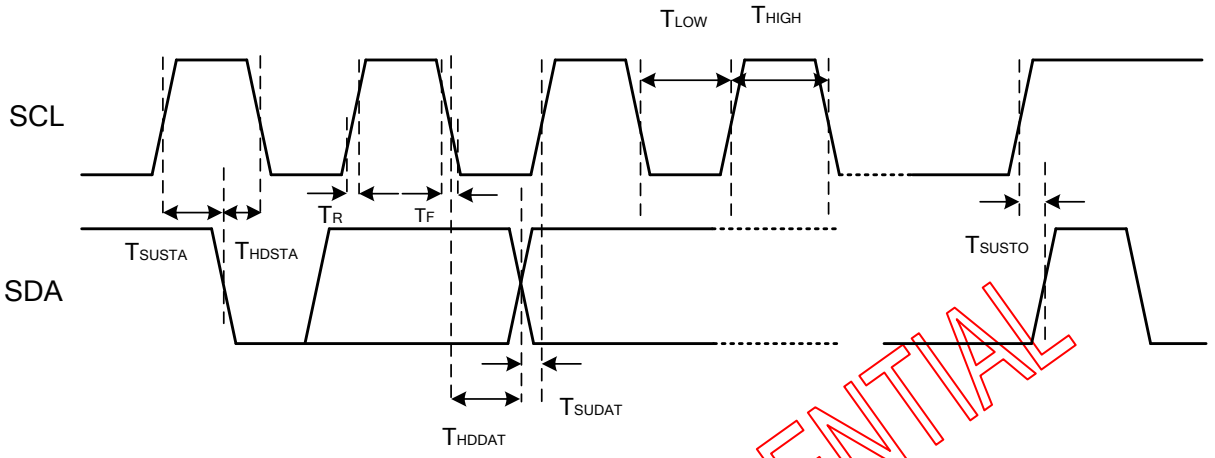


Figure 13.4: Serial interface characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
CSB assertion to first clock edge	T_{SAC}		120	-	-	ns
CSB de-assertion from last clock edge	T_{CSD}		120	-	-	ns
CSB next control enable	T_E		200	-	-	ns
SCL period time	T_{SCK}		200	-	-	ns
SCL high period time	T_{HWD}		100	-	-	ns
SCL low period time	T_{LWD}		100	-	-	ns
SDA input data setup time	T_{DIST}		50	-	-	ns
SDA input data hold time	T_{DIHT}		50	-	-	ns



Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
SCL clock frequency	f_{SCL}		-	-	400	kHz
STOP setup time	T_{SUSTO}		0.60	-	-	uS
START setup time	T_{SUSTA}		0.60	-	-	uS
START hold time	T_{HDSTA}		0.60	-	-	uS
SCL clock pulse width low	T_{LOW}		1.20	-	-	uS
SCL clock pulse width high	T_{HIGH}		0.60	-	-	uS
Data hold time	T_{HDDAT}		0	-	-	uS
Data setup time	T_{SUDAT}		100	-	-	nS
IIC bus rise time	T_R		-	-	300	nS
IIC bus fall time	T_F	Output clock duty	-	-	300	nS

14.4 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(Test condition: VDDIO=2.3V~3.6V, VSS=0V, T_A=-30 ~+85)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
Reset low pulse width	Trst		20	-	-	μs

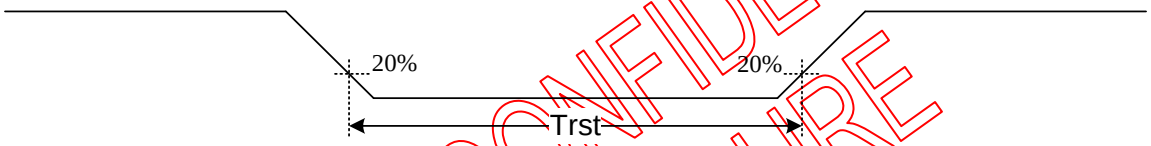
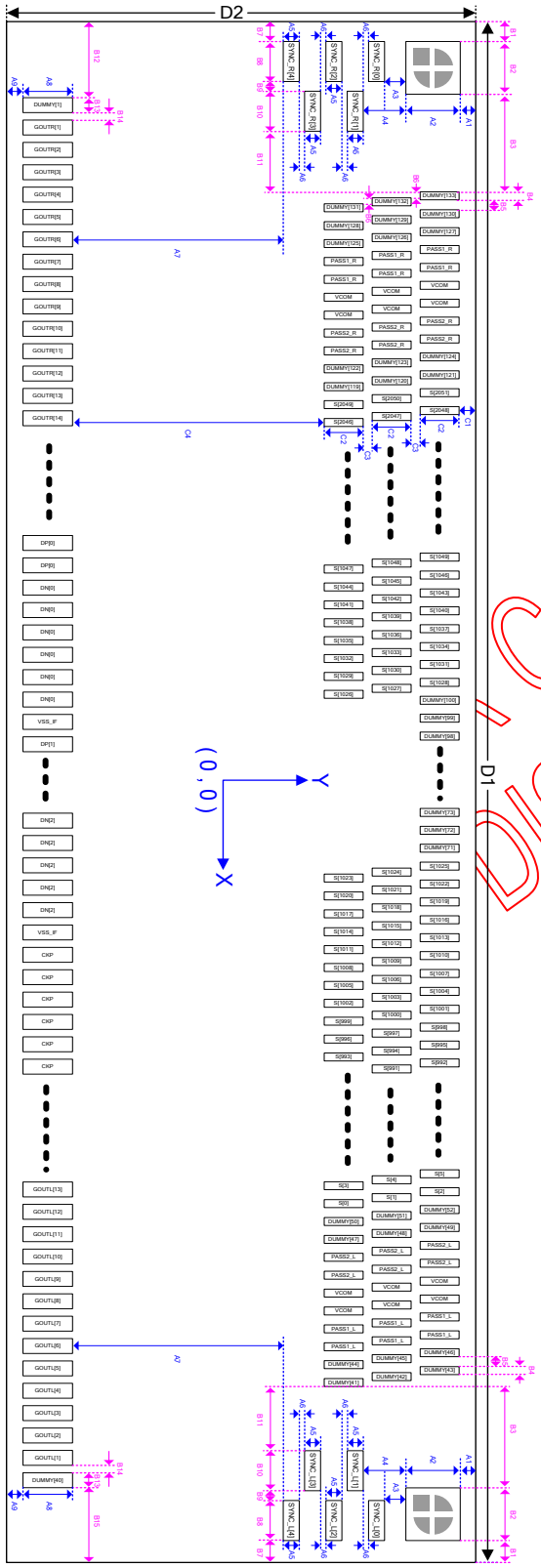
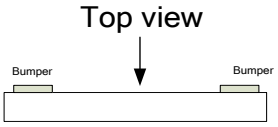


Figure 13.5: Reset timing

15.Chip Outline Dimension





Symbol	Dimension
A1	50
A2	100
A3	31
A4	71
A5	30
A6	10
A7	395
A8	93
A9	41

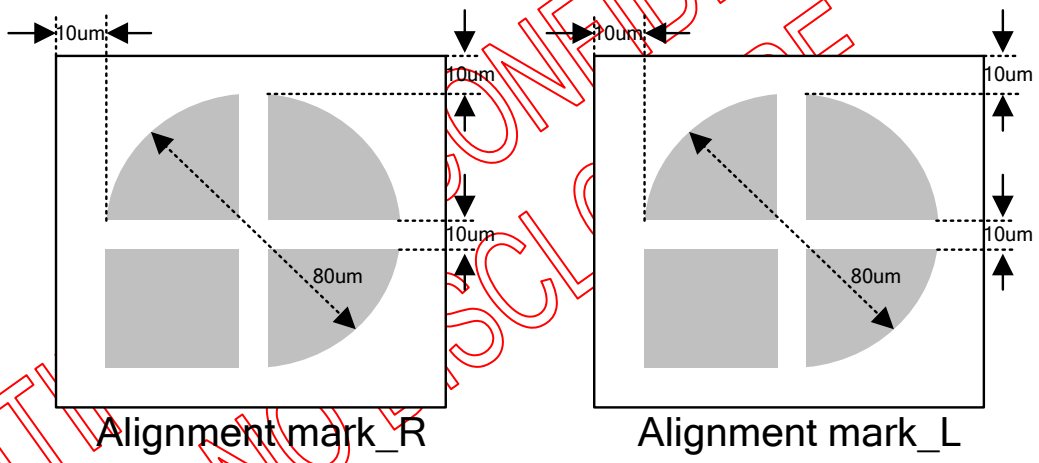
Symbol	Dimension
B1	50
B2	100
B3	202
B4	16
B5	20
B6	12
B7	50
B8	80
B9	20

Symbol	Dimension
B10	80
B11	122
B12	162
B13	30
B14	15
B15	163
-	-
-	-
-	-

Symbol	Dimension
C1	41
C2	73
C3	17
C4	472
D1	27600
D2	900
-	-
-	-
-	-

Unit : um
Bump High=9um
Die size with ScribeLine

15.1 Alignment mark



ALM	X – axis	Y – axis
A_MARK_R	-13700	350
A_MARK_L	13700	350

15.2 Pad Coordinate

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1	SYNC_R[0]	-13710	254	58	VGH	-11272.5	-362.5	115	TP[15]	-8707.5	-362.5
2	SYNC_R[1]	-13610	214	59	VGH	-11227.5	-362.5	116	TP[16]	-8662.5	-362.5
3	SYNC_R[2]	-13710	174	60	T_S[1996]	-11182.5	-362.5	117	TP[17]	-8617.5	-362.5
4	SYNC_R[3]	-13610	134	61	T_S[1995]	-11137.5	-362.5	118	CAS	-8572.5	-362.5
5	SYNC_R[4]	-13710	94	62	VGH_REG	-11092.5	-362.5	119	VSS	-8527.5	-362.5
6	DUMMY[1]	-13622.5	-362.5	63	VGH_REG	-11047.5	-362.5	120	SDLOC	-8482.5	-362.5
7	GOUTR[1]	-13577.5	-362.5	64	VGH_REG	-11002.5	-362.5	121	SDLOC	-8437.5	-362.5
8	GOUTR[2]	-13532.5	-362.5	65	VGH_REG	-10957.5	-362.5	122	ZIGZAG	-8392.5	-362.5
9	GOUTR[3]	-13487.5	-362.5	66	VGH_REG	-10912.5	-362.5	123	ZIGZAG	-8347.5	-362.5
10	GOUTR[4]	-13442.5	-362.5	67	VSN	-10867.5	-362.5	124	ZTYPE	-8302.5	-362.5
11	GOUTR[5]	-13397.5	-362.5	68	VSN	-10822.5	-362.5	125	ZTYPE	-8257.5	-362.5
12	GOUTR[6]	-13352.5	-362.5	69	VSN	-10777.5	-362.5	126	TP[18]	-8212.5	-362.5
13	GOUTR[7]	-13307.5	-362.5	70	VSN	-10732.5	-362.5	127	TP[19]	-8167.5	-362.5
14	GOUTR[8]	-13262.5	-362.5	71	VSN	-10687.5	-362.5	128	TP[20]	-8122.5	-362.5
15	GOUTR[9]	-13217.5	-362.5	72	VSN	-10642.5	-362.5	129	TP[21]	-8077.5	-362.5
16	GOUTR[10]	-13172.5	-362.5	73	VSN	-10597.5	-362.5	130	TP[22]	-8032.5	-362.5
17	GOUTR[11]	-13127.5	-362.5	74	VSP	-10552.5	-362.5	131	TP[23]	-7987.5	-362.5
18	GOUTR[12]	-13082.5	-362.5	75	VSP	-10507.5	-362.5	132	TP[24]	-7942.5	-362.5
19	GOUTR[13]	-13037.5	-362.5	76	VSP	-10462.5	-362.5	133	TP[25]	-7897.5	-362.5
20	GOUTR[14]	-12992.5	-362.5	77	VSP	-10417.5	-362.5	134	TP[26]	-7852.5	-362.5
21	GOUTR[15]	-12947.5	-362.5	78	VSP	-10372.5	-362.5	135	TP[27]	-7807.5	-362.5
22	GOUTR[16]	-12902.5	-362.5	79	VSP	-10327.5	-362.5	136	TP[28]	-7762.5	-362.5
23	GOUTR[17]	-12857.5	-362.5	80	VSP	-10282.5	-362.5	137	TP[29]	-7717.5	-362.5
24	GOUTR[18]	-12812.5	-362.5	81	VSSA	-10237.5	-362.5	138	TP[30]	-7672.5	-362.5
25	GOUTR[19]	-12767.5	-362.5	82	VSSA	-10192.5	-362.5	139	TP[31]	-7627.5	-362.5
26	GOUTR[20]	-12722.5	-362.5	83	VSSA	-10147.5	-362.5	140	TP[32]	-7582.5	-362.5
27	GOUTR[21]	-12677.5	-362.5	84	VSSA	-10102.5	-362.5	141	TP[33]	-7537.5	-362.5
28	GOUTR[22]	-12632.5	-362.5	85	VSSA	-10057.5	-362.5	142	TP[34]	-7492.5	-362.5
29	PASS1_R	-12587.5	-362.5	86	VSSA	-10012.5	-362.5	143	TP[35]	-7447.5	-362.5
30	PASS1_R	-12542.5	-362.5	87	VSSA	-9967.5	-362.5	144	TP[36]	-7402.5	-362.5
31	PASS1_R	-12497.5	-362.5	88	VSSA	-9922.5	-362.5	145	TP[37]	-7357.5	-362.5
32	VCOM	-12442.5	-362.5	89	VSS	-9877.5	-362.5	146	TP[38]	-7312.5	-362.5
33	VCOM	-12397.5	-362.5	90	VSS	-9832.5	-362.5	147	TP[39]	-7267.5	-362.5
34	VCOM	-12352.5	-362.5	91	VSS	-9787.5	-362.5	148	TP[40]	-7222.5	-362.5
35	VCOM	-12307.5	-362.5	92	VSS	-9742.5	-362.5	149	TP[41]	-7177.5	-362.5
36	PASS2_R	-12262.5	-362.5	93	VSS	-9697.5	-362.5	150	TP[42]	-7132.5	-362.5
37	PASS2_R	-12217.5	-362.5	94	VSS	-9652.5	-362.5	151	RESETB	-7087.5	-362.5
38	PASS2_R	-12172.5	-362.5	95	VSS	-9607.5	-362.5	152	RESETB	-7042.5	-362.5
39	VGL	-12127.5	-362.5	96	VSS	-9562.5	-362.5	153	RESETB	-6997.5	-362.5
40	VGL	-12082.5	-362.5	97	VDD_15V	-9517.5	-362.5	154	RESETB	-6952.5	-362.5
41	VGL	-12037.5	-362.5	98	VDD_15V	-9472.5	-362.5	155	LNSW[1]	-6907.5	-362.5
42	VGL	-11992.5	-362.5	99	VDD_15V	-9427.5	-362.5	156	LNSW[1]	-6862.5	-362.5
43	VGL	-11947.5	-362.5	100	TP[0]	-9382.5	-362.5	157	LNSW[0]	-6817.5	-362.5
44	VGL	-11902.5	-362.5	101	TP[1]	-9337.5	-362.5	158	LNSW[0]	-6772.5	-362.5
45	VGL	-11857.5	-362.5	102	TP[2]	-9292.5	-362.5	159	PNSW	-6727.5	-362.5
46	VGL_REG	-11812.5	-362.5	103	TP[3]	-9247.5	-362.5	160	PNSW	-6682.5	-362.5
47	VGL_REG	-11767.5	-362.5	104	TP[4]	-9202.5	-362.5	161	IFSEL[1]	-6637.5	-362.5
48	VGL_REG	-11722.5	-362.5	105	TP[5]	-9157.5	-362.5	162	IFSEL[1]	-6592.5	-362.5
49	VGL_REG	-11677.5	-362.5	106	TP[6]	-9112.5	-362.5	163	IFSEL[0]	-6547.5	-362.5
50	VGL_REG	-11632.5	-362.5	107	TP[7]	-9067.5	-362.5	164	IFSEL[0]	-6502.5	-362.5
51	VGL_REG	-11587.5	-362.5	108	TP[8]	-9022.5	-362.5	165	RES[2]	-6457.5	-362.5
52	VGL_REG	-11542.5	-362.5	109	TP[9]	-8977.5	-362.5	166	VSS	-6412.5	-362.5
53	VGH	-11497.5	-362.5	110	TP[10]	-8932.5	-362.5	167	RES[1]	-6367.5	-362.5
54	VGH	-11452.5	-362.5	111	TP[11]	-8887.5	-362.5	168	VSS	-6322.5	-362.5
55	VGH	-11407.5	-362.5	112	TP[12]	-8842.5	-362.5	169	RES[0]	-6277.5	-362.5
56	VGH	-11362.5	-362.5	113	TP[13]	-8797.5	-362.5	170	VSS	-6232.5	-362.5

57	VGH	-11317.5	-362.5	114	TP[14]	-8752.5	-362.5	171	GATE_SW[1]	-6187.5	-362.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
172	GATE_SW[1]	-6142.5	-362.5	229	VDD	-3577.5	-362.5	286	DP[0]	-1012.5	-362.5
173	GATE_SW[0]	-6097.5	-362.5	230	VDD	-3532.5	-362.5	287	DP[0]	-967.5	-362.5
174	GATE_SW[0]	-6052.5	-362.5	231	VDD	-3487.5	-362.5	288	DP[0]	-922.5	-362.5
175	OP_DRV[1]	-6007.5	-362.5	232	VCL	-3442.5	-362.5	289	DP[0]	-877.5	-362.5
176	OP_DRV[1]	-5962.5	-362.5	233	VCL	-3397.5	-362.5	290	DP[0]	-832.5	-362.5
177	OP_DRV[0]	-5917.5	-362.5	234	VCL	-3352.5	-362.5	291	DP[0]	-787.5	-362.5
178	OP_DRV[0]	-5872.5	-362.5	235	VCL	-3307.5	-362.5	292	DN[0]	-742.5	-362.5
179	GIP_LRSEL[1]	-5827.5	-362.5	236	VCL	-3262.5	-362.5	293	DN[0]	-697.5	-362.5
180	VSS	-5782.5	-362.5	237	VSN	-3217.5	-362.5	294	DN[0]	-652.5	-362.5
181	GIP_LRSEL[0]	-5737.5	-362.5	238	VSN	-3172.5	-362.5	295	DN[0]	-607.5	-362.5
182	VSS	-5692.5	-362.5	239	VSN	-3127.5	-362.5	296	DN[0]	-562.5	-362.5
183	DVCOM_EN	-5647.5	-362.5	240	VSN	-3082.5	-362.5	297	DN[0]	-517.5	-362.5
184	DVCOM_EN	-5602.5	-362.5	241	VSN	-3037.5	-362.5	298	VSS_IF	-472.5	-362.5
185	DITHER_EN	-5557.5	-362.5	242	VSN	-2992.5	-362.5	299	DP[1]	-427.5	-362.5
186	DITHER_EN	-5512.5	-362.5	243	VSN	-2947.5	-362.5	300	DP[1]	-382.5	-362.5
187	HFRC_EN	-5467.5	-362.5	244	VSN	-2902.5	-362.5	301	DP[1]	-337.5	-362.5
188	HFRC_EN	-5422.5	-362.5	245	VSP	-2857.5	-362.5	302	DP[1]	-292.5	-362.5
189	STBYB	-5377.5	-362.5	246	VSP	-2812.5	-362.5	303	DP[1]	-247.5	-362.5
190	STBYB	-5332.5	-362.5	247	VSP	-2767.5	-362.5	304	DP[1]	-202.5	-362.5
191	BISTB	-5287.5	-362.5	248	VSP	-2722.5	-362.5	305	DN[1]	-157.5	-362.5
192	BISTB	-5242.5	-362.5	249	VSP	-2677.5	-362.5	306	DN[1]	-112.5	-362.5
193	CMD_SEL	-5197.5	-362.5	250	VSP	-2632.5	-362.5	307	DN[1]	-67.5	-362.5
194	CMD_SEL	-5152.5	-362.5	251	VSP	-2587.5	-362.5	308	DN[1]	-22.5	-362.5
195	LVFMT	-5107.5	-362.5	252	VSSA	-2542.5	-362.5	309	DN[1]	22.5	-362.5
196	LVFMT	-5062.5	-362.5	253	VSSA	-2497.5	-362.5	310	DN[1]	67.5	-362.5
197	LVBIT	-5017.5	-362.5	254	VSSA	-2452.5	-362.5	311	VSS_IF	112.5	-362.5
198	LVBIT	-4972.5	-362.5	255	VSSA	-2407.5	-362.5	312	CKP	157.5	-362.5
199	SDA	-4927.5	-362.5	256	VSSA	-2362.5	-362.5	313	CKP	202.5	-362.5
200	SDA	-4882.5	-362.5	257	VSSA	-2317.5	-362.5	314	CKP	247.5	-362.5
201	SCL	-4837.5	-362.5	258	VSSA	-2272.5	-362.5	315	CKP	292.5	-362.5
202	SCL	-4792.5	-362.5	259	VGMP	-2227.5	-362.5	316	CKP	337.5	-362.5
203	CSB	-4747.5	-362.5	260	VGMP	-2182.5	-362.5	317	CKP	382.5	-362.5
204	CSB	-4702.5	-362.5	261	VGMP	-2137.5	-362.5	318	CKN	427.5	-362.5
205	FRAME	-4657.5	-362.5	262	VGMP	-2092.5	-362.5	319	CKN	472.5	-362.5
206	FRAME	-4612.5	-362.5	263	VGMP	-2047.5	-362.5	320	CKN	517.5	-362.5
207	DUMMY[2]	-4567.5	-362.5	264	VGMP	-2002.5	-362.5	321	CKN	562.5	-362.5
208	T_VTSEN[2]	-4522.5	-362.5	265	VGMN	-1957.5	-362.5	322	CKN	607.5	-362.5
209	T_VTSEN[1]	-4477.5	-362.5	266	VGMN	-1912.5	-362.5	323	CKN	652.5	-362.5
210	T_VTSEN[0]	-4432.5	-362.5	267	VGMN	-1867.5	-362.5	324	VSS_IF	697.5	-362.5
211	LEDON	-4387.5	-362.5	268	VGMN	-1822.5	-362.5	325	DP[2]	742.5	-362.5
212	LEDON	-4342.5	-362.5	269	VGMN	-1777.5	-362.5	326	DP[2]	787.5	-362.5
213	LEDPWM	-4297.5	-362.5	270	VGMN	-1732.5	-362.5	327	DP[2]	832.5	-362.5
214	LEDPWM	-4252.5	-362.5	271	DUMMY[4]	-1687.5	-362.5	328	DP[2]	877.5	-362.5
215	PWR_EN	-4207.5	-362.5	272	DUMMY[5]	-1642.5	-362.5	329	DP[2]	922.5	-362.5
216	PWR_EN	-4162.5	-362.5	273	DUMMY[6]	-1597.5	-362.5	330	DP[2]	967.5	-362.5
217	DUMMY[3]	-4117.5	-362.5	274	DUMMY[7]	-1552.5	-362.5	331	DN[2]	1012.5	-362.5
218	TP[43]	-4072.5	-362.5	275	DUMMY[8]	-1507.5	-362.5	332	DN[2]	1057.5	-362.5
219	TP[44]	-4027.5	-362.5	276	DUMMY[9]	-1462.5	-362.5	333	DN[2]	1102.5	-362.5
220	VDDIO	-3982.5	-362.5	277	DUMMY[10]	-1417.5	-362.5	334	DN[2]	1147.5	-362.5
221	VDDIO	-3937.5	-362.5	278	VSS_IF	-1372.5	-362.5	335	DN[2]	1192.5	-362.5
222	VDDIO	-3892.5	-362.5	279	VSS_IF	-1327.5	-362.5	336	DN[2]	1237.5	-362.5
223	VDDIO	-3847.5	-362.5	280	VSS_IF	-1282.5	-362.5	337	VSS_IF	1282.5	-362.5
224	VDDIO	-3802.5	-362.5	281	VSS_IF	-1237.5	-362.5	338	DP[3]	1327.5	-362.5
225	VDDIO	-3757.5	-362.5	282	VSS_IF	-1192.5	-362.5	339	DP[3]	1372.5	-362.5
226	VDD	-3712.5	-362.5	283	VSS_IF	-1147.5	-362.5	340	DP[3]	1417.5	-362.5
227	VDD	-3667.5	-362.5	284	VSS_IF	-1102.5	-362.5	341	DP[3]	1462.5	-362.5
228	VDD	-3622.5	-362.5	285	VSS_IF	-1057.5	-362.5	342	DP[3]	1507.5	-362.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
343	DP[3]	1552.5	-362.5	400	VDD_15V	4117.5	-362.5	457	TP[59]	6682.5	-362.5
344	DN[3]	1597.5	-362.5	401	VDD_15V	4162.5	-362.5	458	TP[60]	6727.5	-362.5
345	DN[3]	1642.5	-362.5	402	VDD_15V	4207.5	-362.5	459	TP[61]	6772.5	-362.5
346	DN[3]	1687.5	-362.5	403	VDD_15V	4252.5	-362.5	460	TP[62]	6817.5	-362.5
347	DN[3]	1732.5	-362.5	404	VDD_15V	4297.5	-362.5	461	TP[63]	6862.5	-362.5
348	DN[3]	1777.5	-362.5	405	VDD_15V	4342.5	-362.5	462	TP[64]	6907.5	-362.5
349	DN[3]	1822.5	-362.5	406	VDD_15V	4387.5	-362.5	463	TP[65]	6952.5	-362.5
350	VSS_IF	1867.5	-362.5	407	VDD	4432.5	-362.5	464	TP[66]	6997.5	-362.5
351	VSS_IF	1912.5	-362.5	408	VDD	4477.5	-362.5	465	TP[67]	7042.5	-362.5
352	DUMMY[11]	1957.5	-362.5	409	VDD	4522.5	-362.5	466	TP[68]	7087.5	-362.5
353	DUMMY[12]	2002.5	-362.5	410	VDD	4567.5	-362.5	467	TP[69]	7132.5	-362.5
354	TP[45]	2047.5	-362.5	411	VDD	4612.5	-362.5	468	TP[70]	7177.5	-362.5
355	TP[46]	2092.5	-362.5	412	VDD	4657.5	-362.5	469	CS_GIP	7222.5	-362.5
356	TP[47]	2137.5	-362.5	413	VDD	4702.5	-362.5	470	CS_GIP	7267.5	-362.5
357	TP[48]	2182.5	-362.5	414	VDD	4747.5	-362.5	471	CS_SD	7312.5	-362.5
358	TP[49]	2227.5	-362.5	415	VDD	4792.5	-362.5	472	CS_SD	7357.5	-362.5
359	TP[50]	2272.5	-362.5	416	VDD	4837.5	-362.5	473	DIR	7402.5	-362.5
360	VSS	2317.5	-362.5	417	VDD_IF	4882.5	-362.5	474	DIR	7447.5	-362.5
361	VSS	2362.5	-362.5	418	VDD_IF	4927.5	-362.5	475	REV	7492.5	-362.5
362	VSS	2407.5	-362.5	419	VDD_IF	4972.5	-362.5	476	REV	7537.5	-362.5
363	VSS	2452.5	-362.5	420	VDD_IF	5017.5	-362.5	477	TP[71]	7582.5	-362.5
364	VSS	2497.5	-362.5	421	VDD_IF	5062.5	-362.5	478	TP[72]	7627.5	-362.5
365	VSS	2542.5	-362.5	422	VDD_IF	5107.5	-362.5	479	TP[73]	7672.5	-362.5
366	VSS	2587.5	-362.5	423	VDD_IF	5152.5	-362.5	480	TP[74]	7717.5	-362.5
367	VSS	2632.5	-362.5	424	VDD_IF	5197.5	-362.5	481	A0	7762.5	-362.5
368	VSS	2677.5	-362.5	425	VDD_IF	5242.5	-362.5	482	A0	7807.5	-362.5
369	VSS	2722.5	-362.5	426	VDD_IF	5287.5	-362.5	483	DVCOM_WP	7852.5	-362.5
370	VSS	2767.5	-362.5	427	VDDIO	5332.5	-362.5	484	DVCOM_WP	7897.5	-362.5
371	VSS	2812.5	-362.5	428	VDDIO	5377.5	-362.5	485	SCL_I2C	7942.5	-362.5
372	VGH_REG	2857.5	-362.5	429	VDDIO	5422.5	-362.5	486	SCL_I2C	7987.5	-362.5
373	VGH_REG	2902.5	-362.5	430	VDDIO	5467.5	-362.5	487	SDA_I2C	8032.5	-362.5
374	VGH_REG	2947.5	-362.5	431	VDDIO	5512.5	-362.5	488	SDA_I2C	8077.5	-362.5
375	VGH_REG	2992.5	-362.5	432	VDDIO	5557.5	-362.5	489	SCAN_SEL	8122.5	-362.5
376	DUMMY[13]	3037.5	-362.5	433	VDDIO	5602.5	-362.5	490	SCAN_SEL	8167.5	-362.5
377	DUMMY[14]	3082.5	-362.5	434	VDDIO	5647.5	-362.5	491	INV_SEL[1]	8212.5	-362.5
378	DUMMY[15]	3127.5	-362.5	435	VDDIO	5692.5	-362.5	492	INV_SEL[1]	8257.5	-362.5
379	DUMMY[16]	3172.5	-362.5	436	VDDIO	5737.5	-362.5	493	INV_SEL[0]	8302.5	-362.5
380	DUMMY[17]	3217.5	-362.5	437	DUMMY[20]	5782.5	-362.5	494	INV_SEL[0]	8347.5	-362.5
381	DUMMY[18]	3262.5	-362.5	438	DUMMY[21]	5827.5	-362.5	495	DUMMY[30]	8392.5	-362.5
382	DUMMY[19]	3307.5	-362.5	439	DUMMY[22]	5872.5	-362.5	496	TP[75]	8437.5	-362.5
383	VDD_15V_IF	3352.5	-362.5	440	DUMMY[23]	5917.5	-362.5	497	TP[76]	8482.5	-362.5
384	VDD_15V_IF	3397.5	-362.5	441	DUMMY[24]	5962.5	-362.5	498	TP[77]	8527.5	-362.5
385	VDD_15V_IF	3442.5	-362.5	442	DUMMY[25]	6007.5	-362.5	499	DUMMY[31]	8572.5	-362.5
386	VDD_15V_IF	3487.5	-362.5	443	DUMMY[26]	6052.5	-362.5	500	DUMMY[32]	8617.5	-362.5
387	VDD_15V_IF	3532.5	-362.5	444	DUMMY[27]	6097.5	-362.5	501	DUMMY[33]	8662.5	-362.5
388	VDD_15V_IF	3577.5	-362.5	445	DUMMY[28]	6142.5	-362.5	502	DUMMY[34]	8707.5	-362.5
389	VDD_15V_IF	3622.5	-362.5	446	DUMMY[29]	6187.5	-362.5	503	DUMMY[35]	8752.5	-362.5
390	VDD_15V_IF	3667.5	-362.5	447	TP[51]	6232.5	-362.5	504	VSN	8797.5	-362.5
391	VDD_15V_IF	3712.5	-362.5	448	TP[52]	6277.5	-362.5	505	VSN	8842.5	-362.5
392	VDD_15V_IF	3757.5	-362.5	449	UPDN	6322.5	-362.5	506	VSN	8887.5	-362.5
393	VDD_15V_IF	3802.5	-362.5	450	UPDN	6367.5	-362.5	507	VSN	8932.5	-362.5
394	VDD_15V_IF	3847.5	-362.5	451	TP[53]	6412.5	-362.5	508	VSN	8977.5	-362.5
395	VDD_15V	3892.5	-362.5	452	TP[54]	6457.5	-362.5	509	VSN	9022.5	-362.5
396	VDD_15V	3937.5	-362.5	453	TP[55]	6502.5	-362.5	510	VSN	9067.5	-362.5
397	VDD_15V	3982.5	-362.5	454	TP[56]	6547.5	-362.5	511	VSP	9112.5	-362.5
398	VDD_15V	4027.5	-362.5	455	TP[57]	6592.5	-362.5	512	VSP	9157.5	-362.5
399	VDD_15V	4072.5	-362.5	456	TP[58]	6637.5	-362.5	513	VSP	9202.5	-362.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
514	VSP	9247.5	-362.5	571	VGL	11812.5	-362.5	628	PASS1_L	13308	372.5
515	VSP	9292.5	-362.5	572	VGL	11857.5	-362.5	629	VCOM	13296	192.5
516	VSP	9337.5	-362.5	573	VGL	11902.5	-362.5	630	VCOM	13284	282.5
517	VSP	9382.5	-362.5	574	VGL	11947.5	-362.5	631	VCOM	13272	372.5
518	VSSA	9427.5	-362.5	575	VGL	11992.5	-362.5	632	VCOM	13260	192.5
519	VSSA	9472.5	-362.5	576	VGL	12037.5	-362.5	633	VCOM	13248	282.5
520	VSSA	9517.5	-362.5	577	VGL	12082.5	-362.5	634	VCOM	13236	372.5
521	VSSA	9562.5	-362.5	578	VGL	12127.5	-362.5	635	PASS2_L	13224	192.5
522	VSSA	9607.5	-362.5	579	PASS2_L	12172.5	-362.5	636	PASS2_L	13212	282.5
523	VSSA	9652.5	-362.5	580	PASS2_L	12217.5	-362.5	637	PASS2_L	13200	372.5
524	VSSA	9697.5	-362.5	581	PASS2_L	12262.5	-362.5	638	PASS2_L	13188	192.5
525	VSSA	9742.5	-362.5	582	VCOM	12307.5	-362.5	639	PASS2_L	13176	282.5
526	VSS	9787.5	-362.5	583	VCOM	12352.5	-362.5	640	PASS2_L	13164	372.5
527	VSS	9832.5	-362.5	584	VCOM	12397.5	-362.5	641	DUMMY[43]	13152	192.5
528	VSS	9877.5	-362.5	585	VCOM	12442.5	-362.5	642	DUMMY[44]	13140	282.5
529	VSS	9922.5	-362.5	586	PASS1_L	12487.5	-362.5	643	DUMMY[45]	13128	372.5
530	VSS	9967.5	-362.5	587	PASS1_L	12542.5	-362.5	644	DUMMY[46]	13116	192.5
531	VSS	10012.5	-362.5	588	PASS1_L	12587.5	-362.5	645	DUMMY[47]	13104	282.5
532	VSS	10057.5	-362.5	589	GOUTL[22]	12632.5	-362.5	646	DUMMY[48]	13092	372.5
533	VDD_15V	10102.5	-362.5	590	GOUTL[21]	12677.5	-362.5	647	S[0]	13080	192.5
534	VDD_15V	10147.5	-362.5	591	GOUTL[20]	12722.5	-362.5	648	S[1]	13068	282.5
535	VDD_15V	10192.5	-362.5	592	GOUTL[19]	12767.5	-362.5	649	S[2]	13056	372.5
536	VDD_15V	10237.5	-362.5	593	GOUTL[18]	12812.5	-362.5	650	S[3]	13044	192.5
537	VDD_15V	10282.5	-362.5	594	GOUTL[17]	12857.5	-362.5	651	S[4]	13032	282.5
538	VDD_15V	10327.5	-362.5	595	GOUTL[16]	12902.5	-362.5	652	S[5]	13020	372.5
539	VGH_REG	10372.5	-362.5	596	GOUTL[15]	12947.5	-362.5	653	S[6]	13008	192.5
540	VGH_REG	10417.5	-362.5	597	GOUTL[14]	12992.5	-362.5	654	S[7]	12996	282.5
541	VGH_REG	10462.5	-362.5	598	GOUTL[13]	13037.5	-362.5	655	S[8]	12984	372.5
542	VGH_REG	10507.5	-362.5	599	GOUTL[12]	13082.5	-362.5	656	S[9]	12972	192.5
543	VGH_REG	10552.5	-362.5	600	GOUTL[11]	13127.5	-362.5	657	S[10]	12960	282.5
544	VGH_REG	10597.5	-362.5	601	GOUTL[10]	13172.5	-362.5	658	S[11]	12948	372.5
545	VGH_REG	10642.5	-362.5	602	GOUTL[9]	13217.5	-362.5	659	S[12]	12936	192.5
546	VGH_REG	10687.5	-362.5	603	GOUTL[8]	13262.5	-362.5	660	S[13]	12924	282.5
547	VGH_REG	10732.5	-362.5	604	GOUTL[7]	13307.5	-362.5	661	S[14]	12912	372.5
548	VGH_REG	10777.5	-362.5	605	GOUTL[6]	13352.5	-362.5	662	S[15]	12900	192.5
549	T_S[115]	10822.5	-362.5	606	GOUTL[5]	13397.5	-362.5	663	S[16]	12888	282.5
550	T_S[114]	10867.5	-362.5	607	GOUTL[4]	13442.5	-362.5	664	S[17]	12876	372.5
551	VGH	10912.5	-362.5	608	GOUTL[3]	13487.5	-362.5	665	S[18]	12864	192.5
552	VGH	10957.5	-362.5	609	GOUTL[2]	13532.5	-362.5	666	S[19]	12852	282.5
553	VGH	11002.5	-362.5	610	GOUTL[1]	13577.5	-362.5	667	S[20]	12840	372.5
554	VGH	11047.5	-362.5	611	DUMMY[36]	13622.5	-362.5	668	S[21]	12828	192.5
555	VGH	11092.5	-362.5	612	SYNC_L[4]	13710	94	669	S[22]	12816	282.5
556	VGH	11137.5	-362.5	613	SYNC_L[3]	13610	134	670	S[23]	12804	372.5
557	VGH	11182.5	-362.5	614	SYNC_L[2]	13710	174	671	S[24]	12792	192.5
558	VGH	11227.5	-362.5	615	SYNC_L[1]	13610	214	672	S[25]	12780	282.5
559	VGH	11272.5	-362.5	616	SYNC_L[0]	13710	254	673	S[26]	12768	372.5
560	VGH	11317.5	-362.5	617	DUMMY[37]	13440	192.5	674	S[27]	12756	192.5
561	VGL_REG	11362.5	-362.5	618	DUMMY[38]	13428	282.5	675	S[28]	12744	282.5
562	VGL_REG	11407.5	-362.5	619	DUMMY[39]	13416	372.5	676	S[29]	12732	372.5
563	VGL_REG	11452.5	-362.5	620	DUMMY[40]	13404	192.5	677	S[30]	12720	192.5
564	VGL_REG	11497.5	-362.5	621	DUMMY[41]	13392	282.5	678	S[31]	12708	282.5
565	VGL_REG	11542.5	-362.5	622	DUMMY[42]	13380	372.5	679	S[32]	12696	372.5
566	VGL_REG	11587.5	-362.5	623	PASS1_L	13368	192.5	680	S[33]	12684	192.5
567	VGL_REG	11632.5	-362.5	624	PASS1_L	13356	282.5	681	S[34]	12672	282.5
568	VGL_REG	11677.5	-362.5	625	PASS1_L	13344	372.5	682	S[35]	12660	372.5
569	VGL	11722.5	-362.5	626	PASS1_L	13332	192.5	683	S[36]	12648	192.5
570	VGL	11767.5	-362.5	627	PASS1_L	13320	282.5	684	S[37]	12636	282.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
685	S[38]	12624	372.5	742	S[95]	11940	372.5	799	S[152]	11256	372.5
686	S[39]	12612	192.5	743	S[96]	11928	192.5	800	S[153]	11244	192.5
687	S[40]	12600	282.5	744	S[97]	11916	282.5	801	S[154]	11232	282.5
688	S[41]	12588	372.5	745	S[98]	11904	372.5	802	S[155]	11220	372.5
689	S[42]	12576	192.5	746	S[99]	11892	192.5	803	S[156]	11208	192.5
690	S[43]	12564	282.5	747	S[100]	11880	282.5	804	S[157]	11196	282.5
691	S[44]	12552	372.5	748	S[101]	11868	372.5	805	S[158]	11184	372.5
692	S[45]	12540	192.5	749	S[102]	11856	192.5	806	S[159]	11172	192.5
693	S[46]	12528	282.5	750	S[103]	11844	282.5	807	S[160]	11160	282.5
694	S[47]	12516	372.5	751	S[104]	11832	372.5	808	S[161]	11148	372.5
695	S[48]	12504	192.5	752	S[105]	11820	192.5	809	S[162]	11136	192.5
696	S[49]	12492	282.5	753	S[106]	11808	282.5	810	S[163]	11124	282.5
697	S[50]	12480	372.5	754	S[107]	11796	372.5	811	S[164]	11112	372.5
698	S[51]	12468	192.5	755	S[108]	11784	192.5	812	S[165]	11100	192.5
699	S[52]	12456	282.5	756	S[109]	11772	282.5	813	S[166]	11088	282.5
700	S[53]	12444	372.5	757	S[110]	11760	372.5	814	S[167]	11076	372.5
701	S[54]	12432	192.5	758	S[111]	11748	192.5	815	S[168]	11064	192.5
702	S[55]	12420	282.5	759	S[112]	11736	282.5	816	S[169]	11052	282.5
703	S[56]	12408	372.5	760	S[113]	11724	372.5	817	S[170]	11040	372.5
704	S[57]	12396	192.5	761	S[114]	11712	192.5	818	S[171]	11028	192.5
705	S[58]	12384	282.5	762	S[115]	11700	282.5	819	S[172]	11016	282.5
706	S[59]	12372	372.5	763	S[116]	11688	372.5	820	S[173]	11004	372.5
707	S[60]	12360	192.5	764	S[117]	11676	192.5	821	S[174]	10992	192.5
708	S[61]	12348	282.5	765	S[118]	11664	282.5	822	S[175]	10980	282.5
709	S[62]	12336	372.5	766	S[119]	11652	372.5	823	S[176]	10968	372.5
710	S[63]	12324	192.5	767	S[120]	11640	192.5	824	S[177]	10956	192.5
711	S[64]	12312	282.5	768	S[121]	11628	282.5	825	S[178]	10944	282.5
712	S[65]	12300	372.5	769	S[122]	11616	372.5	826	S[179]	10932	372.5
713	S[66]	12288	192.5	770	S[123]	11604	192.5	827	S[180]	10920	192.5
714	S[67]	12276	282.5	771	S[124]	11592	282.5	828	S[181]	10908	282.5
715	S[68]	12264	372.5	772	S[125]	11580	372.5	829	S[182]	10896	372.5
716	S[69]	12252	192.5	773	S[126]	11568	192.5	830	S[183]	10884	192.5
717	S[70]	12240	282.5	774	S[127]	11556	282.5	831	S[184]	10872	282.5
718	S[71]	12228	372.5	775	S[128]	11544	372.5	832	S[185]	10860	372.5
719	S[72]	12216	192.5	776	S[129]	11532	192.5	833	S[186]	10848	192.5
720	S[73]	12204	282.5	777	S[130]	11520	282.5	834	S[187]	10836	282.5
721	S[74]	12192	372.5	778	S[131]	11508	372.5	835	S[188]	10824	372.5
722	S[75]	12180	192.5	779	S[132]	11496	192.5	836	S[189]	10812	192.5
723	S[76]	12168	282.5	780	S[133]	11484	282.5	837	S[190]	10800	282.5
724	S[77]	12156	372.5	781	S[134]	11472	372.5	838	S[191]	10788	372.5
725	S[78]	12144	192.5	782	S[135]	11460	192.5	839	S[192]	10776	192.5
726	S[79]	12132	282.5	783	S[136]	11448	282.5	840	S[193]	10764	282.5
727	S[80]	12120	372.5	784	S[137]	11436	372.5	841	S[194]	10752	372.5
728	S[81]	12108	192.5	785	S[138]	11424	192.5	842	S[195]	10740	192.5
729	S[82]	12096	282.5	786	S[139]	11412	282.5	843	S[196]	10728	282.5
730	S[83]	12084	372.5	787	S[140]	11400	372.5	844	S[197]	10716	372.5
731	S[84]	12072	192.5	788	S[141]	11388	192.5	845	S[198]	10704	192.5
732	S[85]	12060	282.5	789	S[142]	11376	282.5	846	S[199]	10692	282.5
733	S[86]	12048	372.5	790	S[143]	11364	372.5	847	S[200]	10680	372.5
734	S[87]	12036	192.5	791	S[144]	11352	192.5	848	S[201]	10668	192.5
735	S[88]	12024	282.5	792	S[145]	11340	282.5	849	S[202]	10656	282.5
736	S[89]	12012	372.5	793	S[146]	11328	372.5	850	S[203]	10644	372.5
737	S[90]	12000	192.5	794	S[147]	11316	192.5	851	S[204]	10632	192.5
738	S[91]	11988	282.5	795	S[148]	11304	282.5	852	S[205]	10620	282.5
739	S[92]	11976	372.5	796	S[149]	11292	372.5	853	S[206]	10608	372.5
740	S[93]	11964	192.5	797	S[150]	11280	192.5	854	S[207]	10596	192.5
741	S[94]	11952	282.5	798	S[151]	11268	282.5	855	S[208]	10584	282.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
856	S[209]	10572	372.5	913	S[266]	9888	372.5	970	S[323]	9204	372.5
857	S[210]	10560	192.5	914	S[267]	9876	192.5	971	S[324]	9192	192.5
858	S[211]	10548	282.5	915	S[268]	9864	282.5	972	S[325]	9180	282.5
859	S[212]	10536	372.5	916	S[269]	9852	372.5	973	S[326]	9168	372.5
860	S[213]	10524	192.5	917	S[270]	9840	192.5	974	S[327]	9156	192.5
861	S[214]	10512	282.5	918	S[271]	9828	282.5	975	S[328]	9144	282.5
862	S[215]	10500	372.5	919	S[272]	9816	372.5	976	S[329]	9132	372.5
863	S[216]	10488	192.5	920	S[273]	9804	192.5	977	S[330]	9120	192.5
864	S[217]	10476	282.5	921	S[274]	9792	282.5	978	S[331]	9108	282.5
865	S[218]	10464	372.5	922	S[275]	9780	372.5	979	S[332]	9096	372.5
866	S[219]	10452	192.5	923	S[276]	9768	192.5	980	S[333]	9084	192.5
867	S[220]	10440	282.5	924	S[277]	9756	282.5	981	S[334]	9072	282.5
868	S[221]	10428	372.5	925	S[278]	9744	372.5	982	S[335]	9060	372.5
869	S[222]	10416	192.5	926	S[279]	9732	192.5	983	S[336]	9048	192.5
870	S[223]	10404	282.5	927	S[280]	9720	282.5	984	S[337]	9036	282.5
871	S[224]	10392	372.5	928	S[281]	9708	372.5	985	S[338]	9024	372.5
872	S[225]	10380	192.5	929	S[282]	9696	192.5	986	S[339]	9012	192.5
873	S[226]	10368	282.5	930	S[283]	9684	282.5	987	S[340]	9000	282.5
874	S[227]	10356	372.5	931	S[284]	9672	372.5	988	S[341]	8988	372.5
875	S[228]	10344	192.5	932	S[285]	9660	192.5	989	S[342]	8976	192.5
876	S[229]	10332	282.5	933	S[286]	9648	282.5	990	S[343]	8964	282.5
877	S[230]	10320	372.5	934	S[287]	9636	372.5	991	S[344]	8952	372.5
878	S[231]	10308	192.5	935	S[288]	9624	192.5	992	S[345]	8940	192.5
879	S[232]	10296	282.5	936	S[289]	9612	282.5	993	S[346]	8928	282.5
880	S[233]	10284	372.5	937	S[290]	9600	372.5	994	S[347]	8916	372.5
881	S[234]	10272	192.5	938	S[291]	9588	192.5	995	S[348]	8904	192.5
882	S[235]	10260	282.5	939	S[292]	9576	282.5	996	S[349]	8892	282.5
883	S[236]	10248	372.5	940	S[293]	9564	372.5	997	S[350]	8880	372.5
884	S[237]	10236	192.5	941	S[294]	9552	192.5	998	S[351]	8868	192.5
885	S[238]	10224	282.5	942	S[295]	9540	282.5	999	S[352]	8856	282.5
886	S[239]	10212	372.5	943	S[296]	9528	372.5	1000	S[353]	8844	372.5
887	S[240]	10200	192.5	944	S[297]	9516	192.5	1001	S[354]	8832	192.5
888	S[241]	10188	282.5	945	S[298]	9504	282.5	1002	S[355]	8820	282.5
889	S[242]	10176	372.5	946	S[299]	9492	372.5	1003	S[356]	8808	372.5
890	S[243]	10164	192.5	947	S[300]	9480	192.5	1004	S[357]	8796	192.5
891	S[244]	10152	282.5	948	S[301]	9468	282.5	1005	S[358]	8784	282.5
892	S[245]	10140	372.5	949	S[302]	9456	372.5	1006	S[359]	8772	372.5
893	S[246]	10128	192.5	950	S[303]	9444	192.5	1007	S[360]	8760	192.5
894	S[247]	10116	282.5	951	S[304]	9432	282.5	1008	S[361]	8748	282.5
895	S[248]	10104	372.5	952	S[305]	9420	372.5	1009	S[362]	8736	372.5
896	S[249]	10092	192.5	953	S[306]	9408	192.5	1010	S[363]	8724	192.5
897	S[250]	10080	282.5	954	S[307]	9396	282.5	1011	S[364]	8712	282.5
898	S[251]	10068	372.5	955	S[308]	9384	372.5	1012	S[365]	8700	372.5
899	S[252]	10056	192.5	956	S[309]	9372	192.5	1013	S[366]	8688	192.5
900	S[253]	10044	282.5	957	S[310]	9360	282.5	1014	S[367]	8676	282.5
901	S[254]	10032	372.5	958	S[311]	9348	372.5	1015	S[368]	8664	372.5
902	S[255]	10020	192.5	959	S[312]	9336	192.5	1016	S[369]	8652	192.5
903	S[256]	10008	282.5	960	S[313]	9324	282.5	1017	S[370]	8640	282.5
904	S[257]	9996	372.5	961	S[314]	9312	372.5	1018	S[371]	8628	372.5
905	S[258]	9984	192.5	962	S[315]	9300	192.5	1019	S[372]	8616	192.5
906	S[259]	9972	282.5	963	S[316]	9288	282.5	1020	S[373]	8604	282.5
907	S[260]	9960	372.5	964	S[317]	9276	372.5	1021	S[374]	8592	372.5
908	S[261]	9948	192.5	965	S[318]	9264	192.5	1022	S[375]	8580	192.5
909	S[262]	9936	282.5	966	S[319]	9252	282.5	1023	S[376]	8568	282.5
910	S[263]	9924	372.5	967	S[320]	9240	372.5	1024	S[377]	8556	372.5
911	S[264]	9912	192.5	968	S[321]	9228	192.5	1025	S[378]	8544	192.5
912	S[265]	9900	282.5	969	S[322]	9216	282.5	1026	S[379]	8532	282.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1027	S[380]	8520	372.5	1084	S[437]	7836	372.5	1141	S[494]	7152	372.5
1028	S[381]	8508	192.5	1085	S[438]	7824	192.5	1142	S[495]	7140	192.5
1029	S[382]	8496	282.5	1086	S[439]	7812	282.5	1143	S[496]	7128	282.5
1030	S[383]	8484	372.5	1087	S[440]	7800	372.5	1144	S[497]	7116	372.5
1031	S[384]	8472	192.5	1088	S[441]	7788	192.5	1145	S[498]	7104	192.5
1032	S[385]	8460	282.5	1089	S[442]	7776	282.5	1146	S[499]	7092	282.5
1033	S[386]	8448	372.5	1090	S[443]	7764	372.5	1147	S[500]	7080	372.5
1034	S[387]	8436	192.5	1091	S[444]	7752	192.5	1148	S[501]	7068	192.5
1035	S[388]	8424	282.5	1092	S[445]	7740	282.5	1149	S[502]	7056	282.5
1036	S[389]	8412	372.5	1093	S[446]	7728	372.5	1150	S[503]	7044	372.5
1037	S[390]	8400	192.5	1094	S[447]	7716	192.5	1151	S[504]	7032	192.5
1038	S[391]	8388	282.5	1095	S[448]	7704	282.5	1152	S[505]	7020	282.5
1039	S[392]	8376	372.5	1096	S[449]	7692	372.5	1153	S[506]	7008	372.5
1040	S[393]	8364	192.5	1097	S[450]	7680	192.5	1154	S[507]	6996	192.5
1041	S[394]	8352	282.5	1098	S[451]	7668	282.5	1155	S[508]	6984	282.5
1042	S[395]	8340	372.5	1099	S[452]	7656	372.5	1156	S[509]	6972	372.5
1043	S[396]	8328	192.5	1100	S[453]	7644	192.5	1157	S[510]	6960	192.5
1044	S[397]	8316	282.5	1101	S[454]	7632	282.5	1158	S[511]	6948	282.5
1045	S[398]	8304	372.5	1102	S[455]	7620	372.5	1159	S[512]	6936	372.5
1046	S[399]	8292	192.5	1103	S[456]	7608	192.5	1160	DUMMY[49]	6924	192.5
1047	S[400]	8280	282.5	1104	S[457]	7596	282.5	1161	DUMMY[50]	6912	282.5
1048	S[401]	8268	372.5	1105	S[458]	7584	372.5	1162	DUMMY[51]	6900	372.5
1049	S[402]	8256	192.5	1106	S[459]	7572	192.5	1163	DUMMY[52]	6888	192.5
1050	S[403]	8244	282.5	1107	S[460]	7560	282.5	1164	DUMMY[53]	6876	282.5
1051	S[404]	8232	372.5	1108	S[461]	7548	372.5	1165	DUMMY[54]	6864	372.5
1052	S[405]	8220	192.5	1109	S[462]	7536	192.5	1166	DUMMY[55]	6852	192.5
1053	S[406]	8208	282.5	1110	S[463]	7524	282.5	1167	DUMMY[56]	6840	282.5
1054	S[407]	8196	372.5	1111	S[464]	7512	372.5	1168	DUMMY[57]	6828	372.5
1055	S[408]	8184	192.5	1112	S[465]	7500	192.5	1169	DUMMY[58]	6816	192.5
1056	S[409]	8172	282.5	1113	S[466]	7488	282.5	1170	DUMMY[59]	6804	282.5
1057	S[410]	8160	372.5	1114	S[467]	7476	372.5	1171	DUMMY[60]	6792	372.5
1058	S[411]	8148	192.5	1115	S[468]	7464	192.5	1172	DUMMY[61]	6780	192.5
1059	S[412]	8136	282.5	1116	S[469]	7452	282.5	1173	DUMMY[62]	6768	282.5
1060	S[413]	8124	372.5	1117	S[470]	7440	372.5	1174	DUMMY[63]	6756	372.5
1061	S[414]	8112	192.5	1118	S[471]	7428	192.5	1175	DUMMY[64]	6744	192.5
1062	S[415]	8100	282.5	1119	S[472]	7416	282.5	1176	DUMMY[65]	6732	282.5
1063	S[416]	8088	372.5	1120	S[473]	7404	372.5	1177	DUMMY[66]	6720	372.5
1064	S[417]	8076	192.5	1121	S[474]	7392	192.5	1178	S[513]	6708	192.5
1065	S[418]	8064	282.5	1122	S[475]	7380	282.5	1179	S[514]	6696	282.5
1066	S[419]	8052	372.5	1123	S[476]	7368	372.5	1180	S[515]	6684	372.5
1067	S[420]	8040	192.5	1124	S[477]	7356	192.5	1181	S[516]	6672	192.5
1068	S[421]	8028	282.5	1125	S[478]	7344	282.5	1182	S[517]	6660	282.5
1069	S[422]	8016	372.5	1126	S[479]	7332	372.5	1183	S[518]	6648	372.5
1070	S[423]	8004	192.5	1127	S[480]	7320	192.5	1184	S[519]	6636	192.5
1071	S[424]	7992	282.5	1128	S[481]	7308	282.5	1185	S[520]	6624	282.5
1072	S[425]	7980	372.5	1129	S[482]	7296	372.5	1186	S[521]	6612	372.5
1073	S[426]	7968	192.5	1130	S[483]	7284	192.5	1187	S[522]	6600	192.5
1074	S[427]	7956	282.5	1131	S[484]	7272	282.5	1188	S[523]	6588	282.5
1075	S[428]	7944	372.5	1132	S[485]	7260	372.5	1189	S[524]	6576	372.5
1076	S[429]	7932	192.5	1133	S[486]	7248	192.5	1190	S[525]	6564	192.5
1077	S[430]	7920	282.5	1134	S[487]	7236	282.5	1191	S[526]	6552	282.5
1078	S[431]	7908	372.5	1135	S[488]	7224	372.5	1192	S[527]	6540	372.5
1079	S[432]	7896	192.5	1136	S[489]	7212	192.5	1193	S[528]	6528	192.5
1080	S[433]	7884	282.5	1137	S[490]	7200	282.5	1194	S[529]	6516	282.5
1081	S[434]	7872	372.5	1138	S[491]	7188	372.5	1195	S[530]	6504	372.5
1082	S[435]	7860	192.5	1139	S[492]	7176	192.5	1196	S[531]	6492	192.5
1083	S[436]	7848	282.5	1140	S[493]	7164	282.5	1197	S[532]	6480	282.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1198	S[533]	6468	372.5	1255	S[590]	5784	372.5	1312	S[647]	5100	372.5
1199	S[534]	6456	192.5	1256	S[591]	5772	192.5	1313	S[648]	5088	192.5
1200	S[535]	6444	282.5	1257	S[592]	5760	282.5	1314	S[649]	5076	282.5
1201	S[536]	6432	372.5	1258	S[593]	5748	372.5	1315	S[650]	5064	372.5
1202	S[537]	6420	192.5	1259	S[594]	5736	192.5	1316	S[651]	5052	192.5
1203	S[538]	6408	282.5	1260	S[595]	5724	282.5	1317	S[652]	5040	282.5
1204	S[539]	6396	372.5	1261	S[596]	5712	372.5	1318	S[653]	5028	372.5
1205	S[540]	6384	192.5	1262	S[597]	5700	192.5	1319	S[654]	5016	192.5
1206	S[541]	6372	282.5	1263	S[598]	5688	282.5	1320	S[655]	5004	282.5
1207	S[542]	6360	372.5	1264	S[599]	5676	372.5	1321	S[656]	4992	372.5
1208	S[543]	6348	192.5	1265	S[600]	5664	192.5	1322	S[657]	4980	192.5
1209	S[544]	6336	282.5	1266	S[601]	5652	282.5	1323	S[658]	4968	282.5
1210	S[545]	6324	372.5	1267	S[602]	5640	372.5	1324	S[659]	4956	372.5
1211	S[546]	6312	192.5	1268	S[603]	5628	192.5	1325	S[660]	4944	192.5
1212	S[547]	6300	282.5	1269	S[604]	5616	282.5	1326	S[661]	4932	282.5
1213	S[548]	6288	372.5	1270	S[605]	5604	372.5	1327	S[662]	4920	372.5
1214	S[549]	6276	192.5	1271	S[606]	5592	192.5	1328	S[663]	4908	192.5
1215	S[550]	6264	282.5	1272	S[607]	5580	282.5	1329	S[664]	4896	282.5
1216	S[551]	6252	372.5	1273	S[608]	5568	372.5	1330	S[665]	4884	372.5
1217	S[552]	6240	192.5	1274	S[609]	5556	192.5	1331	S[666]	4872	192.5
1218	S[553]	6228	282.5	1275	S[610]	5544	282.5	1332	S[667]	4860	282.5
1219	S[554]	6216	372.5	1276	S[611]	5532	372.5	1333	S[668]	4848	372.5
1220	S[555]	6204	192.5	1277	S[612]	5520	192.5	1334	S[669]	4836	192.5
1221	S[556]	6192	282.5	1278	S[613]	5508	282.5	1335	S[670]	4824	282.5
1222	S[557]	6180	372.5	1279	S[614]	5496	372.5	1336	S[671]	4812	372.5
1223	S[558]	6168	192.5	1280	S[615]	5484	192.5	1337	S[672]	4800	192.5
1224	S[559]	6156	282.5	1281	S[616]	5472	282.5	1338	S[673]	4788	282.5
1225	S[560]	6144	372.5	1282	S[617]	5460	372.5	1339	S[674]	4776	372.5
1226	S[561]	6132	192.5	1283	S[618]	5448	192.5	1340	S[675]	4764	192.5
1227	S[562]	6120	282.5	1284	S[619]	5436	282.5	1341	S[676]	4752	282.5
1228	S[563]	6108	372.5	1285	S[620]	5424	372.5	1342	S[677]	4740	372.5
1229	S[564]	6096	192.5	1286	S[621]	5412	192.5	1343	S[678]	4728	192.5
1230	S[565]	6084	282.5	1287	S[622]	5400	282.5	1344	S[679]	4716	282.5
1231	S[566]	6072	372.5	1288	S[623]	5388	372.5	1345	S[680]	4704	372.5
1232	S[567]	6060	192.5	1289	S[624]	5376	192.5	1346	S[681]	4692	192.5
1233	S[568]	6048	282.5	1290	S[625]	5364	282.5	1347	S[682]	4680	282.5
1234	S[569]	6036	372.5	1291	S[626]	5352	372.5	1348	S[683]	4668	372.5
1235	S[570]	6024	192.5	1292	S[627]	5340	192.5	1349	S[684]	4656	192.5
1236	S[571]	6012	282.5	1293	S[628]	5328	282.5	1350	S[685]	4644	282.5
1237	S[572]	6000	372.5	1294	S[629]	5316	372.5	1351	S[686]	4632	372.5
1238	S[573]	5988	192.5	1295	S[630]	5304	192.5	1352	S[687]	4620	192.5
1239	S[574]	5976	282.5	1296	S[631]	5292	282.5	1353	S[688]	4608	282.5
1240	S[575]	5964	372.5	1297	S[632]	5280	372.5	1354	S[689]	4596	372.5
1241	S[576]	5952	192.5	1298	S[633]	5268	192.5	1355	S[690]	4584	192.5
1242	S[577]	5940	282.5	1299	S[634]	5256	282.5	1356	S[691]	4572	282.5
1243	S[578]	5928	372.5	1300	S[635]	5244	372.5	1357	S[692]	4560	372.5
1244	S[579]	5916	192.5	1301	S[636]	5232	192.5	1358	S[693]	4548	192.5
1245	S[580]	5904	282.5	1302	S[637]	5220	282.5	1359	S[694]	4536	282.5
1246	S[581]	5892	372.5	1303	S[638]	5208	372.5	1360	S[695]	4524	372.5
1247	S[582]	5880	192.5	1304	S[639]	5196	192.5	1361	S[696]	4512	192.5
1248	S[583]	5868	282.5	1305	S[640]	5184	282.5	1362	S[697]	4500	282.5
1249	S[584]	5856	372.5	1306	S[641]	5172	372.5	1363	S[698]	4488	372.5
1250	S[585]	5844	192.5	1307	S[642]	5160	192.5	1364	S[699]	4476	192.5
1251	S[586]	5832	282.5	1308	S[643]	5148	282.5	1365	S[700]	4464	282.5
1252	S[587]	5820	372.5	1309	S[644]	5136	372.5	1366	S[701]	4452	372.5
1253	S[588]	5808	192.5	1310	S[645]	5124	192.5	1367	S[702]	4440	192.5
1254	S[589]	5796	282.5	1311	S[646]	5112	282.5	1368	S[703]	4428	282.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1369	S[704]	4416	372.5	1426	S[761]	3732	372.5	1483	S[818]	3048	372.5
1370	S[705]	4404	192.5	1427	S[762]	3720	192.5	1484	S[819]	3036	192.5
1371	S[706]	4392	282.5	1428	S[763]	3708	282.5	1485	S[820]	3024	282.5
1372	S[707]	4380	372.5	1429	S[764]	3696	372.5	1486	S[821]	3012	372.5
1373	S[708]	4368	192.5	1430	S[765]	3684	192.5	1487	S[822]	3000	192.5
1374	S[709]	4356	282.5	1431	S[766]	3672	282.5	1488	S[823]	2988	282.5
1375	S[710]	4344	372.5	1432	S[767]	3660	372.5	1489	S[824]	2976	372.5
1376	S[711]	4332	192.5	1433	S[768]	3648	192.5	1490	S[825]	2964	192.5
1377	S[712]	4320	282.5	1434	S[769]	3636	282.5	1491	S[826]	2952	282.5
1378	S[713]	4308	372.5	1435	S[770]	3624	372.5	1492	S[827]	2940	372.5
1379	S[714]	4296	192.5	1436	S[771]	3612	192.5	1493	S[828]	2928	192.5
1380	S[715]	4284	282.5	1437	S[772]	3600	282.5	1494	S[829]	2916	282.5
1381	S[716]	4272	372.5	1438	S[773]	3588	372.5	1495	S[830]	2904	372.5
1382	S[717]	4260	192.5	1439	S[774]	3576	192.5	1496	S[831]	2892	192.5
1383	S[718]	4248	282.5	1440	S[775]	3564	282.5	1497	S[832]	2880	282.5
1384	S[719]	4236	372.5	1441	S[776]	3552	372.5	1498	S[833]	2868	372.5
1385	S[720]	4224	192.5	1442	S[777]	3540	192.5	1499	S[834]	2856	192.5
1386	S[721]	4212	282.5	1443	S[778]	3528	282.5	1500	S[835]	2844	282.5
1387	S[722]	4200	372.5	1444	S[779]	3516	372.5	1501	S[836]	2832	372.5
1388	S[723]	4188	192.5	1445	S[780]	3504	192.5	1502	S[837]	2820	192.5
1389	S[724]	4176	282.5	1446	S[781]	3492	282.5	1503	S[838]	2808	282.5
1390	S[725]	4164	372.5	1447	S[782]	3480	372.5	1504	S[839]	2796	372.5
1391	S[726]	4152	192.5	1448	S[783]	3468	192.5	1505	S[840]	2784	192.5
1392	S[727]	4140	282.5	1449	S[784]	3456	282.5	1506	S[841]	2772	282.5
1393	S[728]	4128	372.5	1450	S[785]	3444	372.5	1507	S[842]	2760	372.5
1394	S[729]	4116	192.5	1451	S[786]	3432	192.5	1508	S[843]	2748	192.5
1395	S[730]	4104	282.5	1452	S[787]	3420	282.5	1509	S[844]	2736	282.5
1396	S[731]	4092	372.5	1453	S[788]	3408	372.5	1510	S[845]	2724	372.5
1397	S[732]	4080	192.5	1454	S[789]	3396	192.5	1511	S[846]	2712	192.5
1398	S[733]	4068	282.5	1455	S[790]	3384	282.5	1512	S[847]	2700	282.5
1399	S[734]	4056	372.5	1456	S[791]	3372	372.5	1513	S[848]	2688	372.5
1400	S[735]	4044	192.5	1457	S[792]	3360	192.5	1514	S[849]	2676	192.5
1401	S[736]	4032	282.5	1458	S[793]	3348	282.5	1515	S[850]	2664	282.5
1402	S[737]	4020	372.5	1459	S[794]	3336	372.5	1516	S[851]	2652	372.5
1403	S[738]	4008	192.5	1460	S[795]	3324	192.5	1517	S[852]	2640	192.5
1404	S[739]	3996	282.5	1461	S[796]	3312	282.5	1518	S[853]	2628	282.5
1405	S[740]	3984	372.5	1462	S[797]	3300	372.5	1519	S[854]	2616	372.5
1406	S[741]	3972	192.5	1463	S[798]	3288	192.5	1520	S[855]	2604	192.5
1407	S[742]	3960	282.5	1464	S[799]	3276	282.5	1521	S[856]	2592	282.5
1408	S[743]	3948	372.5	1465	S[800]	3264	372.5	1522	S[857]	2580	372.5
1409	S[744]	3936	192.5	1466	S[801]	3252	192.5	1523	S[858]	2568	192.5
1410	S[745]	3924	282.5	1467	S[802]	3240	282.5	1524	S[859]	2556	282.5
1411	S[746]	3912	372.5	1468	S[803]	3228	372.5	1525	S[860]	2544	372.5
1412	S[747]	3900	192.5	1469	S[804]	3216	192.5	1526	S[861]	2532	192.5
1413	S[748]	3888	282.5	1470	S[805]	3204	282.5	1527	S[862]	2520	282.5
1414	S[749]	3876	372.5	1471	S[806]	3192	372.5	1528	S[863]	2508	372.5
1415	S[750]	3864	192.5	1472	S[807]	3180	192.5	1529	S[864]	2496	192.5
1416	S[751]	3852	282.5	1473	S[808]	3168	282.5	1530	S[865]	2484	282.5
1417	S[752]	3840	372.5	1474	S[809]	3156	372.5	1531	S[866]	2472	372.5
1418	S[753]	3828	192.5	1475	S[810]	3144	192.5	1532	S[867]	2460	192.5
1419	S[754]	3816	282.5	1476	S[811]	3132	282.5	1533	S[868]	2448	282.5
1420	S[755]	3804	372.5	1477	S[812]	3120	372.5	1534	S[869]	2436	372.5
1421	S[756]	3792	192.5	1478	S[813]	3108	192.5	1535	S[870]	2424	192.5
1422	S[757]	3780	282.5	1479	S[814]	3096	282.5	1536	S[871]	2412	282.5
1423	S[758]	3768	372.5	1480	S[815]	3084	372.5	1537	S[872]	2400	372.5
1424	S[759]	3756	192.5	1481	S[816]	3072	192.5	1538	S[873]	2388	192.5
1425	S[760]	3744	282.5	1482	S[817]	3060	282.5	1539	S[874]	2376	282.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1540	S[875]	2364	372.5	1597	S[932]	1680	372.5	1654	S[989]	996	372.5
1541	S[876]	2352	192.5	1598	S[933]	1668	192.5	1655	S[990]	984	192.5
1542	S[877]	2340	282.5	1599	S[934]	1656	282.5	1656	S[991]	972	282.5
1543	S[878]	2328	372.5	1600	S[935]	1644	372.5	1657	S[992]	960	372.5
1544	S[879]	2316	192.5	1601	S[936]	1632	192.5	1658	S[993]	948	192.5
1545	S[880]	2304	282.5	1602	S[937]	1620	282.5	1659	S[994]	936	282.5
1546	S[881]	2292	372.5	1603	S[938]	1608	372.5	1660	S[995]	924	372.5
1547	S[882]	2280	192.5	1604	S[939]	1596	192.5	1661	S[996]	912	192.5
1548	S[883]	2268	282.5	1605	S[940]	1584	282.5	1662	S[997]	900	282.5
1549	S[884]	2256	372.5	1606	S[941]	1572	372.5	1663	S[998]	888	372.5
1550	S[885]	2244	192.5	1607	S[942]	1560	192.5	1664	S[999]	876	192.5
1551	S[886]	2232	282.5	1608	S[943]	1548	282.5	1665	S[1000]	864	282.5
1552	S[887]	2220	372.5	1609	S[944]	1536	372.5	1666	S[1001]	852	372.5
1553	S[888]	2208	192.5	1610	S[945]	1524	192.5	1667	S[1002]	840	192.5
1554	S[889]	2196	282.5	1611	S[946]	1512	282.5	1668	S[1003]	828	282.5
1555	S[890]	2184	372.5	1612	S[947]	1500	372.5	1669	S[1004]	816	372.5
1556	S[891]	2172	192.5	1613	S[948]	1488	192.5	1670	S[1005]	804	192.5
1557	S[892]	2160	282.5	1614	S[949]	1476	282.5	1671	S[1006]	792	282.5
1558	S[893]	2148	372.5	1615	S[950]	1464	372.5	1672	S[1007]	780	372.5
1559	S[894]	2136	192.5	1616	S[951]	1452	192.5	1673	S[1008]	768	192.5
1560	S[895]	2124	282.5	1617	S[952]	1440	282.5	1674	S[1009]	756	282.5
1561	S[896]	2112	372.5	1618	S[953]	1428	372.5	1675	S[1010]	744	372.5
1562	S[897]	2100	192.5	1619	S[954]	1416	192.5	1676	S[1011]	732	192.5
1563	S[898]	2088	282.5	1620	S[955]	1404	282.5	1677	S[1012]	720	282.5
1564	S[899]	2076	372.5	1621	S[956]	1392	372.5	1678	S[1013]	708	372.5
1565	S[900]	2064	192.5	1622	S[957]	1380	192.5	1679	S[1014]	696	192.5
1566	S[901]	2052	282.5	1623	S[958]	1368	282.5	1680	S[1015]	684	282.5
1567	S[902]	2040	372.5	1624	S[959]	1356	372.5	1681	S[1016]	672	372.5
1568	S[903]	2028	192.5	1625	S[960]	1344	192.5	1682	S[1017]	660	192.5
1569	S[904]	2016	282.5	1626	S[961]	1332	282.5	1683	S[1018]	648	282.5
1570	S[905]	2004	372.5	1627	S[962]	1320	372.5	1684	S[1019]	636	372.5
1571	S[906]	1992	192.5	1628	S[963]	1308	192.5	1685	S[1020]	624	192.5
1572	S[907]	1980	282.5	1629	S[964]	1296	282.5	1686	S[1021]	612	282.5
1573	S[908]	1968	372.5	1630	S[965]	1284	372.5	1687	S[1022]	600	372.5
1574	S[909]	1956	192.5	1631	S[966]	1272	192.5	1688	S[1023]	588	192.5
1575	S[910]	1944	282.5	1632	S[967]	1260	282.5	1689	S[1024]	576	282.5
1576	S[911]	1932	372.5	1633	S[968]	1248	372.5	1690	S[1025]	564	372.5
1577	S[912]	1920	192.5	1634	S[969]	1236	192.5	1691	DUMMY[67]	528	372.5
1578	S[913]	1908	282.5	1635	S[970]	1224	282.5	1692	DUMMY[68]	492	372.5
1579	S[914]	1896	372.5	1636	S[971]	1212	372.5	1693	DUMMY[69]	456	372.5
1580	S[915]	1884	192.5	1637	S[972]	1200	192.5	1694	DUMMY[70]	420	372.5
1581	S[916]	1872	282.5	1638	S[973]	1188	282.5	1695	DUMMY[71]	384	372.5
1582	S[917]	1860	372.5	1639	S[974]	1176	372.5	1696	DUMMY[72]	348	372.5
1583	S[918]	1848	192.5	1640	S[975]	1164	192.5	1697	DUMMY[73]	312	372.5
1584	S[919]	1836	282.5	1641	S[976]	1152	282.5	1698	DUMMY[74]	276	372.5
1585	S[920]	1824	372.5	1642	S[977]	1140	372.5	1699	DUMMY[75]	240	372.5
1586	S[921]	1812	192.5	1643	S[978]	1128	192.5	1700	DUMMY[76]	204	372.5
1587	S[922]	1800	282.5	1644	S[979]	1116	282.5	1701	DUMMY[77]	168	372.5
1588	S[923]	1788	372.5	1645	S[980]	1104	372.5	1702	DUMMY[78]	132	372.5
1589	S[924]	1776	192.5	1646	S[981]	1092	192.5	1703	DUMMY[79]	96	372.5
1590	S[925]	1764	282.5	1647	S[982]	1080	282.5	1704	DUMMY[80]	60	372.5
1591	S[926]	1752	372.5	1648	S[983]	1068	372.5	1705	DUMMY[81]	24	372.5
1592	S[927]	1740	192.5	1649	S[984]	1056	192.5	1706	DUMMY[82]	-12	372.5
1593	S[928]	1728	282.5	1650	S[985]	1044	282.5	1707	DUMMY[83]	-48	372.5
1594	S[929]	1716	372.5	1651	S[986]	1032	372.5	1708	DUMMY[84]	-84	372.5
1595	S[930]	1704	192.5	1652	S[987]	1020	192.5	1709	DUMMY[85]	-120	372.5
1596	S[931]	1692	282.5	1653	S[988]	1008	282.5	1710	DUMMY[86]	-156	372.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1711	DUMMY[87]	-192	372.5	1768	S[1073]	-1092	372.5	1825	S[1130]	-1776	372.5
1712	DUMMY[88]	-228	372.5	1769	S[1074]	-1104	192.5	1826	S[1131]	-1788	192.5
1713	DUMMY[89]	-264	372.5	1770	S[1075]	-1116	282.5	1827	S[1132]	-1800	282.5
1714	DUMMY[90]	-300	372.5	1771	S[1076]	-1128	372.5	1828	S[1133]	-1812	372.5
1715	DUMMY[91]	-336	372.5	1772	S[1077]	-1140	192.5	1829	S[1134]	-1824	192.5
1716	DUMMY[92]	-372	372.5	1773	S[1078]	-1152	282.5	1830	S[1135]	-1836	282.5
1717	DUMMY[93]	-408	372.5	1774	S[1079]	-1164	372.5	1831	S[1136]	-1848	372.5
1718	DUMMY[94]	-444	372.5	1775	S[1080]	-1176	192.5	1832	S[1137]	-1860	192.5
1719	DUMMY[95]	-480	372.5	1776	S[1081]	-1188	282.5	1833	S[1138]	-1872	282.5
1720	DUMMY[96]	-516	372.5	1777	S[1082]	-1200	372.5	1834	S[1139]	-1884	372.5
1721	S[1026]	-528	192.5	1778	S[1083]	-1212	192.5	1835	S[1140]	-1896	192.5
1722	S[1027]	-540	282.5	1779	S[1084]	-1224	282.5	1836	S[1141]	-1908	282.5
1723	S[1028]	-552	372.5	1780	S[1085]	-1236	372.5	1837	S[1142]	-1920	372.5
1724	S[1029]	-564	192.5	1781	S[1086]	-1248	192.5	1838	S[1143]	-1932	192.5
1725	S[1030]	-576	282.5	1782	S[1087]	-1260	282.5	1839	S[1144]	-1944	282.5
1726	S[1031]	-588	372.5	1783	S[1088]	-1272	372.5	1840	S[1145]	-1956	372.5
1727	S[1032]	-600	192.5	1784	S[1089]	-1284	192.5	1841	S[1146]	-1968	192.5
1728	S[1033]	-612	282.5	1785	S[1090]	-1296	282.5	1842	S[1147]	-1980	282.5
1729	S[1034]	-624	372.5	1786	S[1091]	-1308	372.5	1843	S[1148]	-1992	372.5
1730	S[1035]	-636	192.5	1787	S[1092]	-1320	192.5	1844	S[1149]	-2004	192.5
1731	S[1036]	-648	282.5	1788	S[1093]	-1332	282.5	1845	S[1150]	-2016	282.5
1732	S[1037]	-660	372.5	1789	S[1094]	-1344	372.5	1846	S[1151]	-2028	372.5
1733	S[1038]	-672	192.5	1790	S[1095]	-1356	192.5	1847	S[1152]	-2040	192.5
1734	S[1039]	-684	282.5	1791	S[1096]	-1368	282.5	1848	S[1153]	-2052	282.5
1735	S[1040]	-696	372.5	1792	S[1097]	-1380	372.5	1849	S[1154]	-2064	372.5
1736	S[1041]	-708	192.5	1793	S[1098]	-1392	192.5	1850	S[1155]	-2076	192.5
1737	S[1042]	-720	282.5	1794	S[1099]	-1404	282.5	1851	S[1156]	-2088	282.5
1738	S[1043]	-732	372.5	1795	S[1100]	-1416	372.5	1852	S[1157]	-2100	372.5
1739	S[1044]	-744	192.5	1796	S[1101]	-1428	192.5	1853	S[1158]	-2112	192.5
1740	S[1045]	-756	282.5	1797	S[1102]	-1440	282.5	1854	S[1159]	-2124	282.5
1741	S[1046]	-768	372.5	1798	S[1103]	-1452	372.5	1855	S[1160]	-2136	372.5
1742	S[1047]	-780	192.5	1799	S[1104]	-1464	192.5	1856	S[1161]	-2148	192.5
1743	S[1048]	-792	282.5	1800	S[1105]	-1476	282.5	1857	S[1162]	-2160	282.5
1744	S[1049]	-804	372.5	1801	S[1106]	-1488	372.5	1858	S[1163]	-2172	372.5
1745	S[1050]	-816	192.5	1802	S[1107]	-1500	192.5	1859	S[1164]	-2184	192.5
1746	S[1051]	-828	282.5	1803	S[1108]	-1512	282.5	1860	S[1165]	-2196	282.5
1747	S[1052]	-840	372.5	1804	S[1109]	-1524	372.5	1861	S[1166]	-2208	372.5
1748	S[1053]	-852	192.5	1805	S[1110]	-1536	192.5	1862	S[1167]	-2220	192.5
1749	S[1054]	-864	282.5	1806	S[1111]	-1548	282.5	1863	S[1168]	-2232	282.5
1750	S[1055]	-876	372.5	1807	S[1112]	-1560	372.5	1864	S[1169]	-2244	372.5
1751	S[1056]	-888	192.5	1808	S[1113]	-1572	192.5	1865	S[1170]	-2256	192.5
1752	S[1057]	-900	282.5	1809	S[1114]	-1584	282.5	1866	S[1171]	-2268	282.5
1753	S[1058]	-912	372.5	1810	S[1115]	-1596	372.5	1867	S[1172]	-2280	372.5
1754	S[1059]	-924	192.5	1811	S[1116]	-1608	192.5	1868	S[1173]	-2292	192.5
1755	S[1060]	-936	282.5	1812	S[1117]	-1620	282.5	1869	S[1174]	-2304	282.5
1756	S[1061]	-948	372.5	1813	S[1118]	-1632	372.5	1870	S[1175]	-2316	372.5
1757	S[1062]	-960	192.5	1814	S[1119]	-1644	192.5	1871	S[1176]	-2328	192.5
1758	S[1063]	-972	282.5	1815	S[1120]	-1656	282.5	1872	S[1177]	-2340	282.5
1759	S[1064]	-984	372.5	1816	S[1121]	-1668	372.5	1873	S[1178]	-2352	372.5
1760	S[1065]	-996	192.5	1817	S[1122]	-1680	192.5	1874	S[1179]	-2364	192.5
1761	S[1066]	-1008	282.5	1818	S[1123]	-1692	282.5	1875	S[1180]	-2376	282.5
1762	S[1067]	-1020	372.5	1819	S[1124]	-1704	372.5	1876	S[1181]	-2388	372.5
1763	S[1068]	-1032	192.5	1820	S[1125]	-1716	192.5	1877	S[1182]	-2400	192.5
1764	S[1069]	-1044	282.5	1821	S[1126]	-1728	282.5	1878	S[1183]	-2412	282.5
1765	S[1070]	-1056	372.5	1822	S[1127]	-1740	372.5	1879	S[1184]	-2424	372.5
1766	S[1071]	-1068	192.5	1823	S[1128]	-1752	192.5	1880	S[1185]	-2436	192.5
1767	S[1072]	-1080	282.5	1824	S[1129]	-1764	282.5	1881	S[1186]	-2448	282.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
1882	S[1187]	-2460	372.5	1939	S[1244]	-3144	372.5	1996	S[1301]	-3828	372.5
1883	S[1188]	-2472	192.5	1940	S[1245]	-3156	192.5	1997	S[1302]	-3840	192.5
1884	S[1189]	-2484	282.5	1941	S[1246]	-3168	282.5	1998	S[1303]	-3852	282.5
1885	S[1190]	-2496	372.5	1942	S[1247]	-3180	372.5	1999	S[1304]	-3864	372.5
1886	S[1191]	-2508	192.5	1943	S[1248]	-3192	192.5	2000	S[1305]	-3876	192.5
1887	S[1192]	-2520	282.5	1944	S[1249]	-3204	282.5	2001	S[1306]	-3888	282.5
1888	S[1193]	-2532	372.5	1945	S[1250]	-3216	372.5	2002	S[1307]	-3900	372.5
1889	S[1194]	-2544	192.5	1946	S[1251]	-3228	192.5	2003	S[1308]	-3912	192.5
1890	S[1195]	-2556	282.5	1947	S[1252]	-3240	282.5	2004	S[1309]	-3924	282.5
1891	S[1196]	-2568	372.5	1948	S[1253]	-3252	372.5	2005	S[1310]	-3936	372.5
1892	S[1197]	-2580	192.5	1949	S[1254]	-3264	192.5	2006	S[1311]	-3948	192.5
1893	S[1198]	-2592	282.5	1950	S[1255]	-3276	282.5	2007	S[1312]	-3960	282.5
1894	S[1199]	-2604	372.5	1951	S[1256]	-3288	372.5	2008	S[1313]	-3972	372.5
1895	S[1200]	-2616	192.5	1952	S[1257]	-3300	192.5	2009	S[1314]	-3984	192.5
1896	S[1201]	-2628	282.5	1953	S[1258]	-3312	282.5	2010	S[1315]	-3996	282.5
1897	S[1202]	-2640	372.5	1954	S[1259]	-3324	372.5	2011	S[1316]	-4008	372.5
1898	S[1203]	-2652	192.5	1955	S[1260]	-3336	192.5	2012	S[1317]	-4020	192.5
1899	S[1204]	-2664	282.5	1956	S[1261]	-3348	282.5	2013	S[1318]	-4032	282.5
1900	S[1205]	-2676	372.5	1957	S[1262]	-3360	372.5	2014	S[1319]	-4044	372.5
1901	S[1206]	-2688	192.5	1958	S[1263]	-3372	192.5	2015	S[1320]	-4056	192.5
1902	S[1207]	-2700	282.5	1959	S[1264]	-3384	282.5	2016	S[1321]	-4068	282.5
1903	S[1208]	-2712	372.5	1960	S[1265]	-3396	372.5	2017	S[1322]	-4080	372.5
1904	S[1209]	-2724	192.5	1961	S[1266]	-3408	192.5	2018	S[1323]	-4092	192.5
1905	S[1210]	-2736	282.5	1962	S[1267]	-3420	282.5	2019	S[1324]	-4104	282.5
1906	S[1211]	-2748	372.5	1963	S[1268]	-3432	372.5	2020	S[1325]	-4116	372.5
1907	S[1212]	-2760	192.5	1964	S[1269]	-3444	192.5	2021	S[1326]	-4128	192.5
1908	S[1213]	-2772	282.5	1965	S[1270]	-3456	282.5	2022	S[1327]	-4140	282.5
1909	S[1214]	-2784	372.5	1966	S[1271]	-3468	372.5	2023	S[1328]	-4152	372.5
1910	S[1215]	-2796	192.5	1967	S[1272]	-3480	192.5	2024	S[1329]	-4164	192.5
1911	S[1216]	-2808	282.5	1968	S[1273]	-3492	282.5	2025	S[1330]	-4176	282.5
1912	S[1217]	-2820	372.5	1969	S[1274]	-3504	372.5	2026	S[1331]	-4188	372.5
1913	S[1218]	-2832	192.5	1970	S[1275]	-3516	192.5	2027	S[1332]	-4200	192.5
1914	S[1219]	-2844	282.5	1971	S[1276]	-3528	282.5	2028	S[1333]	-4212	282.5
1915	S[1220]	-2856	372.5	1972	S[1277]	-3540	372.5	2029	S[1334]	-4224	372.5
1916	S[1221]	-2868	192.5	1973	S[1278]	-3552	192.5	2030	S[1335]	-4236	192.5
1917	S[1222]	-2880	282.5	1974	S[1279]	-3564	282.5	2031	S[1336]	-4248	282.5
1918	S[1223]	-2892	372.5	1975	S[1280]	-3576	372.5	2032	S[1337]	-4260	372.5
1919	S[1224]	-2904	192.5	1976	S[1281]	-3588	192.5	2033	S[1338]	-4272	192.5
1920	S[1225]	-2916	282.5	1977	S[1282]	-3600	282.5	2034	S[1339]	-4284	282.5
1921	S[1226]	-2928	372.5	1978	S[1283]	-3612	372.5	2035	S[1340]	-4296	372.5
1922	S[1227]	-2940	192.5	1979	S[1284]	-3624	192.5	2036	S[1341]	-4308	192.5
1923	S[1228]	-2952	282.5	1980	S[1285]	-3636	282.5	2037	S[1342]	-4320	282.5
1924	S[1229]	-2964	372.5	1981	S[1286]	-3648	372.5	2038	S[1343]	-4332	372.5
1925	S[1230]	-2976	192.5	1982	S[1287]	-3660	192.5	2039	S[1344]	-4344	192.5
1926	S[1231]	-2988	282.5	1983	S[1288]	-3672	282.5	2040	S[1345]	-4356	282.5
1927	S[1232]	-3000	372.5	1984	S[1289]	-3684	372.5	2041	S[1346]	-4368	372.5
1928	S[1233]	-3012	192.5	1985	S[1290]	-3696	192.5	2042	S[1347]	-4380	192.5
1929	S[1234]	-3024	282.5	1986	S[1291]	-3708	282.5	2043	S[1348]	-4392	282.5
1930	S[1235]	-3036	372.5	1987	S[1292]	-3720	372.5	2044	S[1349]	-4404	372.5
1931	S[1236]	-3048	192.5	1988	S[1293]	-3732	192.5	2045	S[1350]	-4416	192.5
1932	S[1237]	-3060	282.5	1989	S[1294]	-3744	282.5	2046	S[1351]	-4428	282.5
1933	S[1238]	-3072	372.5	1990	S[1295]	-3756	372.5	2047	S[1352]	-4440	372.5
1934	S[1239]	-3084	192.5	1991	S[1296]	-3768	192.5	2048	S[1353]	-4452	192.5
1935	S[1240]	-3096	282.5	1992	S[1297]	-3780	282.5	2049	S[1354]	-4464	282.5
1936	S[1241]	-3108	372.5	1993	S[1298]	-3792	372.5	2050	S[1355]	-4476	372.5
1937	S[1242]	-3120	192.5	1994	S[1299]	-3804	192.5	2051	S[1356]	-4488	192.5
1938	S[1243]	-3132	282.5	1995	S[1300]	-3816	282.5	2052	S[1357]	-4500	282.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
2053	S[1358]	-4512	372.5	2110	S[1415]	-5196	372.5	2167	S[1472]	-5880	372.5
2054	S[1359]	-4524	192.5	2111	S[1416]	-5208	192.5	2168	S[1473]	-5892	192.5
2055	S[1360]	-4536	282.5	2112	S[1417]	-5220	282.5	2169	S[1474]	-5904	282.5
2056	S[1361]	-4548	372.5	2113	S[1418]	-5232	372.5	2170	S[1475]	-5916	372.5
2057	S[1362]	-4560	192.5	2114	S[1419]	-5244	192.5	2171	S[1476]	-5928	192.5
2058	S[1363]	-4572	282.5	2115	S[1420]	-5256	282.5	2172	S[1477]	-5940	282.5
2059	S[1364]	-4584	372.5	2116	S[1421]	-5268	372.5	2173	S[1478]	-5952	372.5
2060	S[1365]	-4596	192.5	2117	S[1422]	-5280	192.5	2174	S[1479]	-5964	192.5
2061	S[1366]	-4608	282.5	2118	S[1423]	-5292	282.5	2175	S[1480]	-5976	282.5
2062	S[1367]	-4620	372.5	2119	S[1424]	-5304	372.5	2176	S[1481]	-5988	372.5
2063	S[1368]	-4632	192.5	2120	S[1425]	-5316	192.5	2177	S[1482]	-6000	192.5
2064	S[1369]	-4644	282.5	2121	S[1426]	-5328	282.5	2178	S[1483]	-6012	282.5
2065	S[1370]	-4656	372.5	2122	S[1427]	-5340	372.5	2179	S[1484]	-6024	372.5
2066	S[1371]	-4668	192.5	2123	S[1428]	-5352	192.5	2180	S[1485]	-6036	192.5
2067	S[1372]	-4680	282.5	2124	S[1429]	-5364	282.5	2181	S[1486]	-6048	282.5
2068	S[1373]	-4692	372.5	2125	S[1430]	-5376	372.5	2182	S[1487]	-6060	372.5
2069	S[1374]	-4704	192.5	2126	S[1431]	-5388	192.5	2183	S[1488]	-6072	192.5
2070	S[1375]	-4716	282.5	2127	S[1432]	-5400	282.5	2184	S[1489]	-6084	282.5
2071	S[1376]	-4728	372.5	2128	S[1433]	-5412	372.5	2185	S[1490]	-6096	372.5
2072	S[1377]	-4740	192.5	2129	S[1434]	-5424	192.5	2186	S[1491]	-6108	192.5
2073	S[1378]	-4752	282.5	2130	S[1435]	-5436	282.5	2187	S[1492]	-6120	282.5
2074	S[1379]	-4764	372.5	2131	S[1436]	-5448	372.5	2188	S[1493]	-6132	372.5
2075	S[1380]	-4776	192.5	2132	S[1437]	-5460	192.5	2189	S[1494]	-6144	192.5
2076	S[1381]	-4788	282.5	2133	S[1438]	-5472	282.5	2190	S[1495]	-6156	282.5
2077	S[1382]	-4800	372.5	2134	S[1439]	-5484	372.5	2191	S[1496]	-6168	372.5
2078	S[1383]	-4812	192.5	2135	S[1440]	-5496	192.5	2192	S[1497]	-6180	192.5
2079	S[1384]	-4824	282.5	2136	S[1441]	-5508	282.5	2193	S[1498]	-6192	282.5
2080	S[1385]	-4836	372.5	2137	S[1442]	-5520	372.5	2194	S[1499]	-6204	372.5
2081	S[1386]	-4848	192.5	2138	S[1443]	-5532	192.5	2195	S[1500]	-6216	192.5
2082	S[1387]	-4860	282.5	2139	S[1444]	-5544	282.5	2196	S[1501]	-6228	282.5
2083	S[1388]	-4872	372.5	2140	S[1445]	-5556	372.5	2197	S[1502]	-6240	372.5
2084	S[1389]	-4884	192.5	2141	S[1446]	-5568	192.5	2198	S[1503]	-6252	192.5
2085	S[1390]	-4896	282.5	2142	S[1447]	-5580	282.5	2199	S[1504]	-6264	282.5
2086	S[1391]	-4908	372.5	2143	S[1448]	-5592	372.5	2200	S[1505]	-6276	372.5
2087	S[1392]	-4920	192.5	2144	S[1449]	-5604	192.5	2201	S[1506]	-6288	192.5
2088	S[1393]	-4932	282.5	2145	S[1450]	-5616	282.5	2202	S[1507]	-6300	282.5
2089	S[1394]	-4944	372.5	2146	S[1451]	-5628	372.5	2203	S[1508]	-6312	372.5
2090	S[1395]	-4956	192.5	2147	S[1452]	-5640	192.5	2204	S[1509]	-6324	192.5
2091	S[1396]	-4968	282.5	2148	S[1453]	-5652	282.5	2205	S[1510]	-6336	282.5
2092	S[1397]	-4980	372.5	2149	S[1454]	-5664	372.5	2206	S[1511]	-6348	372.5
2093	S[1398]	-4992	192.5	2150	S[1455]	-5676	192.5	2207	S[1512]	-6360	192.5
2094	S[1399]	-5004	282.5	2151	S[1456]	-5688	282.5	2208	S[1513]	-6372	282.5
2095	S[1400]	-5016	372.5	2152	S[1457]	-5700	372.5	2209	S[1514]	-6384	372.5
2096	S[1401]	-5028	192.5	2153	S[1458]	-5712	192.5	2210	S[1515]	-6396	192.5
2097	S[1402]	-5040	282.5	2154	S[1459]	-5724	282.5	2211	S[1516]	-6408	282.5
2098	S[1403]	-5052	372.5	2155	S[1460]	-5736	372.5	2212	S[1517]	-6420	372.5
2099	S[1404]	-5064	192.5	2156	S[1461]	-5748	192.5	2213	S[1518]	-6432	192.5
2100	S[1405]	-5076	282.5	2157	S[1462]	-5760	282.5	2214	S[1519]	-6444	282.5
2101	S[1406]	-5088	372.5	2158	S[1463]	-5772	372.5	2215	S[1520]	-6456	372.5
2102	S[1407]	-5100	192.5	2159	S[1464]	-5784	192.5	2216	S[1521]	-6468	192.5
2103	S[1408]	-5112	282.5	2160	S[1465]	-5796	282.5	2217	S[1522]	-6480	282.5
2104	S[1409]	-5124	372.5	2161	S[1466]	-5808	372.5	2218	S[1523]	-6492	372.5
2105	S[1410]	-5136	192.5	2162	S[1467]	-5820	192.5	2219	S[1524]	-6504	192.5
2106	S[1411]	-5148	282.5	2163	S[1468]	-5832	282.5	2220	S[1525]	-6516	282.5
2107	S[1412]	-5160	372.5	2164	S[1469]	-5844	372.5	2221	S[1526]	-6528	372.5
2108	S[1413]	-5172	192.5	2165	S[1470]	-5856	192.5	2222	S[1527]	-6540	192.5
2109	S[1414]	-5184	282.5	2166	S[1471]	-5868	282.5	2223	S[1528]	-6552	282.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
2224	S[1529]	-6564	372.5	2281	S[1568]	-7248	372.5	2338	S[1625]	-7932	372.5
2225	S[1530]	-6576	192.5	2282	S[1569]	-7260	192.5	2339	S[1626]	-7944	192.5
2226	S[1531]	-6588	282.5	2283	S[1570]	-7272	282.5	2340	S[1627]	-7956	282.5
2227	S[1532]	-6600	372.5	2284	S[1571]	-7284	372.5	2341	S[1628]	-7968	372.5
2228	S[1533]	-6612	192.5	2285	S[1572]	-7296	192.5	2342	S[1629]	-7980	192.5
2229	S[1534]	-6624	282.5	2286	S[1573]	-7308	282.5	2343	S[1630]	-7992	282.5
2230	S[1535]	-6636	372.5	2287	S[1574]	-7320	372.5	2344	S[1631]	-8004	372.5
2231	S[1536]	-6648	192.5	2288	S[1575]	-7332	192.5	2345	S[1632]	-8016	192.5
2232	S[1537]	-6660	282.5	2289	S[1576]	-7344	282.5	2346	S[1633]	-8028	282.5
2233	S[1538]	-6672	372.5	2290	S[1577]	-7356	372.5	2347	S[1634]	-8040	372.5
2234	DUMMY[97]	-6684	192.5	2291	S[1578]	-7368	192.5	2348	S[1635]	-8052	192.5
2235	DUMMY[98]	-6696	282.5	2292	S[1579]	-7380	282.5	2349	S[1636]	-8064	282.5
2236	DUMMY[99]	-6708	372.5	2293	S[1580]	-7392	372.5	2350	S[1637]	-8076	372.5
2237	DUMMY[100]	-6720	192.5	2294	S[1581]	-7404	192.5	2351	S[1638]	-8088	192.5
2238	DUMMY[101]	-6732	282.5	2295	S[1582]	-7416	282.5	2352	S[1639]	-8100	282.5
2239	DUMMY[102]	-6744	372.5	2296	S[1583]	-7428	372.5	2353	S[1640]	-8112	372.5
2240	DUMMY[103]	-6756	192.5	2297	S[1584]	-7440	192.5	2354	S[1641]	-8124	192.5
2241	DUMMY[104]	-6768	282.5	2298	S[1585]	-7452	282.5	2355	S[1642]	-8136	282.5
2242	DUMMY[105]	-6780	372.5	2299	S[1586]	-7464	372.5	2356	S[1643]	-8148	372.5
2243	DUMMY[106]	-6792	192.5	2300	S[1587]	-7476	192.5	2357	S[1644]	-8160	192.5
2244	DUMMY[107]	-6804	282.5	2301	S[1588]	-7488	282.5	2358	S[1645]	-8172	282.5
2245	DUMMY[108]	-6816	372.5	2302	S[1589]	-7500	372.5	2359	S[1646]	-8184	372.5
2246	DUMMY[109]	-6828	192.5	2303	S[1590]	-7512	192.5	2360	S[1647]	-8196	192.5
2247	DUMMY[110]	-6840	282.5	2304	S[1591]	-7524	282.5	2361	S[1648]	-8208	282.5
2248	DUMMY[111]	-6852	372.5	2305	S[1592]	-7536	372.5	2362	S[1649]	-8220	372.5
2249	DUMMY[112]	-6864	192.5	2306	S[1593]	-7548	192.5	2363	S[1650]	-8232	192.5
2250	DUMMY[113]	-6876	282.5	2307	S[1594]	-7560	282.5	2364	S[1651]	-8244	282.5
2251	DUMMY[114]	-6888	372.5	2308	S[1595]	-7572	372.5	2365	S[1652]	-8256	372.5
2252	S[1539]	-6900	192.5	2309	S[1596]	-7584	192.5	2366	S[1653]	-8268	192.5
2253	S[1540]	-6912	282.5	2310	S[1597]	-7596	282.5	2367	S[1654]	-8280	282.5
2254	S[1541]	-6924	372.5	2311	S[1598]	-7608	372.5	2368	S[1655]	-8292	372.5
2255	S[1542]	-6936	192.5	2312	S[1599]	-7620	192.5	2369	S[1656]	-8304	192.5
2256	S[1543]	-6948	282.5	2313	S[1600]	-7632	282.5	2370	S[1657]	-8316	282.5
2257	S[1544]	-6960	372.5	2314	S[1601]	-7644	372.5	2371	S[1658]	-8328	372.5
2258	S[1545]	-6972	192.5	2315	S[1602]	-7656	192.5	2372	S[1659]	-8340	192.5
2259	S[1546]	-6984	282.5	2316	S[1603]	-7668	282.5	2373	S[1660]	-8352	282.5
2260	S[1547]	-6996	372.5	2317	S[1604]	-7680	372.5	2374	S[1661]	-8364	372.5
2261	S[1548]	-7008	192.5	2318	S[1605]	-7692	192.5	2375	S[1662]	-8376	192.5
2262	S[1549]	-7020	282.5	2319	S[1606]	-7704	282.5	2376	S[1663]	-8388	282.5
2263	S[1550]	-7032	372.5	2320	S[1607]	-7716	372.5	2377	S[1664]	-8400	372.5
2264	S[1551]	-7044	192.5	2321	S[1608]	-7728	192.5	2378	S[1665]	-8412	192.5
2265	S[1552]	-7056	282.5	2322	S[1609]	-7740	282.5	2379	S[1666]	-8424	282.5
2266	S[1553]	-7068	372.5	2323	S[1610]	-7752	372.5	2380	S[1667]	-8436	372.5
2267	S[1554]	-7080	192.5	2324	S[1611]	-7764	192.5	2381	S[1668]	-8448	192.5
2268	S[1555]	-7092	282.5	2325	S[1612]	-7776	282.5	2382	S[1669]	-8460	282.5
2269	S[1556]	-7104	372.5	2326	S[1613]	-7788	372.5	2383	S[1670]	-8472	372.5
2270	S[1557]	-7116	192.5	2327	S[1614]	-7800	192.5	2384	S[1671]	-8484	192.5
2271	S[1558]	-7128	282.5	2328	S[1615]	-7812	282.5	2385	S[1672]	-8496	282.5
2272	S[1559]	-7140	372.5	2329	S[1616]	-7824	372.5	2386	S[1673]	-8508	372.5
2273	S[1560]	-7152	192.5	2330	S[1617]	-7836	192.5	2387	S[1674]	-8520	192.5
2274	S[1561]	-7164	282.5	2331	S[1618]	-7848	282.5	2388	S[1675]	-8532	282.5
2275	S[1562]	-7176	372.5	2332	S[1619]	-7860	372.5	2389	S[1676]	-8544	372.5
2276	S[1563]	-7188	192.5	2333	S[1620]	-7872	192.5	2390	S[1677]	-8556	192.5
2277	S[1564]	-7200	282.5	2334	S[1621]	-7884	282.5	2391	S[1678]	-8568	282.5
2278	S[1565]	-7212	372.5	2335	S[1622]	-7896	372.5	2392	S[1679]	-8580	372.5
2279	S[1566]	-7224	192.5	2336	S[1623]	-7908	192.5	2393	S[1680]	-8592	192.5
2280	S[1567]	-7236	282.5	2337	S[1624]	-7920	282.5	2394	S[1681]	-8604	282.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
2395	S[1682]	-8616	372.5	2452	S[1739]	-9300	372.5	2509	S[1796]	-9984	372.5
2396	S[1683]	-8628	192.5	2453	S[1740]	-9312	192.5	2510	S[1797]	-9996	192.5
2397	S[1684]	-8640	282.5	2454	S[1741]	-9324	282.5	2511	S[1798]	-10008	282.5
2398	S[1685]	-8652	372.5	2455	S[1742]	-9336	372.5	2512	S[1799]	-10020	372.5
2399	S[1686]	-8664	192.5	2456	S[1743]	-9348	192.5	2513	S[1800]	-10032	192.5
2400	S[1687]	-8676	282.5	2457	S[1744]	-9360	282.5	2514	S[1801]	-10044	282.5
2401	S[1688]	-8688	372.5	2458	S[1745]	-9372	372.5	2515	S[1802]	-10056	372.5
2402	S[1689]	-8700	192.5	2459	S[1746]	-9384	192.5	2516	S[1803]	-10068	192.5
2403	S[1690]	-8712	282.5	2460	S[1747]	-9396	282.5	2517	S[1804]	-10080	282.5
2404	S[1691]	-8724	372.5	2461	S[1748]	-9408	372.5	2518	S[1805]	-10092	372.5
2405	S[1692]	-8736	192.5	2462	S[1749]	-9420	192.5	2519	S[1806]	-10104	192.5
2406	S[1693]	-8748	282.5	2463	S[1750]	-9432	282.5	2520	S[1807]	-10116	282.5
2407	S[1694]	-8760	372.5	2464	S[1751]	-9444	372.5	2521	S[1808]	-10128	372.5
2408	S[1695]	-8772	192.5	2465	S[1752]	-9456	192.5	2522	S[1809]	-10140	192.5
2409	S[1696]	-8784	282.5	2466	S[1753]	-9468	282.5	2523	S[1810]	-10152	282.5
2410	S[1697]	-8796	372.5	2467	S[1754]	-9480	372.5	2524	S[1811]	-10164	372.5
2411	S[1698]	-8808	192.5	2468	S[1755]	-9492	192.5	2525	S[1812]	-10176	192.5
2412	S[1699]	-8820	282.5	2469	S[1756]	-9504	282.5	2526	S[1813]	-10188	282.5
2413	S[1700]	-8832	372.5	2470	S[1757]	-9516	372.5	2527	S[1814]	-10200	372.5
2414	S[1701]	-8844	192.5	2471	S[1758]	-9528	192.5	2528	S[1815]	-10212	192.5
2415	S[1702]	-8856	282.5	2472	S[1759]	-9540	282.5	2529	S[1816]	-10224	282.5
2416	S[1703]	-8868	372.5	2473	S[1760]	-9552	372.5	2530	S[1817]	-10236	372.5
2417	S[1704]	-8880	192.5	2474	S[1761]	-9564	192.5	2531	S[1818]	-10248	192.5
2418	S[1705]	-8892	282.5	2475	S[1762]	-9576	282.5	2532	S[1819]	-10260	282.5
2419	S[1706]	-8904	372.5	2476	S[1763]	-9588	372.5	2533	S[1820]	-10272	372.5
2420	S[1707]	-8916	192.5	2477	S[1764]	-9600	192.5	2534	S[1821]	-10284	192.5
2421	S[1708]	-8928	282.5	2478	S[1765]	-9612	282.5	2535	S[1822]	-10296	282.5
2422	S[1709]	-8940	372.5	2479	S[1766]	-9624	372.5	2536	S[1823]	-10308	372.5
2423	S[1710]	-8952	192.5	2480	S[1767]	-9636	192.5	2537	S[1824]	-10320	192.5
2424	S[1711]	-8964	282.5	2481	S[1768]	-9648	282.5	2538	S[1825]	-10332	282.5
2425	S[1712]	-8976	372.5	2482	S[1769]	-9660	372.5	2539	S[1826]	-10344	372.5
2426	S[1713]	-8988	192.5	2483	S[1770]	-9672	192.5	2540	S[1827]	-10356	192.5
2427	S[1714]	-9000	282.5	2484	S[1771]	-9684	282.5	2541	S[1828]	-10368	282.5
2428	S[1715]	-9012	372.5	2485	S[1772]	-9696	372.5	2542	S[1829]	-10380	372.5
2429	S[1716]	-9024	192.5	2486	S[1773]	-9708	192.5	2543	S[1830]	-10392	192.5
2430	S[1717]	-9036	282.5	2487	S[1774]	-9720	282.5	2544	S[1831]	-10404	282.5
2431	S[1718]	-9048	372.5	2488	S[1775]	-9732	372.5	2545	S[1832]	-10416	372.5
2432	S[1719]	-9060	192.5	2489	S[1776]	-9744	192.5	2546	S[1833]	-10428	192.5
2433	S[1720]	-9072	282.5	2490	S[1777]	-9756	282.5	2547	S[1834]	-10440	282.5
2434	S[1721]	-9084	372.5	2491	S[1778]	-9768	372.5	2548	S[1835]	-10452	372.5
2435	S[1722]	-9096	192.5	2492	S[1779]	-9780	192.5	2549	S[1836]	-10464	192.5
2436	S[1723]	-9108	282.5	2493	S[1780]	-9792	282.5	2550	S[1837]	-10476	282.5
2437	S[1724]	-9120	372.5	2494	S[1781]	-9804	372.5	2551	S[1838]	-10488	372.5
2438	S[1725]	-9132	192.5	2495	S[1782]	-9816	192.5	2552	S[1839]	-10500	192.5
2439	S[1726]	-9144	282.5	2496	S[1783]	-9828	282.5	2553	S[1840]	-10512	282.5
2440	S[1727]	-9156	372.5	2497	S[1784]	-9840	372.5	2554	S[1841]	-10524	372.5
2441	S[1728]	-9168	192.5	2498	S[1785]	-9852	192.5	2555	S[1842]	-10536	192.5
2442	S[1729]	-9180	282.5	2499	S[1786]	-9864	282.5	2556	S[1843]	-10548	282.5
2443	S[1730]	-9192	372.5	2500	S[1787]	-9876	372.5	2557	S[1844]	-10560	372.5
2444	S[1731]	-9204	192.5	2501	S[1788]	-9888	192.5	2558	S[1845]	-10572	192.5
2445	S[1732]	-9216	282.5	2502	S[1789]	-9900	282.5	2559	S[1846]	-10584	282.5
2446	S[1733]	-9228	372.5	2503	S[1790]	-9912	372.5	2560	S[1847]	-10596	372.5
2447	S[1734]	-9240	192.5	2504	S[1791]	-9924	192.5	2561	S[1848]	-10608	192.5
2448	S[1735]	-9252	282.5	2505	S[1792]	-9936	282.5	2562	S[1849]	-10620	282.5
2449	S[1736]	-9264	372.5	2506	S[1793]	-9948	372.5	2563	S[1850]	-10632	372.5
2450	S[1737]	-9276	192.5	2507	S[1794]	-9960	192.5	2564	S[1851]	-10644	192.5
2451	S[1738]	-9288	282.5	2508	S[1795]	-9972	282.5	2565	S[1852]	-10656	282.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
2566	S[1853]	-10668	372.5	2623	S[1910]	-11352	372.5	2680	S[1967]	-12036	372.5
2567	S[1854]	-10680	192.5	2624	S[1911]	-11364	192.5	2681	S[1968]	-12048	192.5
2568	S[1855]	-10692	282.5	2625	S[1912]	-11376	282.5	2682	S[1969]	-12060	282.5
2569	S[1856]	-10704	372.5	2626	S[1913]	-11388	372.5	2683	S[1970]	-12072	372.5
2570	S[1857]	-10716	192.5	2627	S[1914]	-11400	192.5	2684	S[1971]	-12084	192.5
2571	S[1858]	-10728	282.5	2628	S[1915]	-11412	282.5	2685	S[1972]	-12096	282.5
2572	S[1859]	-10740	372.5	2629	S[1916]	-11424	372.5	2686	S[1973]	-12108	372.5
2573	S[1860]	-10752	192.5	2630	S[1917]	-11436	192.5	2687	S[1974]	-12120	192.5
2574	S[1861]	-10764	282.5	2631	S[1918]	-11448	282.5	2688	S[1975]	-12132	282.5
2575	S[1862]	-10776	372.5	2632	S[1919]	-11460	372.5	2689	S[1976]	-12144	372.5
2576	S[1863]	-10788	192.5	2633	S[1920]	-11472	192.5	2690	S[1977]	-12156	192.5
2577	S[1864]	-10800	282.5	2634	S[1921]	-11484	282.5	2691	S[1978]	-12168	282.5
2578	S[1865]	-10812	372.5	2635	S[1922]	-11496	372.5	2692	S[1979]	-12180	372.5
2579	S[1866]	-10824	192.5	2636	S[1923]	-11508	192.5	2693	S[1980]	-12192	192.5
2580	S[1867]	-10836	282.5	2637	S[1924]	-11520	282.5	2694	S[1981]	-12204	282.5
2581	S[1868]	-10848	372.5	2638	S[1925]	-11532	372.5	2695	S[1982]	-12216	372.5
2582	S[1869]	-10860	192.5	2639	S[1926]	-11544	192.5	2696	S[1983]	-12228	192.5
2583	S[1870]	-10872	282.5	2640	S[1927]	-11556	282.5	2697	S[1984]	-12240	282.5
2584	S[1871]	-10884	372.5	2641	S[1928]	-11568	372.5	2698	S[1985]	-12252	372.5
2585	S[1872]	-10896	192.5	2642	S[1929]	-11580	192.5	2699	S[1986]	-12264	192.5
2586	S[1873]	-10908	282.5	2643	S[1930]	-11592	282.5	2700	S[1987]	-12276	282.5
2587	S[1874]	-10920	372.5	2644	S[1931]	-11604	372.5	2701	S[1988]	-12288	372.5
2588	S[1875]	-10932	192.5	2645	S[1932]	-11616	192.5	2702	S[1989]	-12300	192.5
2589	S[1876]	-10944	282.5	2646	S[1933]	-11628	282.5	2703	S[1990]	-12312	282.5
2590	S[1877]	-10956	372.5	2647	S[1934]	-11640	372.5	2704	S[1991]	-12324	372.5
2591	S[1878]	-10968	192.5	2648	S[1935]	-11652	192.5	2705	S[1992]	-12336	192.5
2592	S[1879]	-10980	282.5	2649	S[1936]	-11664	282.5	2706	S[1993]	-12348	282.5
2593	S[1880]	-10992	372.5	2650	S[1937]	-11676	372.5	2707	S[1994]	-12360	372.5
2594	S[1881]	-11004	192.5	2651	S[1938]	-11688	192.5	2708	S[1995]	-12372	192.5
2595	S[1882]	-11016	282.5	2652	S[1939]	-11700	282.5	2709	S[1996]	-12384	282.5
2596	S[1883]	-11028	372.5	2653	S[1940]	-11712	372.5	2710	S[1997]	-12396	372.5
2597	S[1884]	-11040	192.5	2654	S[1941]	-11724	192.5	2711	S[1998]	-12408	192.5
2598	S[1885]	-11052	282.5	2655	S[1942]	-11736	282.5	2712	S[1999]	-12420	282.5
2599	S[1886]	-11064	372.5	2656	S[1943]	-11748	372.5	2713	S[2000]	-12432	372.5
2600	S[1887]	-11076	192.5	2657	S[1944]	-11760	192.5	2714	S[2001]	-12444	192.5
2601	S[1888]	-11088	282.5	2658	S[1945]	-11772	282.5	2715	S[2002]	-12456	282.5
2602	S[1889]	-11100	372.5	2659	S[1946]	-11784	372.5	2716	S[2003]	-12468	372.5
2603	S[1890]	-11112	192.5	2660	S[1947]	-11796	192.5	2717	S[2004]	-12480	192.5
2604	S[1891]	-11124	282.5	2661	S[1948]	-11808	282.5	2718	S[2005]	-12492	282.5
2605	S[1892]	-11136	372.5	2662	S[1949]	-11820	372.5	2719	S[2006]	-12504	372.5
2606	S[1893]	-11148	192.5	2663	S[1950]	-11832	192.5	2720	S[2007]	-12516	192.5
2607	S[1894]	-11160	282.5	2664	S[1951]	-11844	282.5	2721	S[2008]	-12528	282.5
2608	S[1895]	-11172	372.5	2665	S[1952]	-11856	372.5	2722	S[2009]	-12540	372.5
2609	S[1896]	-11184	192.5	2666	S[1953]	-11868	192.5	2723	S[2010]	-12552	192.5
2610	S[1897]	-11196	282.5	2667	S[1954]	-11880	282.5	2724	S[2011]	-12564	282.5
2611	S[1898]	-11208	372.5	2668	S[1955]	-11892	372.5	2725	S[2012]	-12576	372.5
2612	S[1899]	-11220	192.5	2669	S[1956]	-11904	192.5	2726	S[2013]	-12588	192.5
2613	S[1900]	-11232	282.5	2670	S[1957]	-11916	282.5	2727	S[2014]	-12600	282.5
2614	S[1901]	-11244	372.5	2671	S[1958]	-11928	372.5	2728	S[2015]	-12612	372.5
2615	S[1902]	-11256	192.5	2672	S[1959]	-11940	192.5	2729	S[2016]	-12624	192.5
2616	S[1903]	-11268	282.5	2673	S[1960]	-11952	282.5	2730	S[2017]	-12636	282.5
2617	S[1904]	-11280	372.5	2674	S[1961]	-11964	372.5	2731	S[2018]	-12648	372.5
2618	S[1905]	-11292	192.5	2675	S[1962]	-11976	192.5	2732	S[2019]	-12660	192.5
2619	S[1906]	-11304	282.5	2676	S[1963]	-11988	282.5	2733	S[2020]	-12672	282.5
2620	S[1907]	-11316	372.5	2677	S[1964]	-12000	372.5	2734	S[2021]	-12684	372.5
2621	S[1908]	-11328	192.5	2678	S[1965]	-12012	192.5	2735	S[2022]	-12696	192.5
2622	S[1909]	-11340	282.5	2679	S[1966]	-12024	282.5	2736	S[2023]	-12708	282.5

Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis	Pin	Pad name	X-axis	Y-axis
2737	S[2024]	-12720	372.5	2794	DUMMY[126]	-13404	372.5				
2738	S[2025]	-12732	192.5	2795	DUMMY[127]	-13416	192.5				
2739	S[2026]	-12744	282.5	2796	DUMMY[128]	-13428	282.5				
2740	S[2027]	-12756	372.5	2797	DUMMY[129]	-13440	372.5				
2741	S[2028]	-12768	192.5								
2742	S[2029]	-12780	282.5								
2743	S[2030]	-12792	372.5								
2744	S[2031]	-12804	192.5								
2745	S[2032]	-12816	282.5								
2746	S[2033]	-12828	372.5								
2747	S[2034]	-12840	192.5								
2748	S[2035]	-12852	282.5								
2749	S[2036]	-12864	372.5								
2750	S[2037]	-12876	192.5								
2751	S[2038]	-12888	282.5								
2752	S[2039]	-12900	372.5								
2753	S[2040]	-12912	192.5								
2754	S[2041]	-12924	282.5								
2755	S[2042]	-12936	372.5								
2756	S[2043]	-12948	192.5								
2757	S[2044]	-12960	282.5								
2758	S[2045]	-12972	372.5								
2759	S[2046]	-12984	192.5								
2760	S[2047]	-12996	282.5								
2761	S[2048]	-13008	372.5								
2762	S[2049]	-13020	192.5								
2763	S[2050]	-13032	282.5								
2764	S[2051]	-13044	372.5								
2765	DUMMY[115]	-13056	192.5								
2766	DUMMY[116]	-13068	282.5								
2767	DUMMY[117]	-13080	372.5								
2768	DUMMY[118]	-13092	192.5								
2769	DUMMY[119]	-13104	282.5								
2770	DUMMY[120]	-13116	372.5								
2771	PASS2_R	-13128	192.5								
2772	PASS2_R	-13140	282.5								
2773	PASS2_R	-13152	372.5								
2774	PASS2_R	-13164	192.5								
2775	PASS2_R	-13176	282.5								
2776	PASS2_R	-13188	372.5								
2777	VCOM	-13200	192.5								
2778	VCOM	-13212	282.5								
2779	VCOM	-13224	372.5								
2780	VCOM	-13236	192.5								
2781	VCOM	-13248	282.5								
2782	VCOM	-13260	372.5								
2783	PASS1_R	-13272	192.5								
2784	PASS1_R	-13284	282.5								
2785	PASS1_R	-13296	372.5								
2786	PASS1_R	-13308	192.5								
2787	PASS1_R	-13320	282.5								
2788	PASS1_R	-13332	372.5								
2789	DUMMY[121]	-13344	192.5								
2790	DUMMY[122]	-13356	282.5								
2791	DUMMY[123]	-13368	372.5								
2792	DUMMY[124]	-13380	192.5								
2793	DUMMY[125]	-13392	282.5								

16. REVISION HISTORY

Revision	Content	Page	Date
0.1	New SPEC For BA	-	2019/08/26
0.2	Modify Pin UPDN define	-	2019/11/26
0.3	Add Normal Dual gate & GOA Application description	P16	2019/12/11
0.4	Modify DIR description	P17	2020/06/18
0.5	Add LVDS DC electrical characteristics descript Add LVDS DE mode timing table DE/SYNC waveform	P44 P29~P30 P32	2020/07/09
0.6	Add LVDS signal characteristics	P44	2020/07/13
0.7	Modify LVDS signal characteristics	P44	2020/07/16
0.8	Modify LVDS DC electrical characteristics	P43	2020/07/20
0.9	Modify operating temperature value	-	2023/01/10
1.0	Add Dual Gate+Zigzag Driving Add Input Timing Table 1280X720 Modify Power on/pff sequence	8 32 36.37	2023/03/21
1.1	Modify LNSW define	18	2023/0406