Specification for LCD

AMC2002CR-B-Y6WFDY-I2C

Revision 00

A	Orient Display
MC	Character Display
2002	Character x Lines 20 x 2
CR	Module Dimension 116.0 x 37.5 x 14.5mm
B	COB Type
Y	STN YELLOW GREEN
6	6 o'clock viewing angle
W	Top: -20~+70°C; Tstr: -30~+80°C
F	Transflective
DY	Yellow Green LED Backlight
/	Controller RW1063-0A Or Compatible
I2C	I2C Interface

DOCUMENT REVISION HISTORY:

DATE	PAGE	DESCRIPTION
2024.4.	-	First release

Contents

1. Precautions in use of LCD Modules

(1)Avoid applying excessive shocks to the module or making any alterations or modifications to it.

(2)Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.

(3)Don't disassemble the LCM.

(4)Don't operate it above the absolute maximum rating.

(5)Don't drop, bend or twist LCM.

(6)Soldering: only to the I/O terminals.

(7)Storage: please storage in anti-static electricity container and clean environment.

2. General Specification

Item	Dimension	Unit
Number of Characters	20 characters x 2 Lines	—
Module dimension(With LED Backlight)	116.0 x 37.5 x 14.5（MAX）	mm
View area	83.0x18.6	mm
Active area	73.5x11.5	mm
Dot size	0.60x 0.65	mm
Dot pitch	0.65 x 0.70	mm
Character size	3.20 x 5.55	mm
Character pitch	3.70 x 5.95	mm
LCD type	STN, Yellow-green, Transflective	
Duty	1/16	
View direction	6 o'clock	
Backlight Type	Yellow-green LED Backlight	

3.Absolute Maximum Ratings

Item		Symbol	Min	Max	Unit
Input Voltage		V_I	-0.3	VDD+0.3	V
Supply Voltage For Logic		VDD-V_{SS}	-0.3	5.5	V
Supply Voltage For LCD		V_{DD}-V_0	Vdd-7.0	VDD+0.3	V
Wide Temperature LCM	Operating Temp.	Top	-20	70	℃
	Storage Temp.	Tstr	-30	80	℃

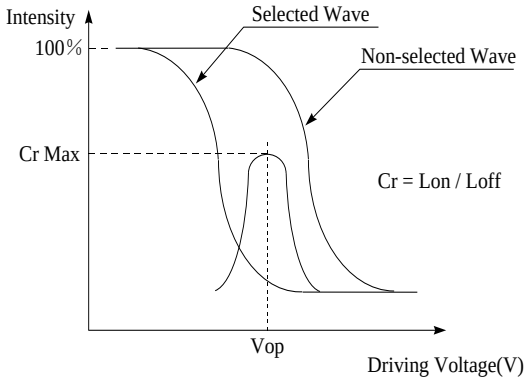
4. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	4.5	5.0	5.5	V
Supply Voltage For LCD	V_{DD}-V_0	Ta=25℃	4.4	4.7	5.0	V
Input High Volt.	V_{IH}	—	2.5	—	V_{DD}	V
Input Low Volt.	V_{IL}	—	-0.3	—	0.55	V
Supply Current	I_{DD}	V_{DD}=5V	0.8	1.2	2.0	mA
Supply Voltage of Yellow-green backlight	V_{LED}	Forward current =14 mA Number of LED die 2x1= 2	3.8	4.1	4.4	V

5. Optical Characteristics

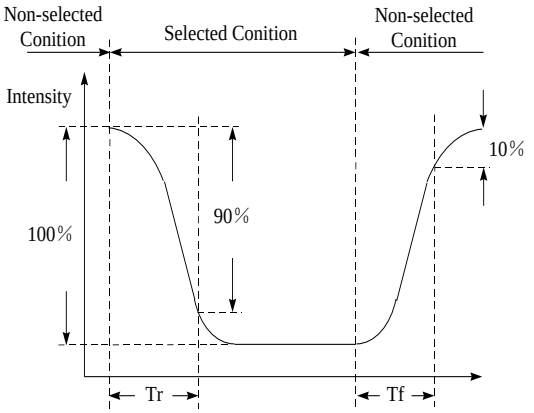
Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V)θ	CR≧2	-20	—	35	deg
	(H)φ	CR≧2	-30	—	30	deg
Contrast Ratio	CR	—	—	3	—	—
Response Time	T rise	—	—	—	250	ms
	T fall	—	—	—	250	ms

Definition of Operation Voltage (Vop)



[positive type]

Definition of Response Time (Tr , Tf)



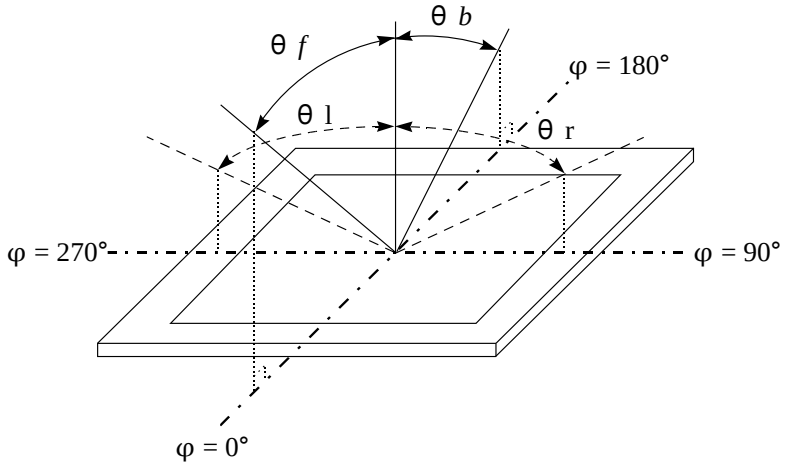
[positive type]

Conditions :

Operating Voltage : Vop Viewing Angle(θ，φ) : 0°， 0°

Frame Frequency : 64 HZ Driving Waveform : 1/N duty , 1/a bias

Definition of viewing angle(CR≧2)

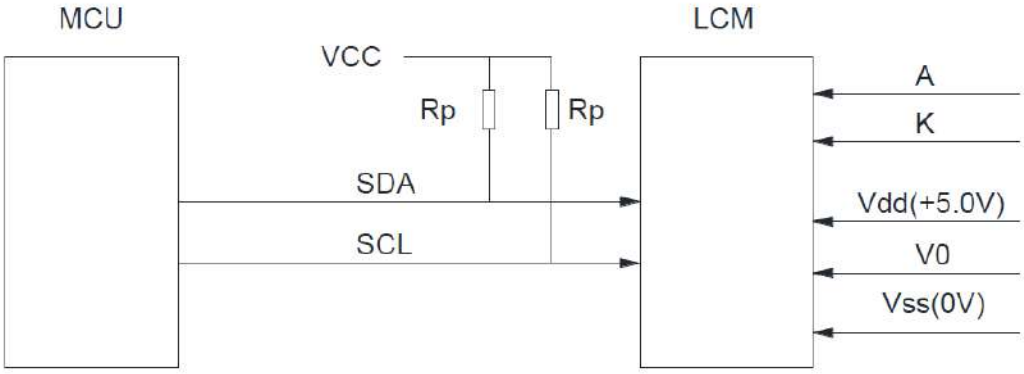


6. Interface Pin Function

Pin No.	Symbol	Level	Description
1	LED(+)		Anode of LED Backlight
2	LED(-)		Cathode of LED Backlight
3	V_{SS}	0V	Ground
4	V_{DD}	5.0V	Supply Voltage for logic
5	SDA	H/L	Serial Data
6	SCL	H/L	Serial Clock
7	V0	(Variable)	Operating voltage for adjusting contrast
8	NC	/	No Connection
9	NC	/	No Connection
10	NC	/	No Connection

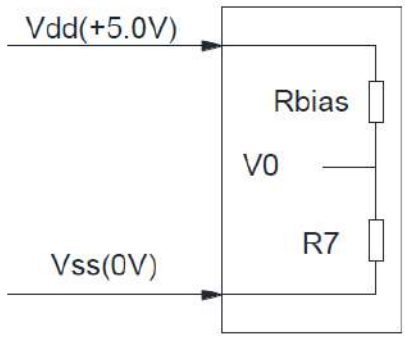
7. POWER SUPPLY

SINGLE SUPPLY VOLTAGE TYPE

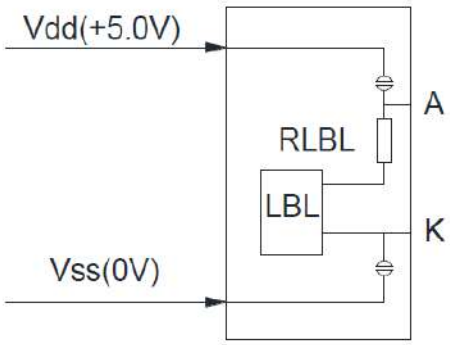


Use Internal Options to Simplify the Circuits

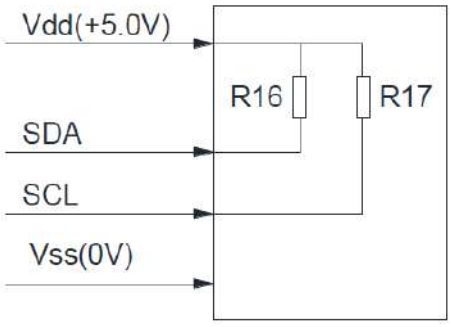
Option 1: Use internal R7 for V0



Option 2: Use internal jumpers for backlight power supply



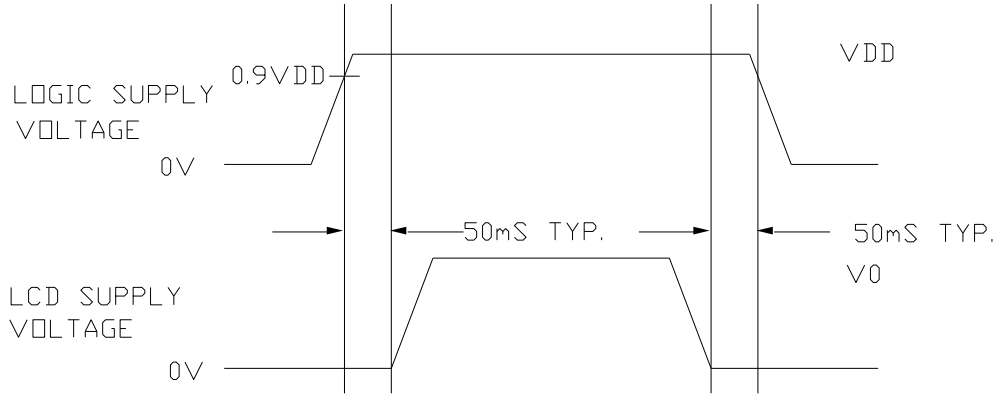
Option 3: Use internal resistors for pull up to Vdd



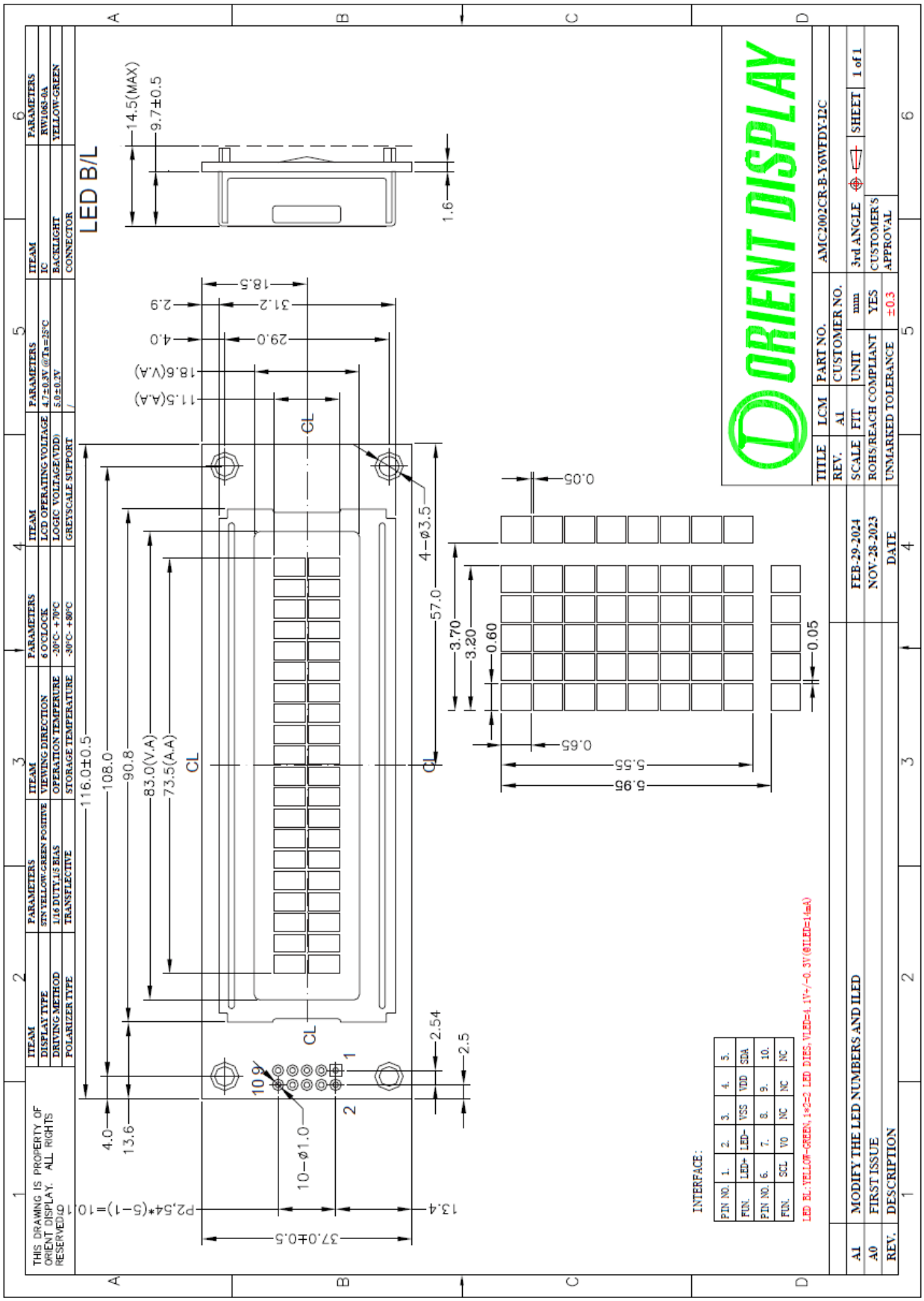
DUAL SUPPLY VOLTAGE TYPE

Timing Diagram of VDD Against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.



8. Contour Drawing &Block Diagram



9. Function Description

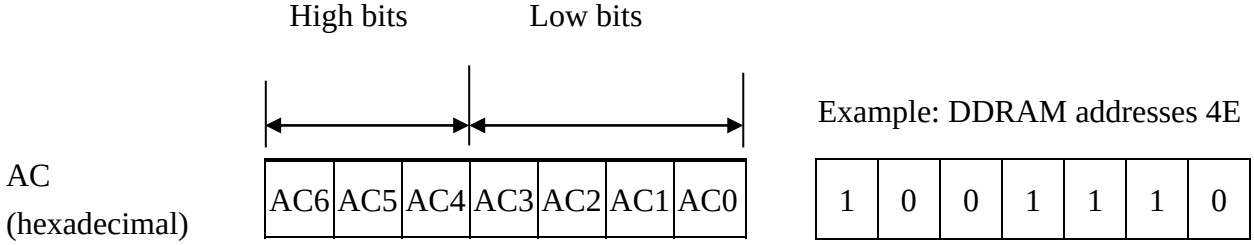
The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).
The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

Busy Flag (BF)
When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)
The address counter (AC) assigns addresses to both DDRAM and CGRAM

Display Data RAM (DDRAM)
This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.



Display position DDRAM address

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53

2-Line by 20-Character Display

Character Generator ROM (CGROM)

The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See Table 2.

Character Generator RAM (CGRAM)

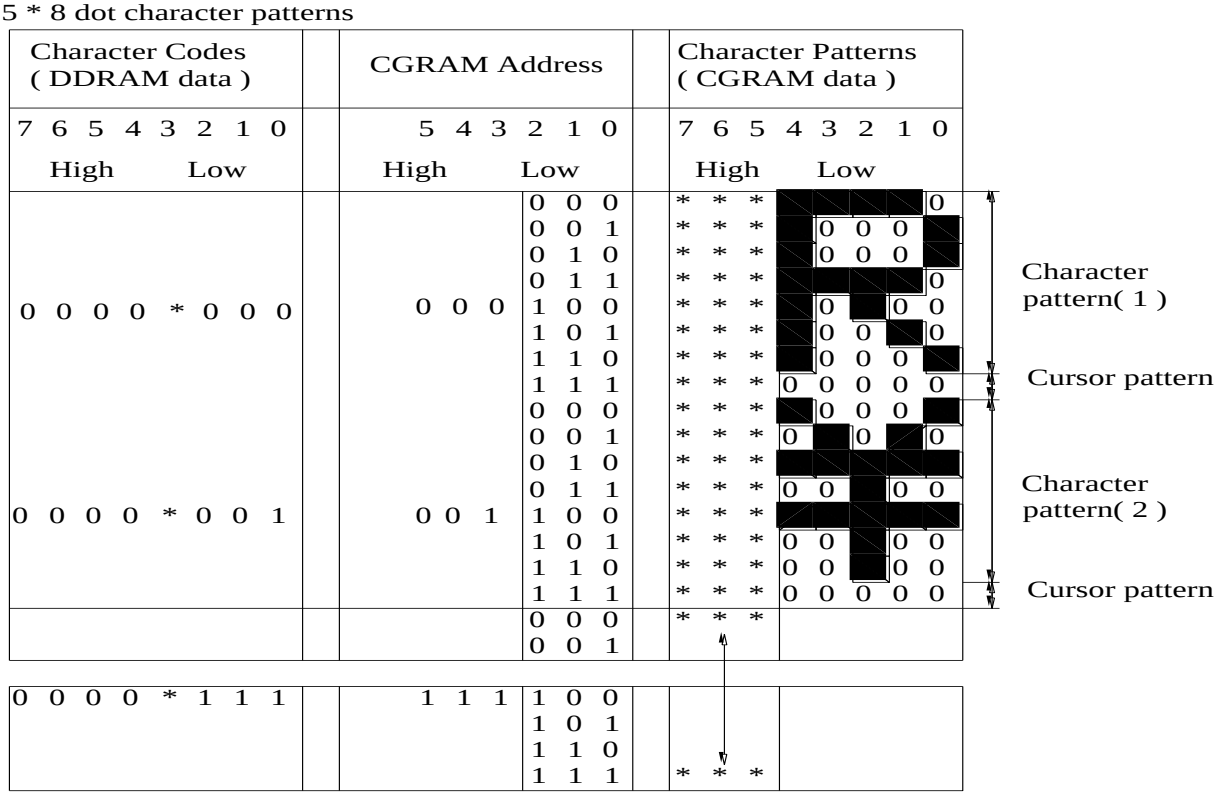
In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns can be written, and for 5×10 dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

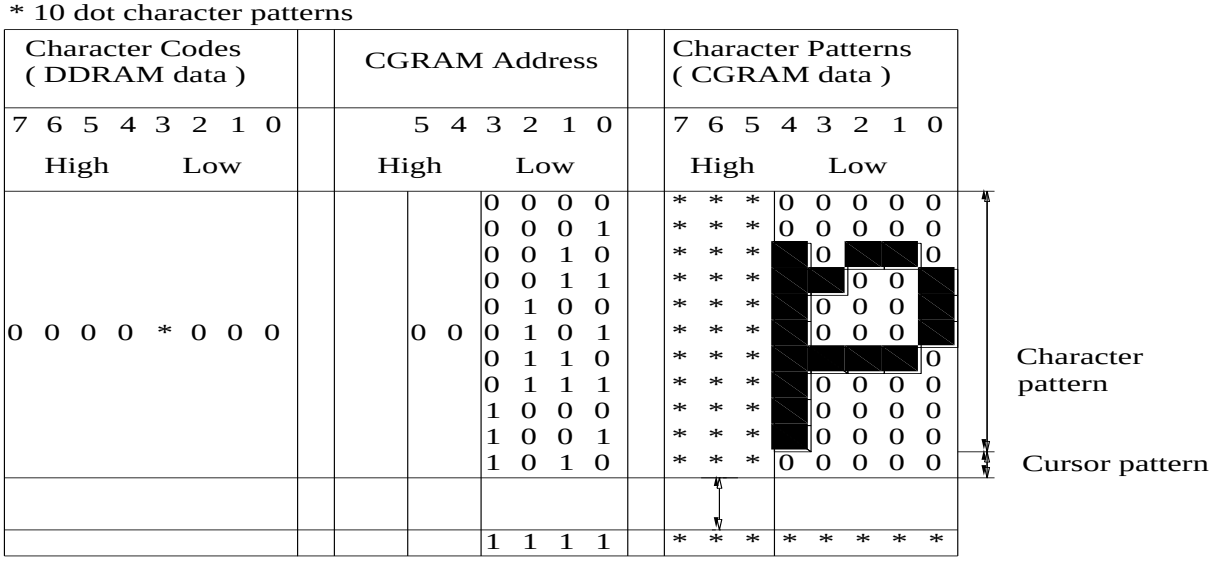
Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns

Table 1.

For 5 * 8 dot character patterns



For 5 * 10 dot character patterns



: " High "

10. Character Generator ROM Pattern

Table.2

RW1063 Font table (0A-001)

b7~4 / b3~0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM [00]															
0001	CG RAM [01]															
0010	CG RAM [02]															
0011	CG RAM [03]															
0100	CG RAM [04]															
0101	CG RAM [05]															
0110	CG RAM [06]															
0111	CG RAM [07]															
1000	CG RAM [00]															
1001	CG RAM [01]															
1010	CG RAM [02]															
1011	CG RAM [03]															
1100	CG RAM [04]															
1101	CG RAM [05]															
1110	CG RAM [06]															
1111	CG RAM [07]															

11. Instruction Table

◆ **INSTRUCTION DESCRIPTION**

Instruction Table:

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Description Time (540KHz)
Read display data	1	1	Read data								Read data from DDRAM/CGRAM	18.5us
Write display data	1	0	Write data								Write data into DDRAM/CGRAM	18.5us
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM, and set DDRAM address to "00H" from AC	0.76ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	0.76ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and specify display shift. These operations are performed during data read and write. I/D="1": increment I/D="0": decrement	18.5us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Set Display /Cursor/Blink On/OFF D="1": display on D="0": display off C="1": cursor on C="0": cursor off B="1": blink on B="0": blink off	18.5us
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	X	X	Cursor or display shift S/C="1": display shift S/C="0": cursor shift R/L="1": shift to right R/L="0": shift to left	18.5us
Function Set	0	0	0	0	1	DL	N	F	X	X	Set Interface Data Length DL= 8-bit interface/ 4-bit interface N = 2-line/1-line display F= 5x8 Font Size / 5x11Font Size	18.5us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	18.5us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	18.5us
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Can know internal operation is ready or not by reading BF. The contents of address counter can also be read. BF="1": busy state BF="0": ready state	0us

Note : 1. When an MPU program with Busy Flag(DB7) checking is made, 1/ 2 FOSC (is necessary) for executing the next instruction by the " E " signal after the Busy Flag (DB7) goes to " Low ".

2. "X" Don't care

12. Interface with MPU

The module is IIC interface

■ **For serial interface data, bus lines (DB5(CSB)、DB6(SDA) and DB7(SCL)) are used. IIC interface**

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.
The IIC Interface is for bi-directional, two-line communication between different ICs or modules. Serial data line SDA (DB6) and a Serial clock line SCL (DB7) must be connected to a positive supply via a pull-up resistor.
Data transfer may be initiated only when the bus is not busy.
*The CSB (DB5) Pin must be setting to "VSS".
* When IIC interface is selected, the DL register must be set to "1".

➢ **BIT TRANSFER**

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.9.1

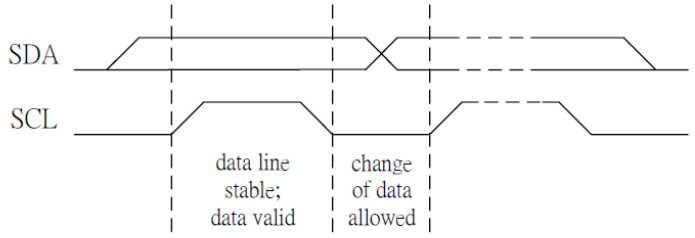


Fig .9.1 Bit transfer

➢ **START AND STOP CONDITIONS**

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.9.2

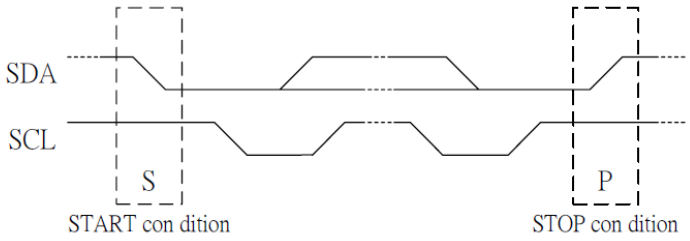


Fig .9.2 Definition of START and STOP conditions

➢ SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.9.3
· Transmitter: the device, which sends the data to the bus
· Receiver: the device, which receives the data from the bus
· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
· Slave: the device addressed by a master
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

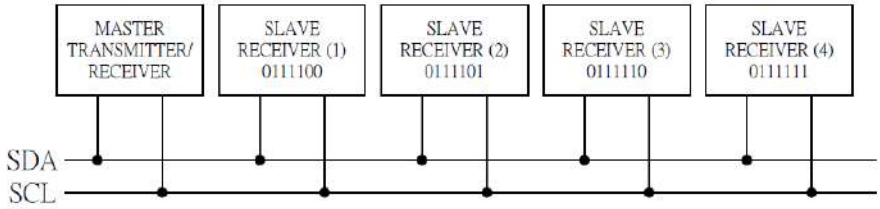


Fig .9.3 System configuration

➢ ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an Acknowledge after the reception of each byte. A master receiver must also generate an Acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the Acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an Acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Fig.9.4

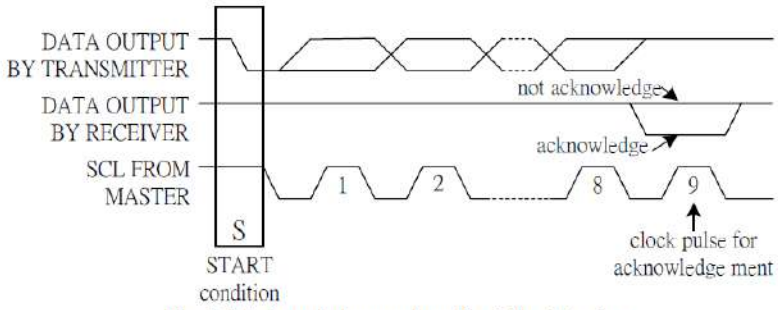
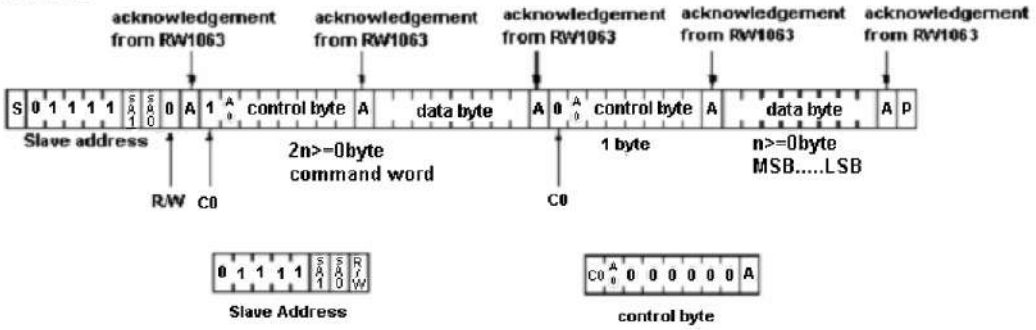


Fig .9.4 Acknowledgement on the 2-line Interface

➢ IIC Interface protocol

The RW1063 supports command, data write addressed slaves on the bus.
Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first.
Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the RW1063. The least significant bit of the slave address is set by connecting the input SA0 (DB0) and SA1 (DB1) to either logic 0 (VSS) or logic 1 (VDD).
The IIC Interface protocol is illustrated in Figure.9.5
The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended RW1063 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC interface-bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

Write Mode



"R/W always "0":RW1063 can only slave receiver

Fig .9.5 2-line Interface protocol

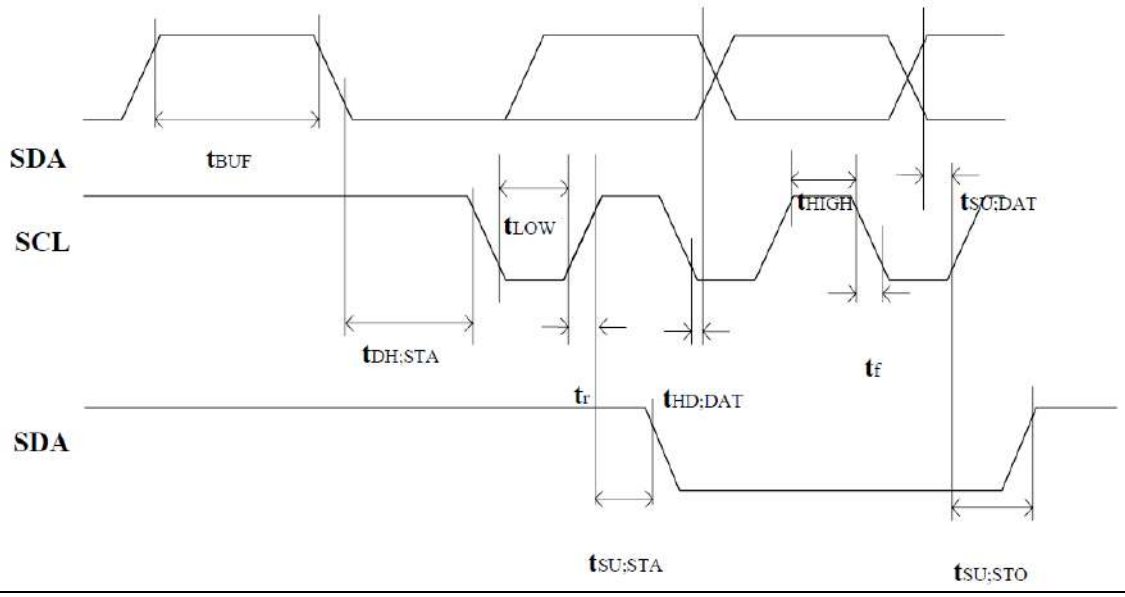
Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

Slave Address Option:

J7	J8	J9	J10	SA1	SA0	Address in Hex(R/W=0)	Address in Hex(without R/W=0) using <Wire.h> in arduino
	short		short	0	0	0X78(default setting)	0X3C(default setting)
	short	short		0	1	0X7A	0X3D
short			short	1	0	0X7C	0X3E
short		short		1	1	0X7E	0X3F

DB5(CSB)is connected to Vss by short J6.

◆ IIC interface timing

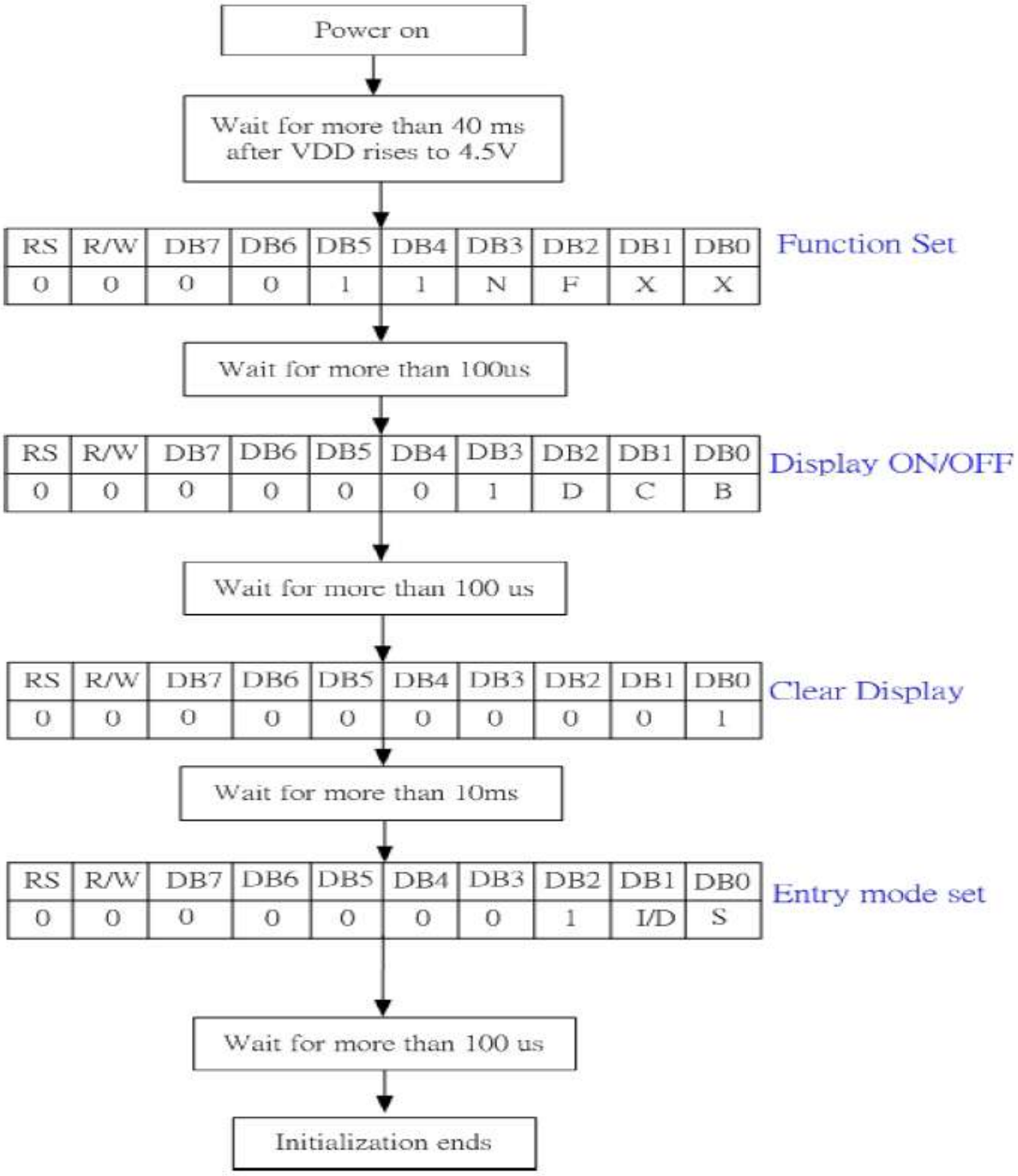


(Ta = 25°C)

Item	Signal	Symbol	Condition	VDD=2.7V		VDD=5V		Units
				Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}	—	DC	400	DC	400	KHz
SCL clock low period		t_{LOW}		1.3	—	1.3	—	us
SCL clock high period		t_{HIGH}		0.6	–	0.6	–	
Data set-up time	SDA	$t_{SU;DAT}$	—	180	–	80	–	ns
Data hold time		$t_{HD;DAT}$		0	0.9	0	0.9	us
SCL,SDA rise time	SCL, SDA	t_r	—	20+0.1C_b	300	20+0.1C_b	300	ns
SCL,SDA fall time		t_f		20+0.1C_b	300	20+0.1C_b	300	
Capacitive load represent by each bus line		C_b	—	–	400	–	400	pf
Setup time for a repeated START condition	SDA	$t_{SU;STA}$	—	0.6	–	0.6	–	us
Start condition hold time		$t_{HD;STA}$	—	0.6	–	0.6	–	us
Setup time for STOP condition		$t_{SU;STO}$	—	0.6	–	0.6	–	us
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	–	1.3	–	us

13.Initializing of LCM

- **Serial Interfaceode(Fosc=540KHz)**



Initial Code:

```
void WriteData(BYTE byData)
{
    I2C_Start();
    I2C_Send(0x78);
    I2C_Ack();
    I2C_Send(0x40);
    I2C_Ack();
    I2C_Send(byData);
    I2C_Ack();
    I2C_Stop();
}

void WriteInst(BYTE byInst)
{
    I2C_Start();
    I2C_Send(0x78);
    I2C_Ack();
    I2C_Send(0x00);
    I2C_Ack();
    I2C_Send(byInst);
    I2C_Ack();
    I2C_Stop();
}

void InitRW1063(void)
{
    WriteInst (0x38);    //DL=1: 8 bits; N=1: 2 line; F=0: 5 x 8dots
    WriteInst (0x0c);    // D=1, display on; C=B=0; cursor off; blinking off;
    WriteInst (0x06);    // I/D=1: Increment by 1; S=0: No shift
}
```

14.Quality Assurance

Screen Cosmetic Criteria

Item	Defect	Judgment Criterion	Partition
1	Spots	A)Clear Size: d mm — Acceptable Qty in active area d ≦0.1 — Disregard 0.1<d≦0.2 — 6 0.2<d≦0.3 — 2 0.3<d — 0 Note: Including pin holes and defective dots which must be within one pixel size. B)Unclear Size: d mm — Acceptable Qty in active area d ≦0.2 — Disregard 0.2<d≦0.5 — 6 0.5<d≦0.7 — 2 0.7<d — 0	Minor
2	Bubbles in Polarizer	Size: d mm — Acceptable Qty in active area d≦0.3 — Disregard 0.3<d≦1.0 — 3 1.0<d≦1.5 — 1 1.5<d — 0	Minor
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor

15.Reliability

Content of Reliability Test

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Applicable Standard**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 96hrs	____
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30℃ 96hrs	____
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 96hrs	____
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 96hrs	____
High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60℃,90%RH 96hrs	____
High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	60℃,90%RH 96hrs	____
Temperature Cycle	Endurance test applying the low and high temperature cycle. -30℃ 25℃ 80℃  30min 5min 30min 1 cycle	-30℃→80℃ 10 cycles	____
Mechanical Test			
Vibration test	Endurance test applying the vibration during transportation and using.	50Hz→3mm p-p Total 0.5hrs	____

***Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25℃