天鈺科技股份有限公司

Fitipower Integrated Technology Inc.

JD9852

Data Sheet

240RGB x 320 dot, 262K color,
with internal GRAM, a-Si TFT LCD Single Chip Driver

Preliminary Version 0.00
2018/12/10

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1. Revision History

Version	Date	Description of modification
0.00	2018/11/19	New setup

2. Introduction

The JD9852 is a 262,144-color single-chip SOC driver for a-Si TFT liquid crystal display with resolution of 240RGBx320dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

The JD9852 supports MIPI-DSI interface, parallel 8-/9-/16-/18-bit data bus MCU interface, 3-/4-line serial peripheral interface (SPI) and 2 lane SPI data transmission. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

The JD9852 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. JD9852 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the JD9852 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

3. Features

- Display resolution: 240xRGB(H) x 320(V)
- LCD Driver Output:
  - 720 source channels
  - 320 gate channels
- Frame Memory Size: 240 x 320 x 18-bit = 1382400 bits
- System Interface
  - MIPI-DSI (Display Serial Interface) interface
  - Parallel 8080-series MCU Interface (8-bits, 9-bits, 16-bits, 18-bits)
  - Serial Peripheral Interface (SPI) (8-bits, 9-bits and 2 data lane SPI)
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color
  - Reduce color mode (Idle mode ON): 8-color
- Pixel Color Format (Color Depth)
  - 12-bit/pixel: RGB=(444)
  - 16-bit/pixel: RGB=(565)
  - 18-bit/pixel: RGB=(666)
- On chip functions:
  - DC/DC converter
  - Timing generator
  - Internal Oscillator generation
  - OTP memory to store initialization register settings
  - Support CABC (Content Adaptive Brightness Control) function
- Display inversion type support
  - Dot Inversion
  - Column Inversion
- Wide Supply Voltage Range
  - IOVCC = 1.65V ~ 3.3V (logic)
  - VCI = 2.6V ~ 3.3V (analog)
- On-Chip Power System:
  - Source Voltage: +6.4~ -4.6V
  - Gate driver output voltage
    - VGH - GND = 12.0V ~ 16.0V
    - VGL - GND = -7.0V ~ -12.0V

4. Device Overview

4.1. Block Diagram

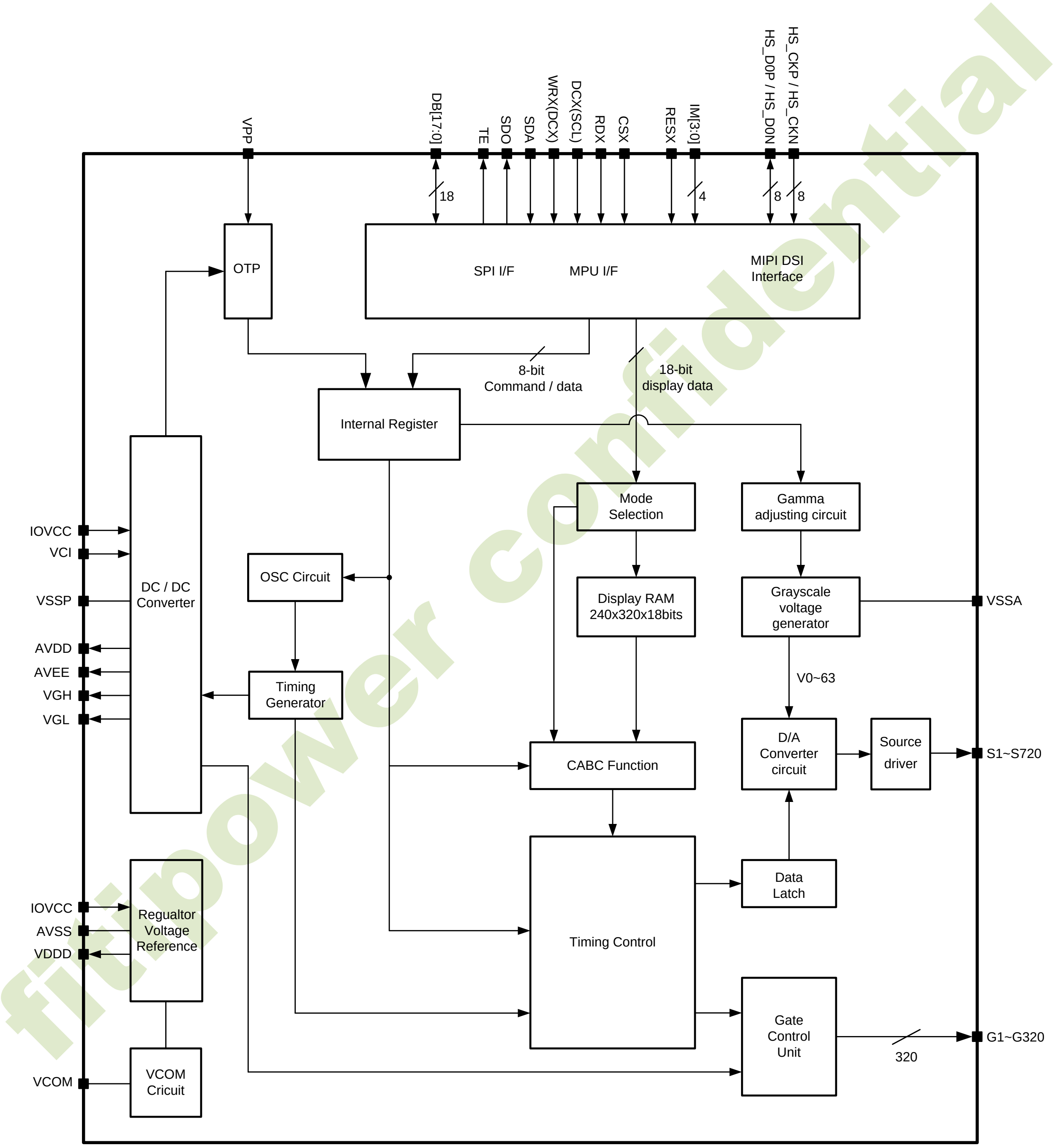


Figure. 4.1 Block Diagram

4.2. LCD power generation scheme

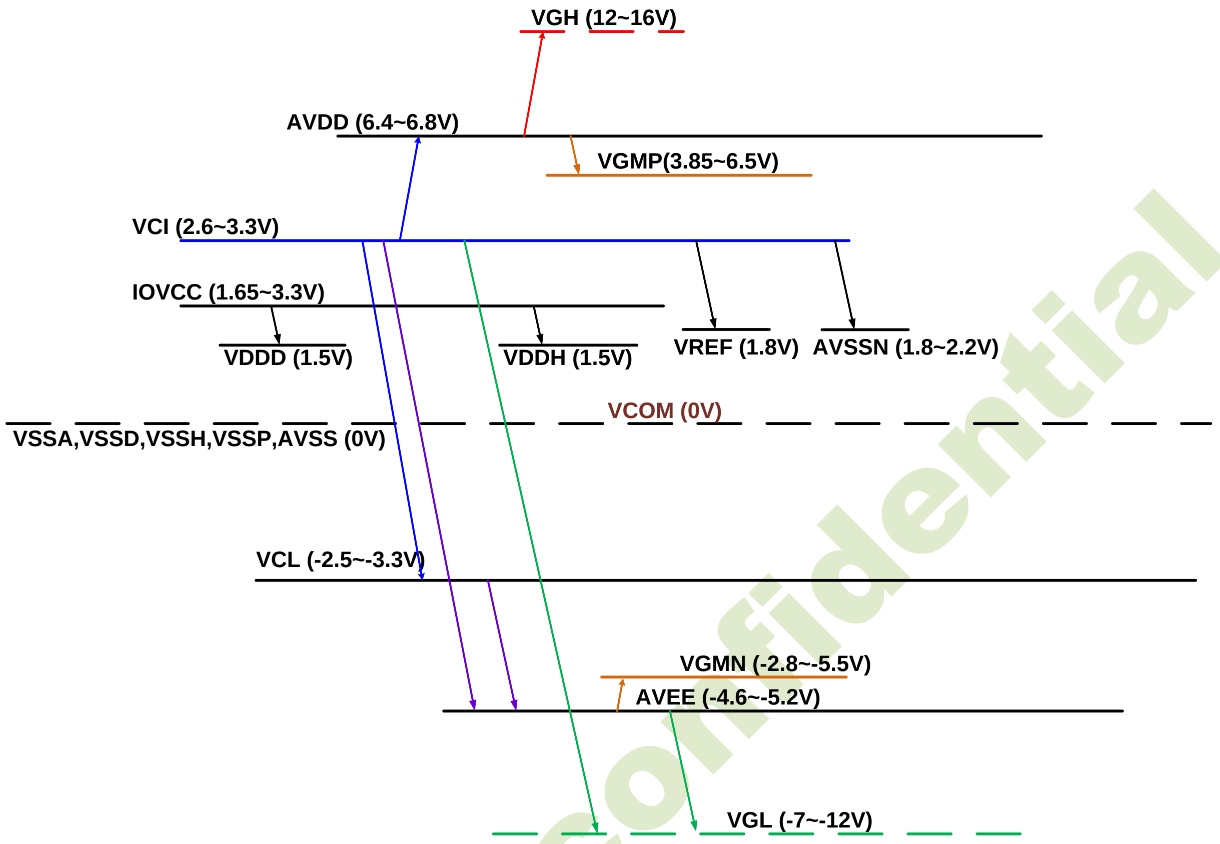


Figure. 4.2 LCD power generation scheme

4.3. Output voltage range

JD9852 generates corresponding voltage with a-Si TFT LCD panel by internal power supply circuit. Please set up each voltage output according to the LCD panel.

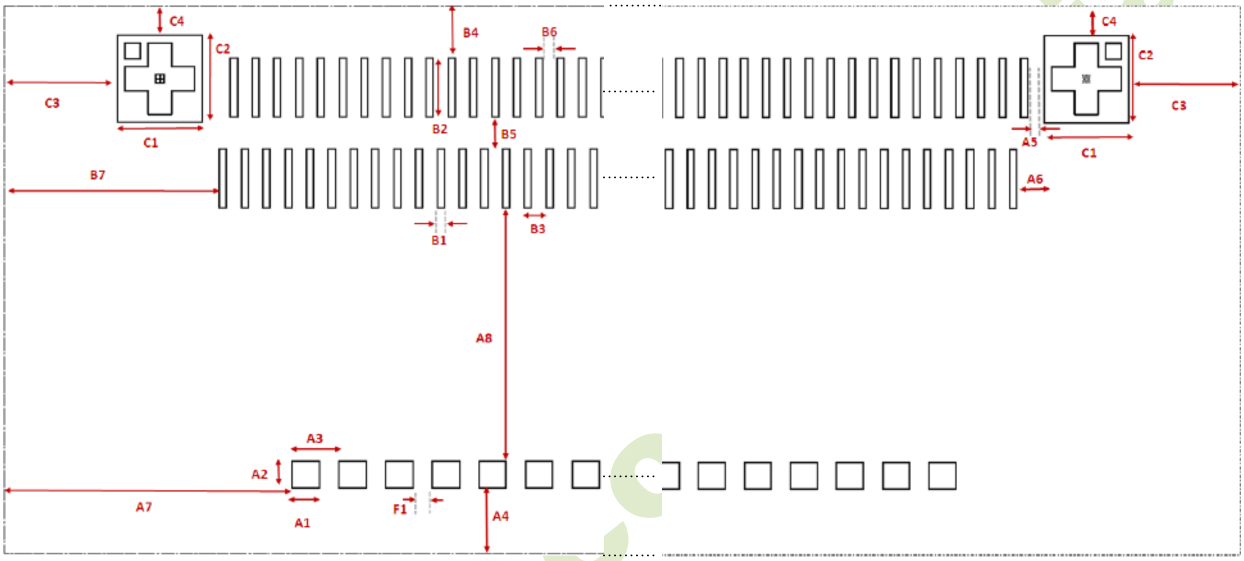
Name	Function	Set up value	Note
AVDD	DC/DC converter circuit output	+6.4~ +6.8V	Do not exceed 6.8V
AVEE	DC/DC converter circuit output	-4.6~ -5.2V	Do not exceed -5.2V
VGMP	Reference voltage for gamma circuit	+3.85V~ +6.5V	Reference register
VGMN	Reference voltage for gamma circuit	-2.8V~ -5.5V	Reference register
VGH	Positive gate driver output voltage level	+12~ +16V	Depend on AVDD & AVEE
VGL	Negative gate driver output voltage level	-7V ~ -12V	Depend on AVDD & AVEE
VCOM	VCOM DC voltage	-3.3~ 0V	-
VDDD	Digital power.	+1.5V	-
VDDH	Analog power.	+1.5V	-

5. Pad Arrangement

5.1. PAD assignment

Chip Size: 15360um * 727um

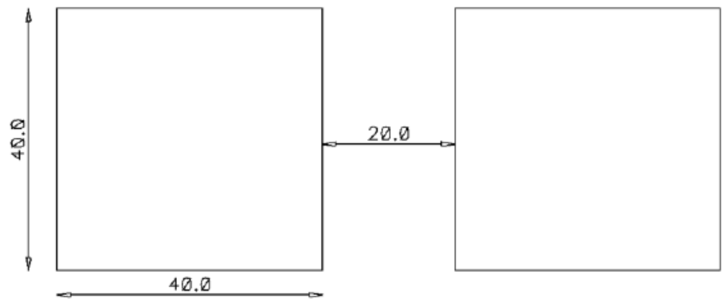
Overview (Simple view)



Condition-1 (+/- 3um temp. compensation)			Unit=um											
INPUT PAD			INPUT PAD Special			OUTPUT PAD			AMARK					
Symbol	Size	Number	Symbol	Size	Number	Symbol	Size	Number	Symbo	Size	Symbo	Size	Symbo	Size
A1	40	No.1~232	F1	20	No.1~232	B1	14	No.233~1278	C1	120				
A2	40					B2	74		C2	120				
A3	60					B3	28		C3	140				
A4	58.88					B4	105.92		C4	71.9				
A5	14					B5	40							
A6	28					B6	14							
A7	367.5					B7	274							
A8	334.2													

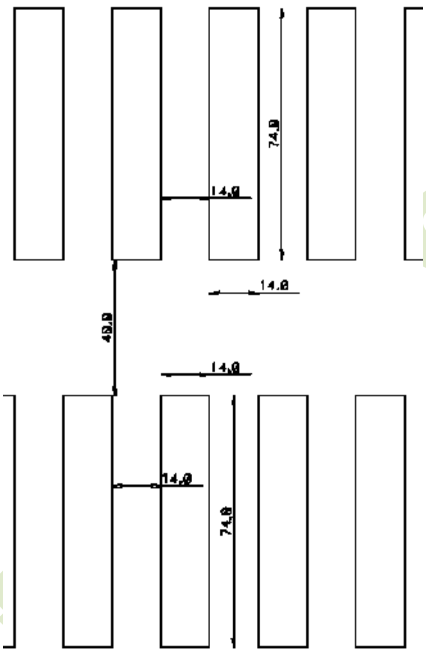
5.2. Input and Output Bump Dimension

5.2.1. Input Pad



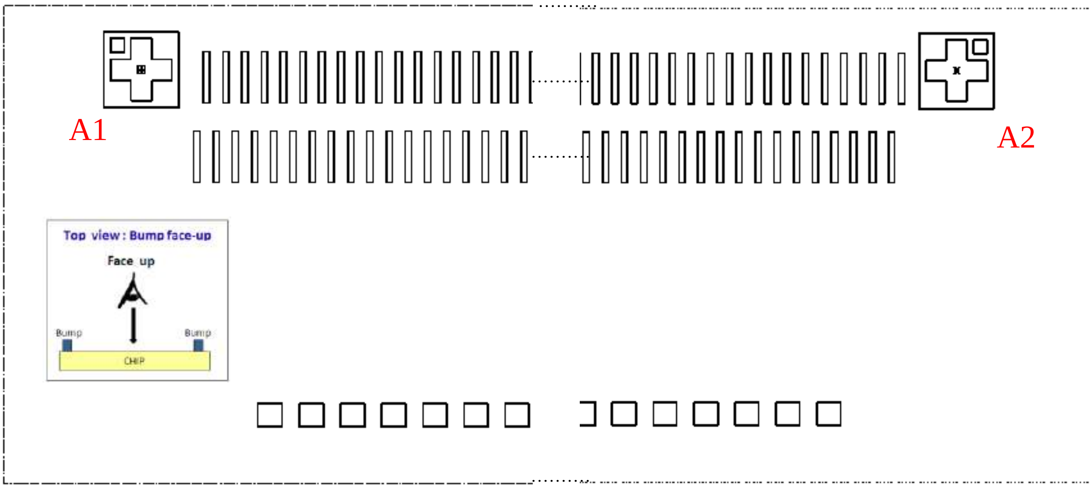
Unit: um

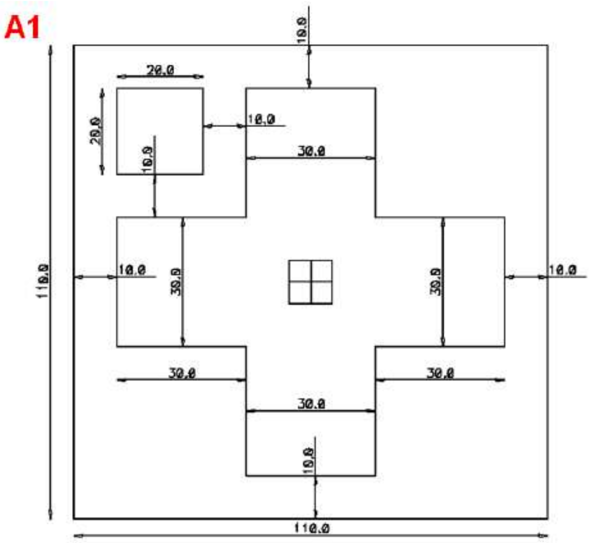
5.2.2. Output Pad

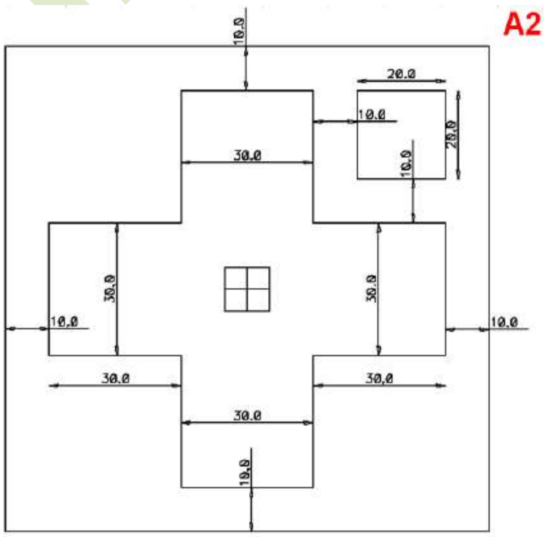


Unit: um

5.3. Alignment Mark Dimension







6. Pin Description

6.1. Power Supply Pins

Pin Name	I/O	Type	Descriptions
IOVCC	I	Digital Power	Power supply for interface logic circuits(1.65~3.3V)
VCI	I	Analog Power	Power supply for analog circuit blocks(2.6~3.3V)
VPP	I	OTP Power	External high voltage pin used in OTP mode and operates at 8.3V. If not used, let this pin open.
VSSA/AVSS/VSSP	I	Analog Ground	System ground level for analog circuit blocks. Connect to VSSA on the FPC to prevent noise.
VSSD/VSSH	I	Digital Ground	System ground level for Digital circuit blocks. Connect to VSSD on the FPC to prevent noise.

6.2. Interface Logic Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>(IOVCC/GND)</td><td>-Select the MCU interface mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MCU-Interface</th><th>Data Pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 8-bit parallel Interface I</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 16-bit parallel Interface I</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 9-bit parallel Interface I</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 18-bit parallel Interface I</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>MIPI-DSI interface</td><td>HS_CKP/CKN
HS_D0P/D0N</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-line 9-bit serial interface I</td><td>SDA: in/out</td></tr>
<tr><td>2 data lane serial interface</td><td>SDA: in/out
WRX: in</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-line 8-bit serial interface I</td><td>SDA: in/out</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8080 16-bit parallel Interface II</td><td>DB[17:10],
DB[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8080 8-bit parallel Interface II</td><td>DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8080 18-bit parallel Interface II</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8080 9-bit parallel Interface II</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-line 9-bit serial interface I</td><td>SDA: in/
SDO: out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-line 8-bit serial interface II</td><td>SDA:in/
SDO: out</td></tr>
</table>
MPU Parallel interface bus and serial interface select.</td></tr>
<tr><td>RESX</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>-This signal will reset the device and must be applied to properly initialize the chip.
-Signal is active low.</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>-Chip select input pin.
Low enable.
High disable.</td></tr>
<tr><td>DCX_SCL</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>-Data/command selection pin in parallel interface.
When DCX='1', data is selected.
When DCX='0', command is selected.
-This pin is used to be serial interface clock.
-If not used, this pin should be connected to IOVCC or GND.</td></tr>
<tr><td>RDX</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>-Read enable in 8080 MCU parallel interface.
-Fix to IOVCC level when not in use</td></tr>
<tr><td>WRX</td><td>I</td><td>MCU
(IOVCC/ GND)</td><td>-Write enable in MCU parallel interface.
-Data/command selection pin in 4-line serial interface.
-Second Data lane in 2 data lane serial interface.</td></tr>
</table>

			-Fix to IOVCC level when not in use.
DB[17:0]	I/O	MCU (IOVCC/ GND)	-DB[17:0] are used as MCU parallel interface data bus. -Fix to IOVCC or GND when not in use
SDA	I/O	MCU (IOVCC/ GND)	-When IM[3]:Low, Serial in/out signal in SPI interface. -When IM[3]:High, Serial input signal in SPI interface. -The data is latched on the rising edge of the SCL signal. -If not used, fix this pin at IOVCC or GND.
SDO	O	MCU (IOVCC/GND)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (IOVCC/ GND)	Tearing effect output pin to synchronize MPU to frame writing. If not used, open this pin.
HS_CKP HS_CKN	I	DSI Host	MIPI-DSI CLOCK differential signal input pins. When IM[3:0] = 2'b0100, HS_CKP is shared input pad with DB[3:0] HS_CKN is shared input pad with DB[7:4] if not used , Please connected to VSSH or open.
HS_D0P HS_D0N	I/O	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 0) When IM[3:0] = 2'b0100, HS_D0P is shared input/output pad with DB[11:8] HS_D0N is shared input/output pad with DB[15:12] if not used , Please connected to VSSH or .open

Note1. When CSX='1', there is no influence to the parallel and serial interface.

6.3. Driver Output Pins

Pin Name	I/O	Descriptions
S1~ S720	O	Source output signals.. Leave the pin to open when not in use.
G1~ G320	O	Gate output signals. Leave the pin to open when not in use.
AVDD	O	Analog positive power.
AVEE	O	Analog negative power.
VGH	O	Power supply for the gate driver (Positive).
VGL	O	Power supply for the gate driver (Negative).
VCOM	O	A power supply for the TFT-LCD common electrode.
VDDD	O	Digital power.
VDDH	O	Analog power.
VREF	O	internal reference voltage
VCL	O	DC/DC converter circuit output.
VGMP	O	Reference voltage for gamma circuit.
VGMN	O	Reference voltage for gamma circuit.
LEDPWM	O	Output pin for PWM(Pulse width Modulation) signal of LED driving. If not used,open this pad.
LEDON	O	-Output pad for enabling LED. -If not used, keep it open.

7. Interface setting

7.1. DSI system interfaces

The JD9852 supports DSI (Display Serial Interface). The IM[3:0] pins setting are fixed as "0100".

The Display Serial Interface (DSI) specifies the interface between a host processor and a peripheral. DSI builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DCS standards.

Figure 7.1 shows a simplified DSI interface. DSI sends display data or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals.

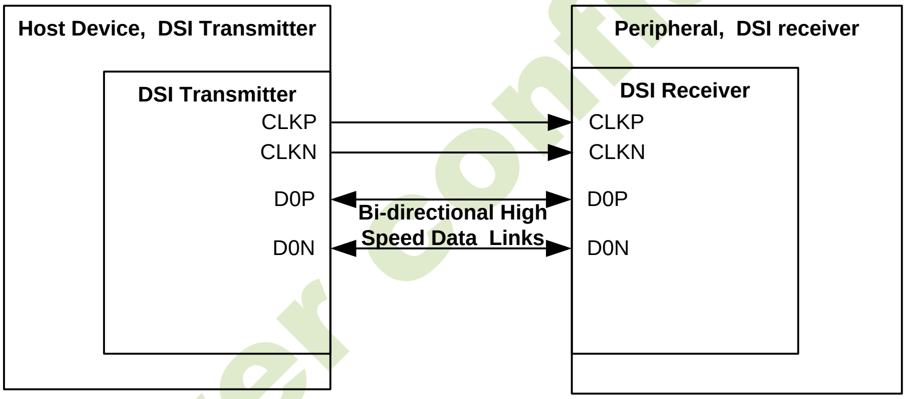


Figure. 7.1 DSI transmitter and receiver interface

A conceptual vide of DSI organizes the interface into several functional layers. A description of the layers follows and is also shown below.

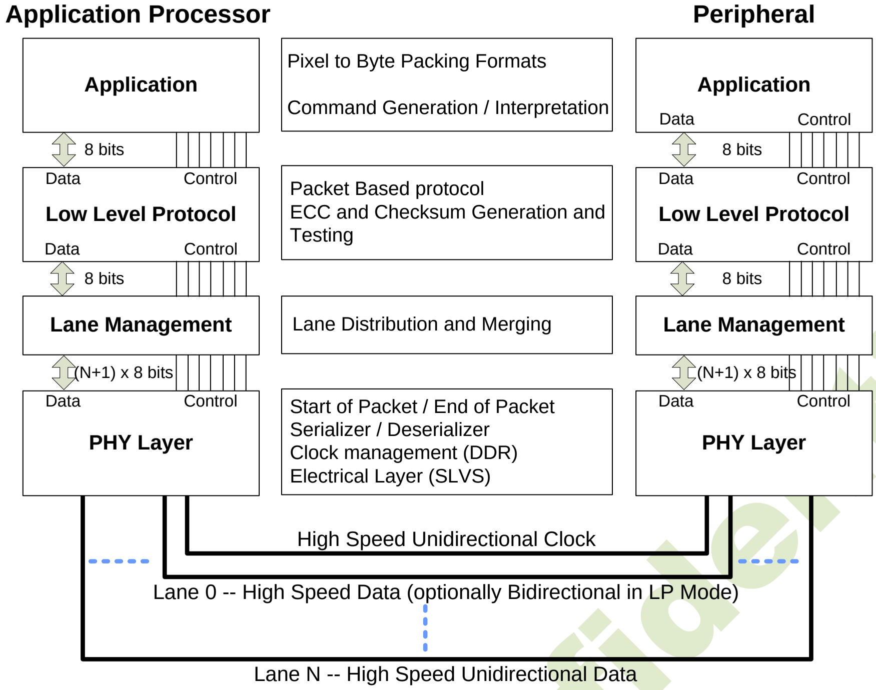


Figure. 7.2 DSI Layer

PHY Layer: The PHY Layer specifies transmission medium (electrical conductors), the input/output circuitry and the clocking mechanism that captures "ones" and "zeroes" from the serial bit stream. Bit-level and byte-level synchronization mechanisms are included as part of the PHY.

Lane Management Layer: DSI is Lane-scalable for increased performance. The number of data signals may be 1 or 2 depending on the bandwidth requirements of the application. The transmitter side of the interface distributes the outgoing data stream to one or more Lanes ("distributor" function). On the receiving end, the interface collects bytes from the Lanes and merges them together into a recombined data stream that restores the original stream sequence ("merger" function).

Protocol Layer: At the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets. The protocol defines required headers for each packet, and how header information is generated and interpreted. The transmitting side of the interface appends header and error-checking information to data being transmitted. On the receiving side, the header is stripped off and interpreted by corresponding logic in the receiver. Error-checking information may be used to test the integrity of incoming data. DSI protocol also documents how packets may be tagged for interleaving multiple command or data streams to separate destinations using a single DSI.

Application Layer: This layer describes higher-level encoding and interpretation of data contained in the data stream. Depending on the display subsystem architecture, it may consist of pixels having a prescribed format, or of commands that are interpreted by the display controller inside a display module. The DSI specification describes the mapping of pixel values, commands and command parameters to bytes in the packet assembly.

7.1.1. Command mode, Video mode and Virtual Channel

DSI-compliant peripheral support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

Video Mode

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Virtual Channel Capability

While this specification only addresses the connection of a host processor to a single peripheral, DSI incorporates a virtual channel capability for communication between a host processor and multiple, physical display modules. Since interface bandwidth is shared between peripherals, there are constraints that limit the physical extent and performance of multiple-peripheral systems. The DSI protocol permits up to four virtual channels, enabling traffic for multiple peripherals to share a common DSI Link. The DSI specification makes no requirements on the specific value assigned to each virtual channel used to designate interlaced fields, For clarity, the first interlaced video field may be assigned as DI[7:6] = 2'b00 and the second interlaced video field may be assigned DI[7:6] = 2'b01.

Note1: JD9852 support video mode.

Note2: For JD9161, DI[7:6] for virtual channel should be set as 2'b00

7.1.2. Power-up Sequence Example

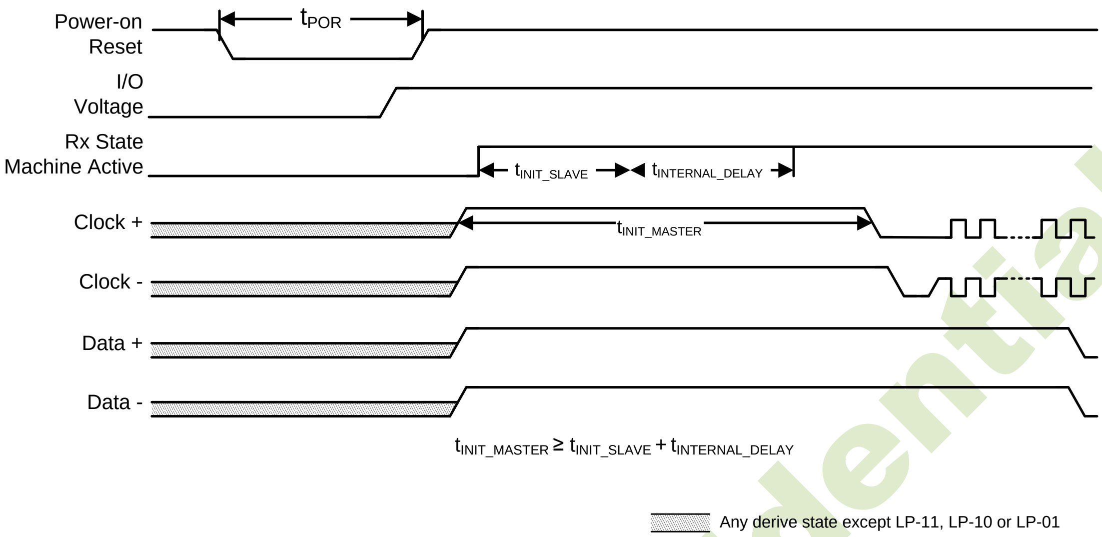


Figure. 7.3 Peripheral Power-Up Sequencing Example

7.1.3. DSI Format

Information is transferred between host processor and peripheral using one or more serial data signals and accompanying serial clock. The action of sending high-speed serial data across the bus is called a HS transmission or burst. Between transmissions, the differential data signal or Lane goes to a low-power state (LPS). Interfaces should be in LPS when they are not actively transmitting or receiving high-speed data. Figure 7.4 shows the basic structure of a HS transmission. N is the total number of bytes sent in the transmission.

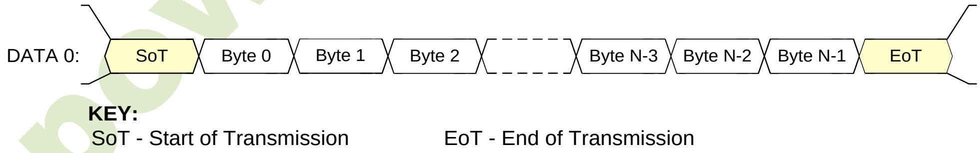


Figure. 7.4 Basic HS Transmission Structure

7.1.4. DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted in the Protocol layer to packets, following the packet organization documented in this section. The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY.

7.1.4.1. Multiple Packets per Transmission

In its simplest form, a transmission may contain one packet. If many packets are to be transmitted, the overhead of frequent switching between LPS and High-Speed Mode will severely limit bandwidth if packets are sent separately, e.g. one packet per transmission.

The DSI protocol permits multiple packets to be concatenated, which substantially boosts effective bandwidth. This is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup.

There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS transmission can be started, the transmitter PHY issues a SoT sequence to the receiver. After that, data or command packets can be transmitted in HS mode. Multiple packets may exist within a single HS transmission and the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. In order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp can be enabled or disabled. The method of enabling or disabling this capability is out of scope for this document.

The top diagram in Figure 7.5 illustrates a case where multiple packets are being sent separately with EoTp support disabled. In HS mode, time gaps between packets shall result in separate HS transmissions for each packet, with a SoT, LPS, and EoT issued by the PHY layer between packets. This constraint does not apply to LP transmissions. The bottom diagram in Figure 7.5 demonstrates a case where multiple packets are concatenated within a single HS transmission.

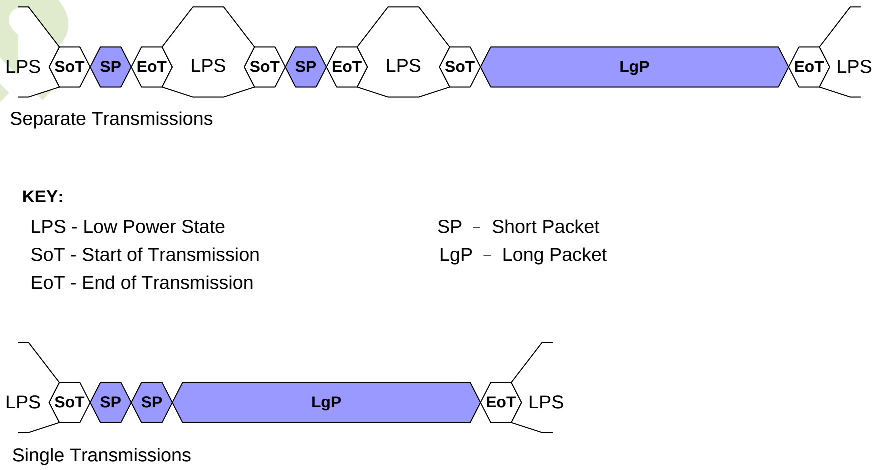


Figure. 7.5 HS Transmission Examples with EoTp disabled

Figure 7.6 depicts HS transmission cases where EoTp generation is enabled. In the figure, EoT short packets are highlighted in red. The top diagram illustrates a case where a host is intending to send a short packet followed by a long packet using two separate transmissions. In this case, an additional EoT short packet is generated before each transmission ends. This mechanism provides a more robust environment, at the expense of increased overhead (four extra bytes per transmission) compared to cases where EoTp generation is disabled, i.e. the system only relies on the PHY layer EoT sequence for signaling the end of HS transmission. The overhead imposed by enabling EoTp can be minimized by sending multiple long and short packets within a single transmission as illustrated by the bottom diagram in Figure 7.6.

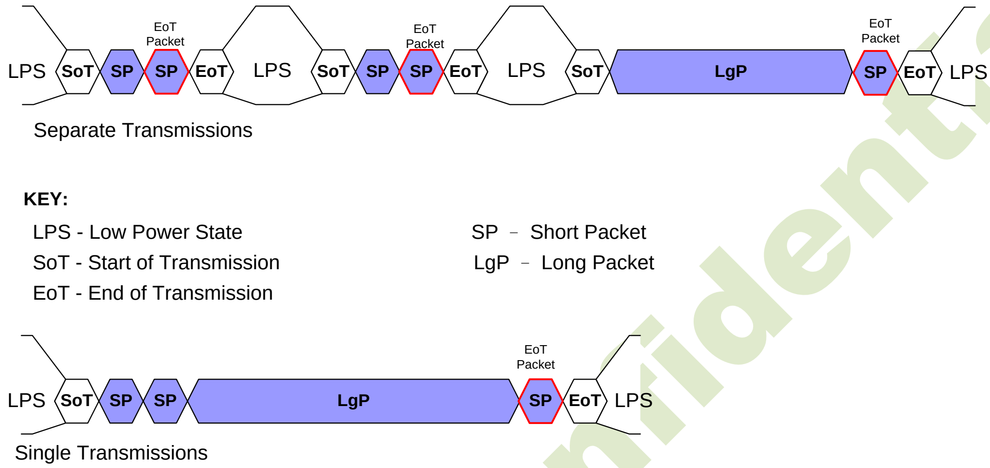


Figure. 7.6 HS Transmission Examples with EoTp enabled

7.1.4.2. Endian Policy

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. Figure 7.7 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

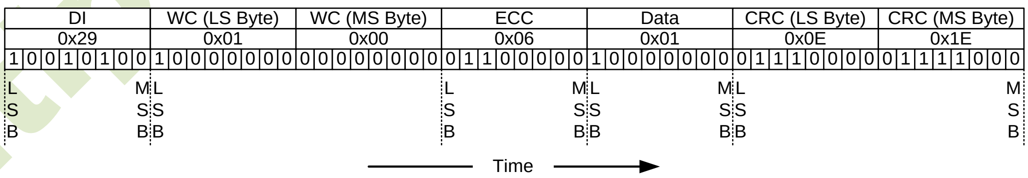


Figure. 7.7 Endian Example (Long Packet)

7.1.5. Packet Structure

The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. Packet sizes fall into two categories:

Long packets specify the payload length using a two-byte Word Count field. Payloads may be from 0 to 216- 1 bytes long. Therefore, a Long packet may be up to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.

Short packets are four bytes in length including the ECC. Short packets are used for most Command Mode commands and associated parameters. Other Short packets convey events like H Sync and V Sync edges. Because they are Short packets they can convey accurate timing information to logic at the peripheral.
The Set Maximum Return Packet Size command allows the host processor to limit the size of response packets coming from a peripheral.

7.1.5.1. Long Packet

Figure 7.8 shows the structure of the Long packet. A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

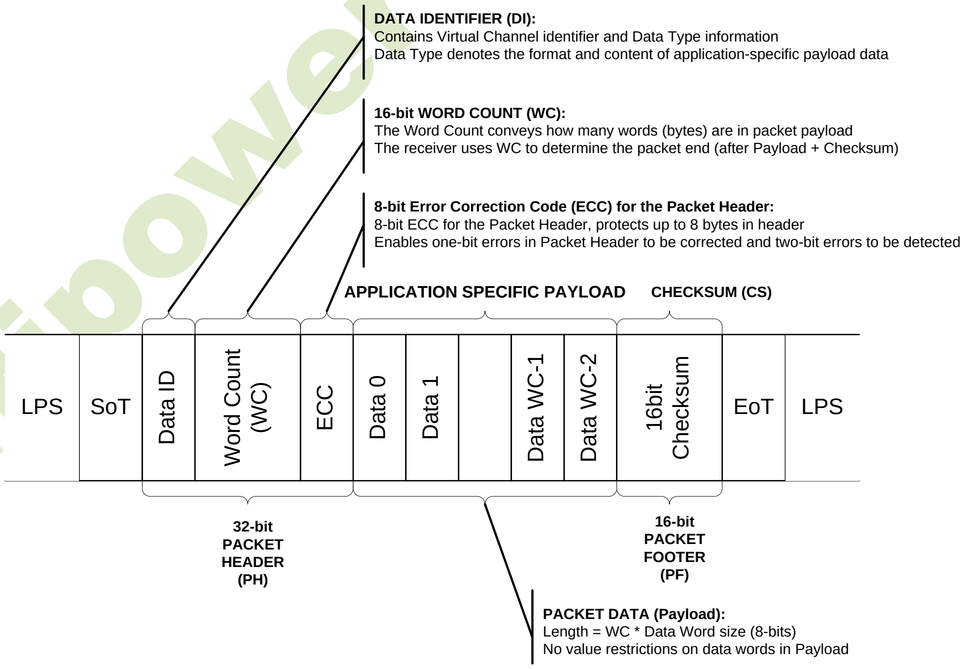


Figure. 7.8 Long Packet Structure

The Data Identifier defines the Virtual Channel for the data and the Data Type for the application specific payload data.

The Word Count defines the number of bytes in the Data Payload between the end of the Packet Header and the start of the Packet Footer. Neither the Packet Header nor the Packet Footer shall be included in the Word Count.

The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. This includes both the Data Identifier and Word Count fields.

After the end of the Packet Header, the receiver reads the next Word Count * bytes of the Data Payload. Within the Data Payload block, there are no limitations on the value of a data word, i.e. no embedded codes are used.

Once the receiver has read the Data Payload it reads the Checksum in the Packet Footer. The host processor shall always calculate and transmit a Checksum in the Packet Footer. Peripherals are not required to calculate a Checksum. Also note the special case of zero-byte Data Payload: if the payload has length 0, then the Checksum calculation results in (0xFFFF). If the Checksum is not calculated, the Packet Footer shall consist of two bytes of all zeros (0x0000). In the generic case, the length of the Data Payload shall be a multiple of bytes.

Each byte shall be transmitted least significant bit first. Payload data may be transmitted in any byte order restricted only by data format requirements. Multi-byte elements such as Word Count and Checksum shall be transmitted least significant byte first.

7.1.5.2. Short Packet

Figure 7.9 shows the structure of the Short packet. A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

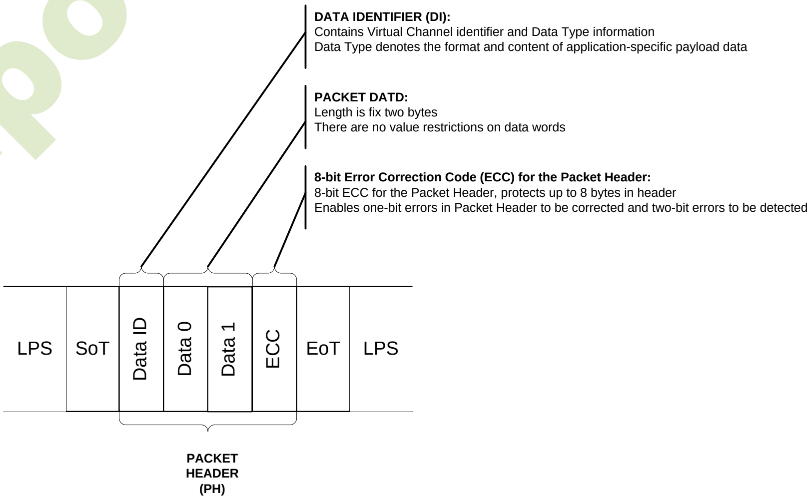


Figure. 7.9 Short Packet Structure

7.1.6. Common Packet Elements

Long and Short packets have several common elements that are described in this section

7.1.6.1. Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte. Figure 7.10 shows the composition of the Data Identifier (DI) byte. DI[7:6]: These two bits identify the data as directed to one of four virtual channels. DI[5:0]: These six bits specify the Data Type.

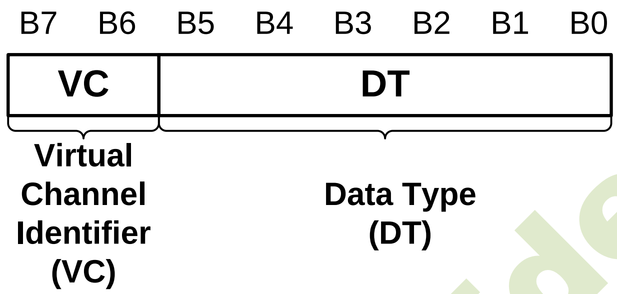


Figure. 7.10 Data Identifier Byte

7.1.6.2. Virtual Channel Identifier – VC field, DI[7:6]

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel.

7.1.6.3. Data Type Field DT[5:0]

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start / end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet. When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

7.1.6.4. ECC

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications.

7.1.7. DSI packet

7.1.7.1. Processor-sourced Packets

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in table 7.1.

Data Type (Hex)	Data Type (Binary)	Description	Packet Size
0x01	00 0001	Sync Event, V Sync Start	Short
0x11	01 0001	Sync Event, V Sync End	Short
0x21	10 0001	Sync Event, H Sync Start	Short
0x31	11 0001	Sync Event, H Sync End	Short
0x08	00 1000	End of Transmission packet (EoTp)	Short
0x02	00 0010	Color Mode (CM) Off Command	Short
0x12	01 0010	Color Mode (CM) On Command	Short
0x22	10 0010	Shut Down Peripheral Command	Short
0x32	11 0010	Turn On Peripheral Command	Short
0x03	00 0011	Generic Short WRITE, no parameters	Short
0x13	01 0011	Generic Short WRITE, 1 parameter	Short
0x23	10 0011	Generic Short WRITE, 2 parameters	Short
0x04	00 0100	Generic READ, no parameters	Short
0x14	01 0100	Generic READ, 1 parameter	Short
0x24	10 0100	Generic READ, 2 parameters	Short
0x05	00 0101	DCS Short WRITE, no parameters	Short
0x15	01 0101	DCS Short WRITE, 1 parameter	Short
0x06	00 0110	DCS READ, no parameters	Short
0x37	11 0111	Set Maximum Return Packet Size	Short
0x09	00 1001	Null Packet, no data	Long
0x19	01 1001	Blanking Packet, no data	Long
0x29	10 1001	Generic Long Write	Long
0x39	11 1001	DCS Long Write/write_LUT Command Packet	Long
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
0xX0 and 0xXF unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

Table 7.1 Data Types for supported Processor-sourced Packets

7.1.7.2. Pixel Stream, 16-bit Format, Long Packet

Packed Pixel Stream 16-Bit Format shown in Figure 7.11 is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Within a color component, the LSB is sent first, the MSB last. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

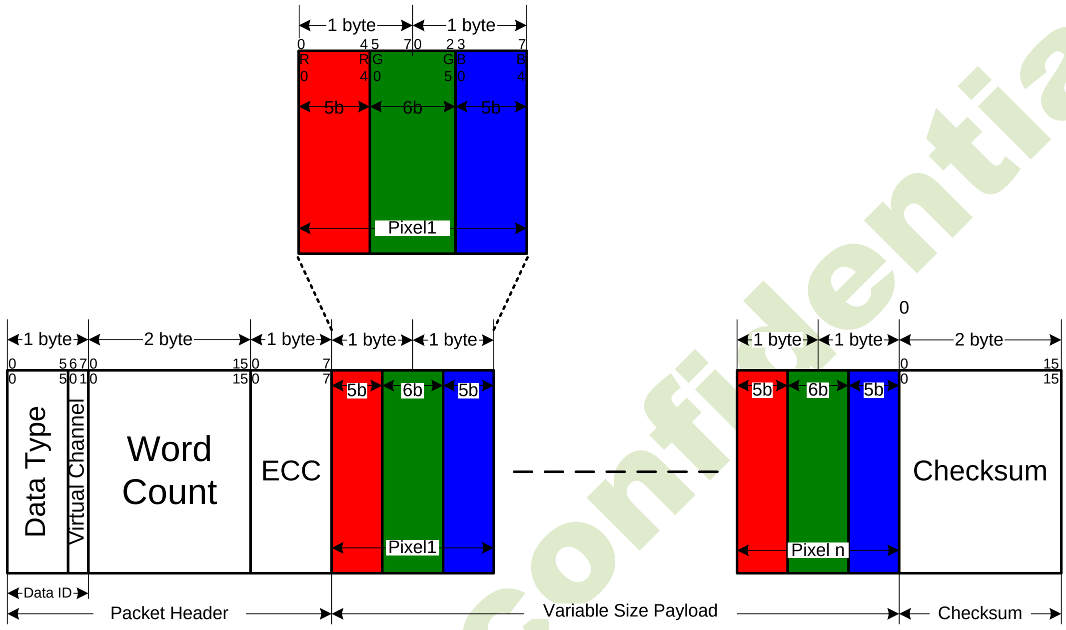


Figure. 7.11 16-bit/pixel – RGB Color Format, Long Packet

7.1.7.3. Pixel Stream, 18-bit Format, Long Packet

Packed Pixel Stream 18-Bit Format (Packed) shown in Figure 7.12 is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. Peripheral will not display the fill pixels when refreshing the display device.

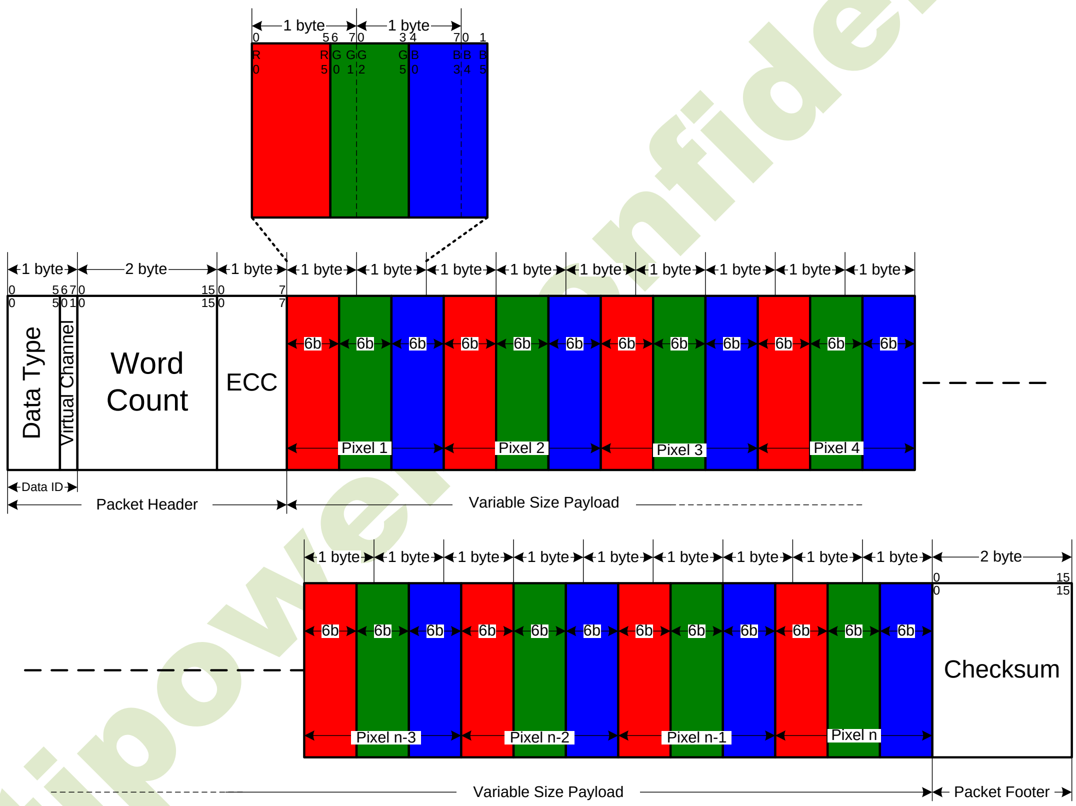


Figure. 7.12 18-bit /pixel (Packed) – RGB Color Format, Long Packet

7.1.7.4. Pixel Stream, 18-bit Loosely Format, Long Packet

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits, but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte as shown in Figure 7.13. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

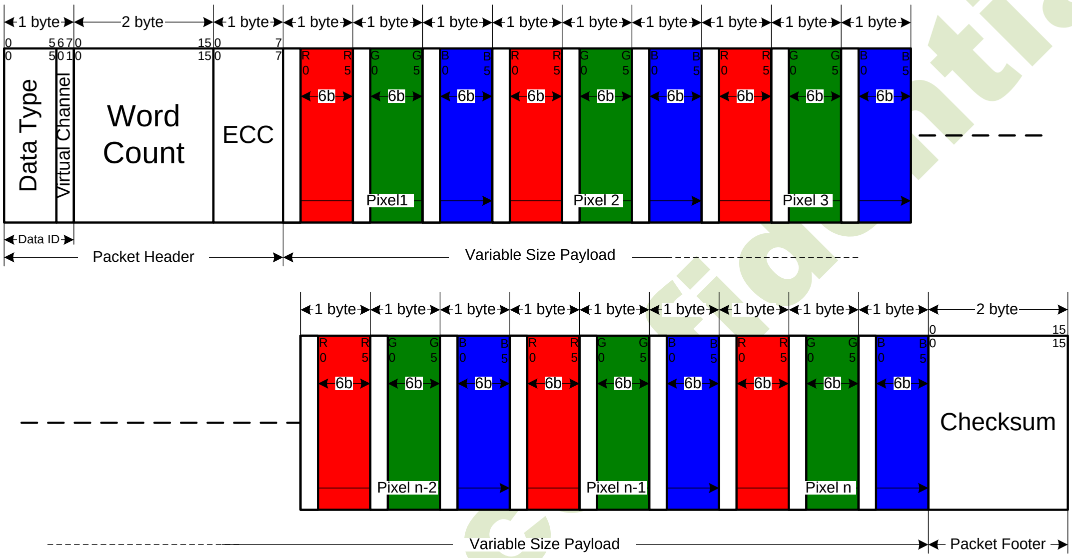


Figure. 7.13 18-bit/pixel (Loosely Packed) – RGB Color Format, Long Packet

7.1.8. Peripheral to Processor Transmission

JD9852 has bidirectional capability for returning READ data, acknowledge, or error information to the host processor. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral. Peripheral-to-processor transactions are of four basic types:

Tearing Effect (TE) is a Trigger message sent to convey display timing information to the host processor. Trigger messages are single byte packets sent by a peripheral's PHY layer in response to a signal from the DSI protocol layer.

Acknowledge is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication, i.e. either triggers or packets, is received by the peripheral with no errors.

Acknowledge and Error Report is a Short packet sent if any errors were detected in preceding transmissions from the host processor. Once reported, accumulated errors in the error register are cleared.

Response to Read Request may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

7.1.8.1. Appropriate Responses to Commands and ACK Requests

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or error information back to the host processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

•Following a non-Read command, the peripheral shall respond with Acknowledge if no errors were detected and stored since the last peripheral to host communication, i.e. either triggers or packets.

•Following a Read request, the peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication, i.e. either triggers or packets.

•Following a Read request if only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte Acknowledge and Error Report packet in the same LP transmission. The Error Report shall have the ECC Error – Single Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

•Following a non-Read command if only a single-bit ECC error was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet. The Error Report shall have the ECC Error – Single Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

•Following a Read request, if multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data. The Error Report shall have the ECC Error – Multi-Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

•Following a non-Read command, if multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet. The Error Report shall have the ECC Error – Multi-Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

•Following any command, if SoT Error, SoT Sync Error or DSI VC ID Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response, with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication, in the two-byte error field. Only the Acknowledge and Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

•Following any command, if EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication. For a read command, only the Acknowledge and Error Report packet shall be transmitted; no read data shall be sent by the peripheral in response.

Once reported to the host processor, all errors documented in this section are cleared from the Error Register.

7.1.8.2. Peripheral-to-Processor Packet Description

Table7.2 presents the complete set of peripheral-to-processor Data Types.

Data Type (Hex)	Data Type (Binary)	Description	Packet Size
0x02	00 0010	Acknowledge and Error Report	Short
0x08	00 1000	End of Transmission packet	Short
0x1C	01 1100	DCS Long READ Response	Long

Table 7.2 Data Types for Peripheral-sourced Packets

7.1.9. Format of Acknowledge and Error Report and Read Response Data Type

Acknowledge is sent using a Trigger message.
•Byte 0: 00100001 (shown here in first bit [left] to last bit [right] sequence)

Response to Read Request returns data requested by the preceding READ command from the processor. These may be short or Long packets. The format for short READ packet responses is:
•Byte 0: Data Identifier (Virtual Channel ID + Data Type)
•Bytes 1, 2: READ data, may be one or two bytes. For single byte parameters, the parameter shall be returned in Byte 1 and Byte 2 shall be set to 0x00.
•ECC byte covering the header

Acknowledge and Error Report confirms that the preceding command or data sent from the host processor to a peripheral was received, and indicates what types of error were detected on the transmission and any preceding transmissions. Note that if errors accumulate from multiple preceding transmissions, it may be difficult or impossible to identify which transmission contained the error. This message is a Short packet of four bytes, taking the form:
•Byte 0: Data Identifier (Virtual Channel ID + Acknowledge Data Type)
•Byte 1: Error Report bits 0-7
•Byte 2: Error Report bits 8-15
•ECC byte covering the header

An error report is a Short packet comprised of two bytes following the DI byte, with an ECC byte following the Error Report bytes. By convention, detection and reporting of each error type is signified by setting the corresponding bit to “1”. Table 7.3 shows the bit assignment for all error reporting.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	False Control Error
7	Contention Detected
8	ECC Error, Single-bit (detected and corrected)
9	ECC Error, Multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

Table 7.3 Error Report Bit Definitions

The first eight bits, bit 0 through bit 7, are related to the physical layer errors. Bits 8 and 9 are related to single-bit and multi-bit ECC errors. The remaining bits indicate DSI protocol-specific errors.

7.1.10. Video Mode Interface Timing

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

7.1.10.1. Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:
•**Non-Burst Mode with Sync Pulses –** enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
•**Non-Burst Mode with Sync Events –** similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
•**Burst mode –** RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral.

To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. The host processor should return to LP state once per scanline during the horizontal blanking time.

During the BLLP the DSI Link may do any of the following:
•Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX
•Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode
•Transmit one or more non-video packets from the host processor to the peripheral using HS Mode
•If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode
•Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VSS; all other lines shall start with VSE or HSS. Note that the position of synchronization packets, such as VSS and HSS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet.

Transmission packet components used in the figures in this section are defined in Figure 7.14 unless otherwise specified.

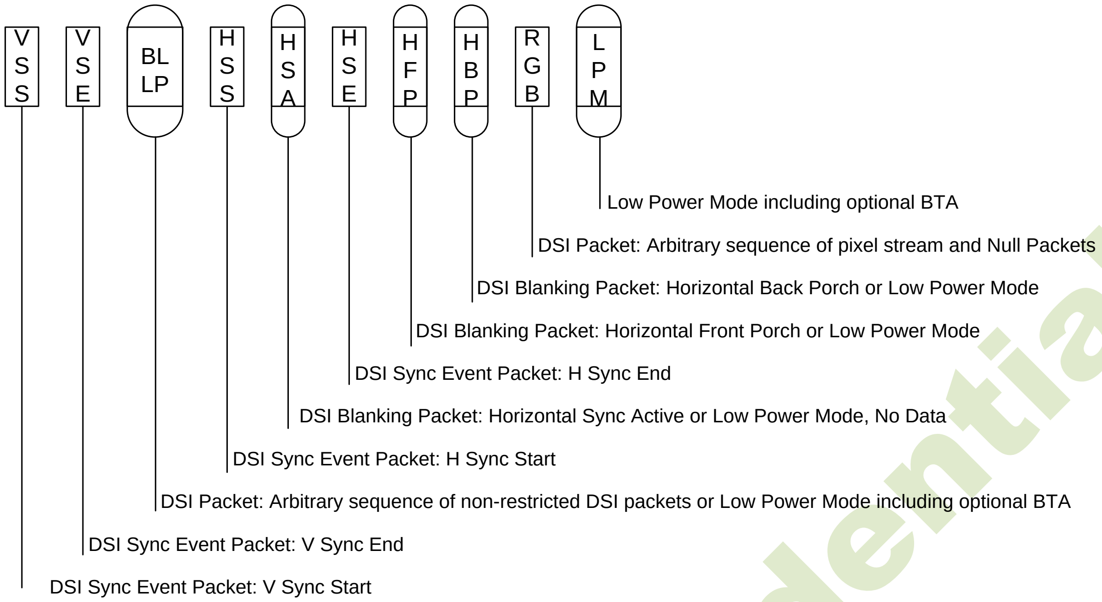


Figure. 7.14 Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

7.1.10.2. Non-Burst sync pulse mode

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure 7.15.

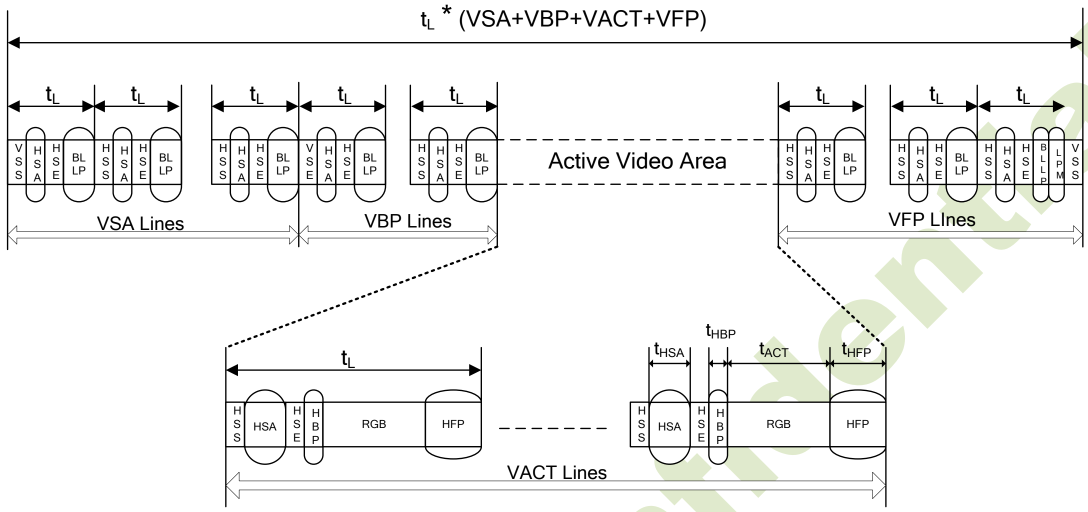


Figure. 7.15 Video Mode Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power. During HSA, HBP and HFP periods, the bus should stay in the LP-11 state.

7.1.10.3. Non-Burst sync event mode

This mode is a simplification of the "Non-Burst Mode with Sync Pulses" format. Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. An example of this mode is shown in Figure 7.16.

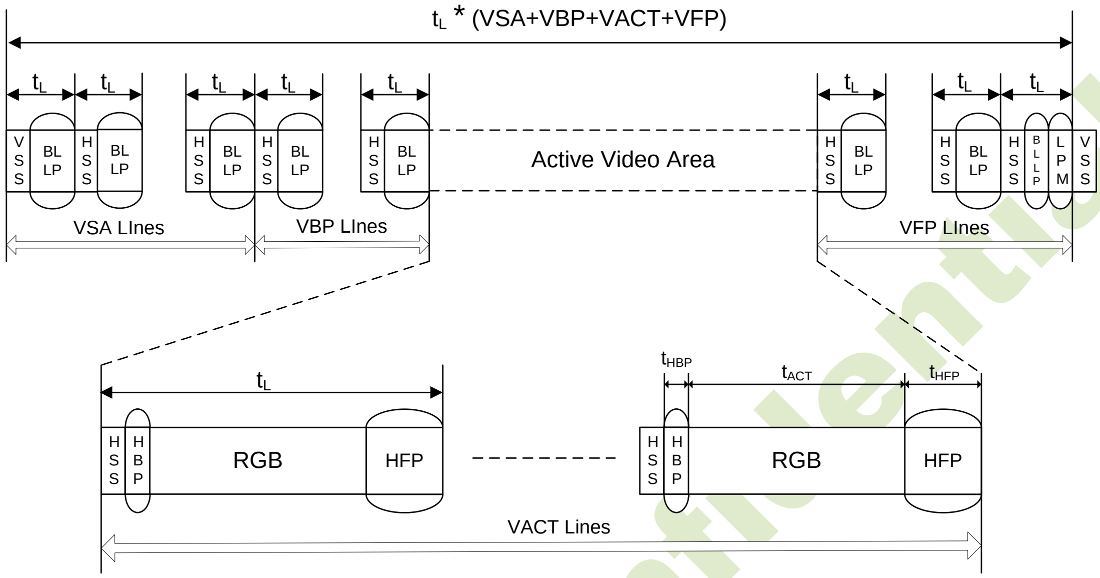


Figure. 7.16 Video Mode Timing: Non-burst Transmission with Sync Events

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

7.1.10.4. Burst mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction.

Following HS pixel data transmission, the bus may stay in HS Mode for sending blanking packets or go to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure 7.17.

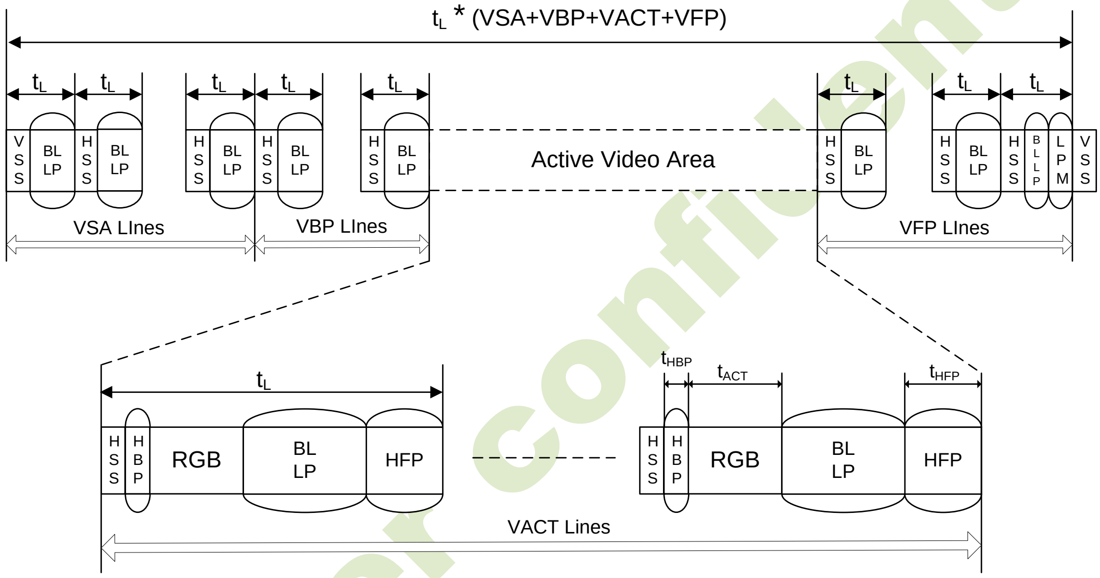


Figure. 7.17 Video Mode Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

7.1.11. Error-Correcting Code and Checksum

7.1.11.1. Burst mode

MIPI DSI uses Hamming Code Theory as ECC generate rule. The parity of each bits in ECC are showed as below.

P7=0
P6=0
P5=D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
P4=D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
P3=D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
P2=D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
P1=D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
P0=D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

ECC is generated from the twenty-four bits with in the Packet Header as illustrated in Figure 7.18, which also serves as an ECC calculation example.

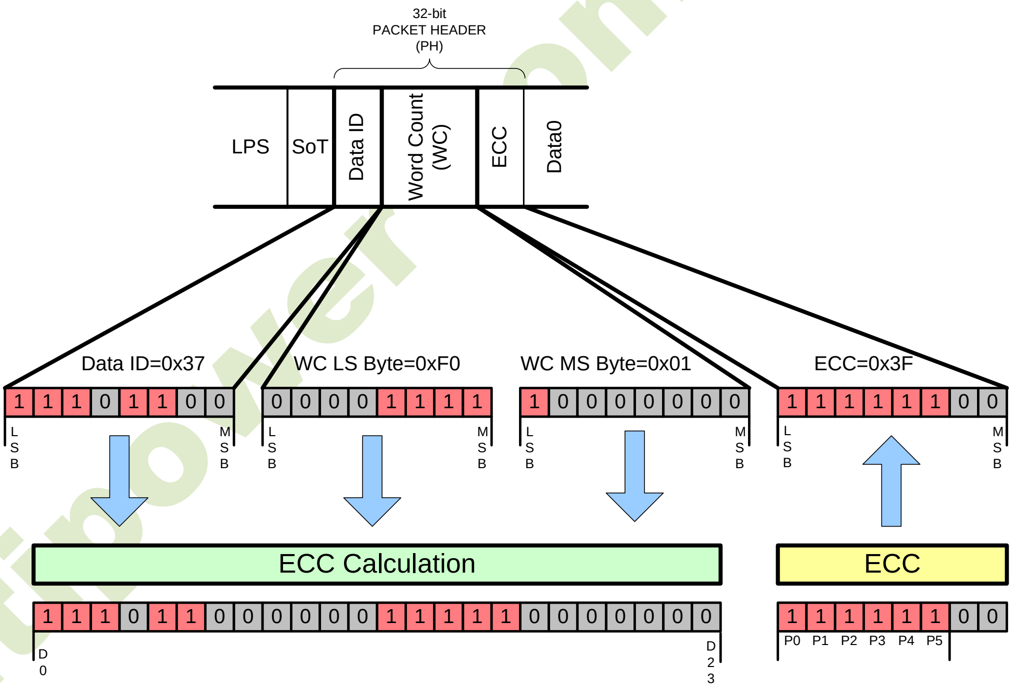


Figure. 7.18 24-bit ECC generation Example

7.1.11.2. Checksum Generation for Long Packet Payloads

To detect errors in transmission of Long packets, a checksum is calculated over the payload portion of the data packet. Note that, for the special case of a zero- length payload, the 2-byte checksum is set to 0xFFFF. The checksum shall be realized as a 16-bit CRC with a generator polynomial of x^16+x^12+x^5+x^0

The transmission of the checksum is illustrated in Figure 7.19. The LS byte is sent first, followed by the MS byte. Note that within the byte, the LS bit is sent first.

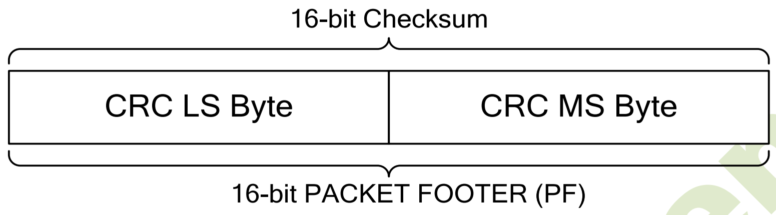


Figure. 7.19 Checksum Transmission

The CRC implementation is presented in Figure 7.20. The CRC shift register shall be initialized to 0xFFFF before packet data enters. Packet data not including the Packet Header then enters as a bitwise data stream from the left, LS bit first. Each bit is fed through the CRC shift register before it is passed to the output for transmission to the peripheral. After all bytes in the packet payload have passed through the CRC shift register, the shift register contains the checksum. C15 contains the checksum's MSB and C0 the LSB of the 16-bit checksum. The checksum is then appended to the data stream and sent to the receiver. The receiver uses its own generated CRC to verify that no errors have occurred in transmission.

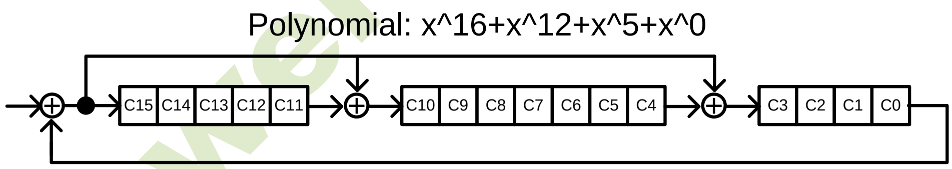


Figure. 7.20 16-bit CRC Generation Using a Shift Register

7.1.12. DPHY

7.1.12.1. Lane Module

A PHY configuration contains a Clock Lane Module and one or more Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Each Lane Module consists of one or more differential High-Speed functions utilizing both interconnect wires simultaneously, one or more single-ended Low-Power functions operating on each of the interconnect wires individually, and control & interface logic. For proper operation, the set of functions in the Lane Modules on both sides of the Lane Interconnect has to be matched.

7.1.12.2. Lane Module Type of Clock Lane and Data0

The required functions in a Lane Module depend on the Lane type and which side (master or slave) of the Lane Interconnect the Lane Module is located. There are three main Lane types: Clock Lane, Unidirectional Data Lane and Bi-directional Data Lane. Several PHY configurations can be constructed with these Lane types. In JD9852 Below show the lane module architecture of each lane.

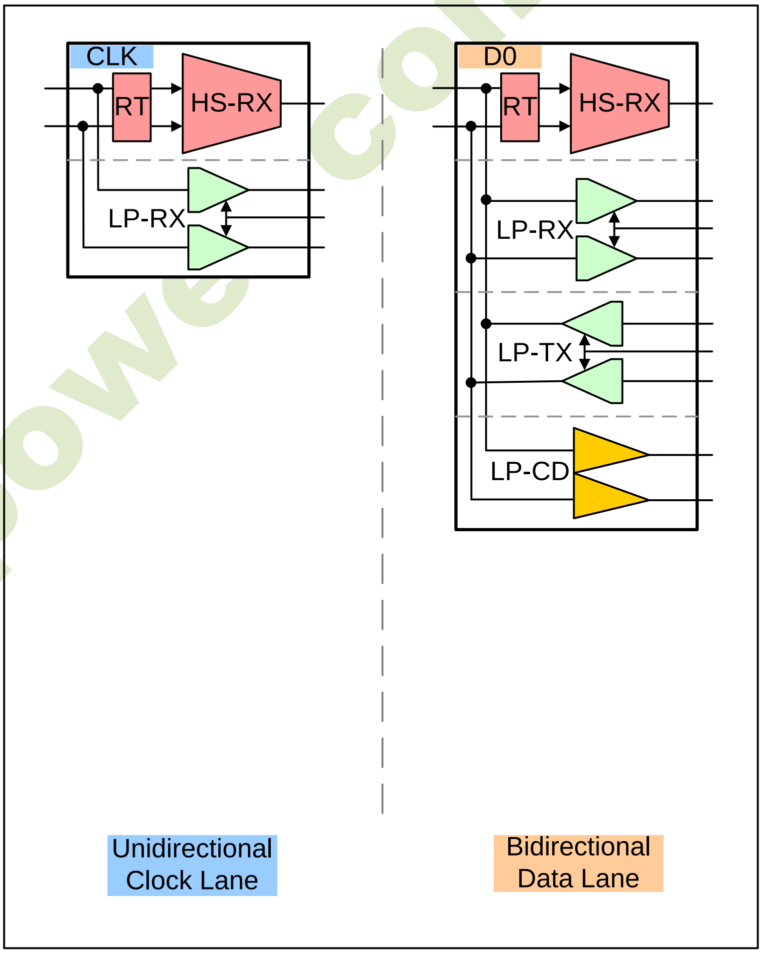


Figure. 7.21 Lane Module Type

7.1.12.3. Master and Slave

Each Link has a Master and a Slave side. The Master provides the High-Speed DDR Clock signal to the Clock Lane and is the main data source. The Slave receives the clock signal at the Clock Lane and is the main data sink. The main direction of data communication, from source to sink, is denoted as the Forward direction. Data communication in the opposite direction is called Reverse transmission. Only bi-directional Data Lanes can transmit in the Reverse direction. In all cases, the Clock Lane remains in the Forward direction, but bi-directional Data Lane(s) can be turned around, sourcing data from the Slave side.

JD9852 serves as Slave side.

7.1.12.4. Lane States and Line Levels

Transmitter functions determine the Lane state by driving certain Line levels. During normal operation either a HS-TX or a LP-TX is driving a Lane. A HS-TX always drives the Lane differentially. The two LP-TX's drive the two Lines of a Lane independently and single-ended. This results in two possible High- Speed Lane states and four possible Low-Power Lane states. The High-Speed Lane states are Differential- 0 and Differential-1. The interpretation of Low-Power Lane states depends on the mode of operation. The LP-Receivers shall always interpret both High-Speed differential states as LP-00.

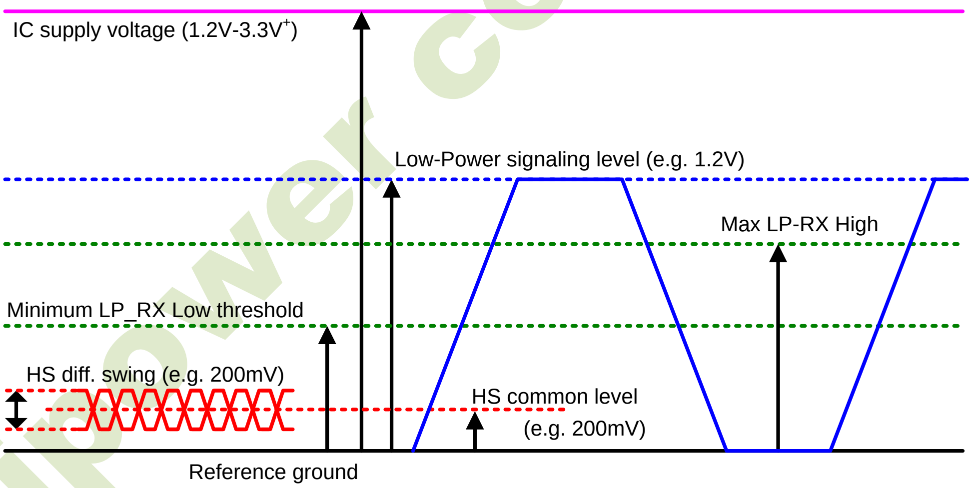


Figure. 7.22 Line Levels

The Stop state has a very exclusive and central function. If the Line levels show a Stop state for the minimum required time, the PHY state machine shall return to the Stop state regardless of the previous state. This can be in RX or TX mode depending on the most recent operating direction. Table 7.7 lists all the states that can appear on a Lane during normal operation. All LP state periods shall be at least TLPX in duration. State transitions shall be smooth and exclude glitch effects. A clock signal can be reconstructed by exclusive-ORing the Dp and Dn Lines. Ideally, the reconstructed clock has a duration of at least 2*TLPX, but may have a duty cycle other than 50% due to signal slope and trip levels effects.

Start Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

Table 7.4 Lane State Descriptions

7.1.12.5. Bi-directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. Notice that Master and Slave side shall not be changed by Turnaround.

Figure 7.23 shows the Turnaround procedure graphically.

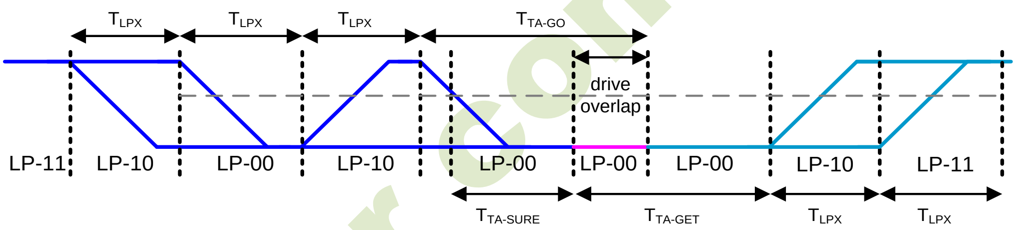


Figure. 7.23 Turnaround Procedure

7.1.12.6. Escape Mode

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. A Data Lane shall enter Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape mode in Space state (LP-00). If an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

For Data Lanes, once Escape mode is entered, the transmitter shall send an 8-bit entry command, by Spaced-One-Hot coding, to indicate the requested action. Table 7.8 lists all supported Escape mode commands and actions.

Spaced-One-Hot coding means that each Mark state is interleaved with a Space state. Each symbol consists therefore of two parts: a One-Hot phase (Mark-0 or Mark-1) and a Space phase. The TX shall send Mark-0 followed by a Space to transmit a 'zero-bit' and it shall send a Mark-1 followed by a Space to transmit a 'one-bit'. A Mark that is not followed by a Space does not represent a bit. The last phase before exiting Escape mode with a Stop state shall be a Mark-1 state that is not part of the communicated bits, as it is not followed by a Space state.

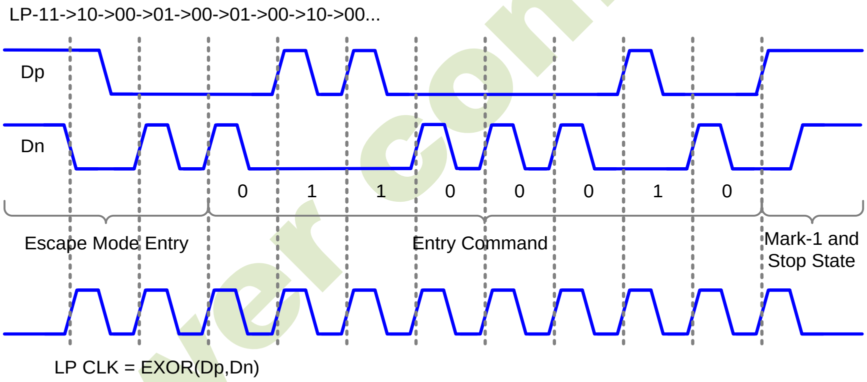


Figure. 7.24 Trigger-Reset Command in Escape Mode

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low power State	mode	00011110
Reset-Trigger	Trigger	01100010
TE-Trigger	Trigger	01011101
Acknowledge	Trigger	00100001

Table 7.5 Escape Entry Codes

7.1.12.7. Remote Trigger

Trigger signaling is the mechanism to send a flag to the protocol at the receiving side, on request of the protocol on the transmitting side. This can be either in the Forward or Reverse direction depending on the direction of operation and available Escape mode functionality. Trigger signaling requires Escape mode capability and at least one matching Trigger Escape Entry Command on both sides of the interface. Any bit received after a Trigger Command but before the Lines go to Stop state shall be ignored. Therefore, dummy bytes can be concatenated in order to provide Clock information to the receive side.

7.1.12.8. Remote Trigger

If the Escape mode Entry procedure is followed-up by the Entry Command for Low-Power Data Transmission (LPDT), Data can be communicated by the protocol at low speed, while the Lane remains in Low-Power mode. Data shall be encoded on the lines with the same Spaced-One-Hot code as used for the Entry Commands. The data is self-clocked by the applied bit encoding and does not rely on the Clock Lane. The Lane can pause while using LPDT by maintaining a Space state on the Lines. A Stop state on the Lines stops LPDT, exits Escape mode, and switches the Lane to Control mode. The last phase before Stop state shall be a Mark-1 state, which does not represent a data-bit. At the end of LPDT the Lane shall return to the Stop state.

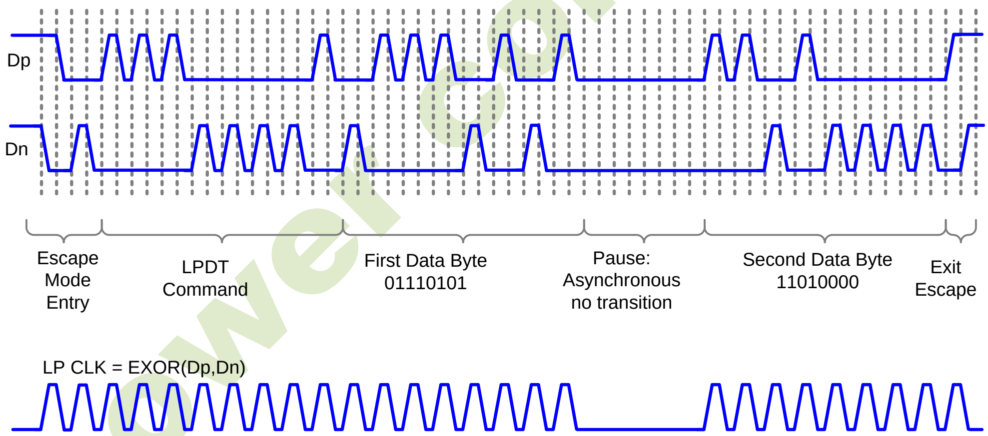


Figure. 7.25 Two Data Byte Low-Power Data Transmission Example

7.1.12.9. Ultra-Low Power State(ULPS)

If the Ultra-Low Power State Entry Command is sent after an Escape mode Entry command, the Lane shall enter the Ultra-Low Power State (ULPS). This command shall be flagged to the receive side Protocol. During this state, the Lines are in the Space state (LP-00). Ultra-Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state.

7.1.12.10. TE Trigger

A Command Mode display module has its own timing controller and local frame buffer for display refresh. In some cases the host processor needs to be notified of timing events on the display module, e.g. the start of vertical blanking or similar timing information. In a traditional parallel-bus interface like DBI-2, a dedicated signal wire labeled TE (Tearing Effect) is provided to convey such timing information to the host processor. In a DSI system, the same information, with reasonably low latency, shall be transmitted from the display module to the host processor when requested, using the bidirectional Data Lane.

For polling to the display module, the host processor shall detect the current scan line information with a DCS command such as get_scan_line to avoid Tearing Effects. For TE-reporting from the display module, the TE-reporting function is enabled and disabled by three DCS commands to the display module’s controller: set_tear_on, set_tear_scanline, and set_tear_off.

set_tear_on and set_tear_scanline are sent to the display module as DSI Data Type 0x15 (DCS Short Write, one parameter) and DSI Data Type 0x39 (DCS Long Write/write_LUT), respectively. The host processor ends the transmission with Bus Turn-Around asserted, giving bus possession to the display module. Since the display module’s DSI Protocol layer does not interpret DCS commands, but only passes them through to the display controller, it responds with a normal Acknowledge and returns bus possession to the host processor. In this state, the display module cannot report TE events to the host processor since it does not have bus possession.

To enable TE-reporting, the host processor shall give bus possession to the display module without an accompanying DSI command transmission after TE reporting has been enabled. This is accomplished by the host processor’s protocol logic asserting (internal) Bus Turn-Around signal to its D-PHY functional block. The PHY layer will then initiate a Bus Turn-Around sequence in LP mode, which gives bus possession to the display module.

Since the timing of a TE event is, by definition, unknown to the host processor, the host processor shall give bus possession to the display module and then wait for up to one video frame period for the TE response. During this time, the host processor cannot send new commands, or requests to the display module, because it does not have bus possession.

When the TE event takes place the display module shall send TE event information in LP mode using a specified trigger message available with D-PHY protocol via the following sequence:
•The display module shall send the LP Escape Mode sequence
•The display module shall then send the trigger message byte 01011101 (shown here in first bit to last bit sequence)
•The display module shall then return bus possession to the host processor
This Trigger Message is reserved by DSI for TE signaling only and shall not be used for any other purpose in a DSI-compliant interface.

7.1.13. High Speed Transmission

7.1.13.1. Burst Payload Data

The payload data of a burst shall always represent an integer number of payload data bytes with a minimum length of one byte. Note that for short bursts the Start and End overhead consumes much more time than the actual transfer of the payload data. There is no maximum number of bytes implied by the PHY. However, in the PHY there is no autonomous way of error recovery during a HS data burst and the practical BER will not be zero. Therefore, it is important to consider for every individual protocol what the best choice is for maximum burst length.

7.1.13.2. Burst Payload Data

After a Transmit request, a Data Lane leaves the Stop state and prepares for High-Speed mode by means of a Start-of-Transmission (SoT) procedure. Table 7.6 describes the sequence of events on TX and RX side.

TX Side	RX Side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Rqst state (LP-01) for time T_{LPX}	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time $T_{HS\text{-}PREPARE}$	Observes transition from LP-01 to LP-00 on the Lines, enables Line Termination after time $T_{D\text{-}TERM\text{-}EN}$
Enables High-Speed driver and disables Low-Powerdrivers simultaneously.	
Drives HS-0 for a time $T_{HS\text{-}ZERO}$	Enables HS-RX and waits for timer $T_{HS\text{-}SETTLE}$ to expire in order to neglect transition effects
	Starts looking for Leader-Sequence
Inserts the HS Sync-Sequence '00011101' beginning on a rising Clock edge	
	Synchronizes upon recognition of Leader Sequence '011101'
Continues to Transmit High-Speed payload data	
	Receives payload data

Table 7.6 Start-of-Transmission Sequence

7.1.13.3. End-of-Transmission

At the end of a Data Burst, a Data Lane leaves High-Speed Transmission mode and enters the Stop state by means of an End-of-Transmission (EoT) procedure. Table 7.7 shows a possible sequence of events during the EoT procedure. Note, EoT processing may be handled by the protocol or by the D-PHY

TX Side	RX Side
Completes Transmission of payload data	Receives payload data
Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS\text{-}TRAIL}$	
Disables the HS-TX, enables the LP-TX, and drives Stop state (LP-11) for a time $T_{HS\text{-}EXIT}$	Detects the Lines leaving LP-00 state and entering Stop state (LP-11) and disables Termination
	Neglect bits of last period $T_{HS\text{-}SKIP}$ to hide transition effects
	Detect last transition in valid Data, determine last valid Data byte and skip trailer sequence

Table 7.7 End-of-Transmission Sequence

7.1.13.4. High Speed Data Transmission

Figure 7.26 shows the sequence of events during the transmission of a Data Burst. Transmission can be started and ended independently for any Lane by the protocol. However, for most applications the Lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per Lane.

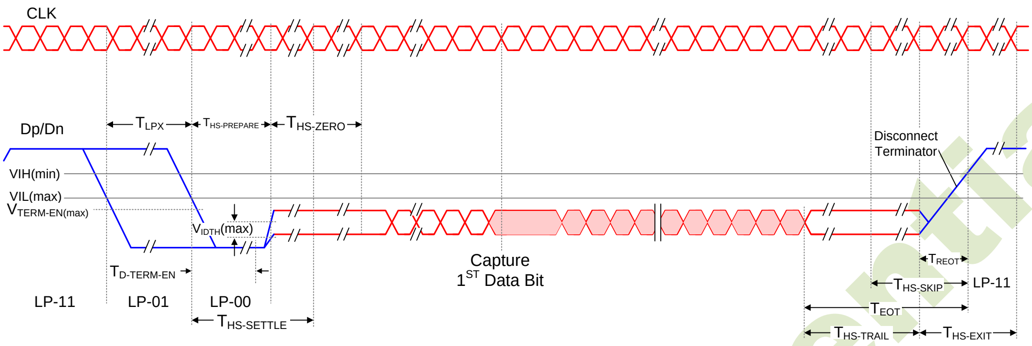


Figure. 7.26 High-Speed Data Transmission in Bursts

7.1.13.5. High Speed Clock Transmission

In High-Speed mode the Clock Lane provides a low-swing, differential DDR (half-rate) clock signal from Master to Slave for High-Speed Data Transmission. The Clock signal shall have quadrature-phase with respect to a toggling bit sequence on a Data Lane in the Forward direction and a rising edge in the center of the first transmitted bit of a burst. The detail Clock Start and Stop procedures are shown in Figure 7.27.

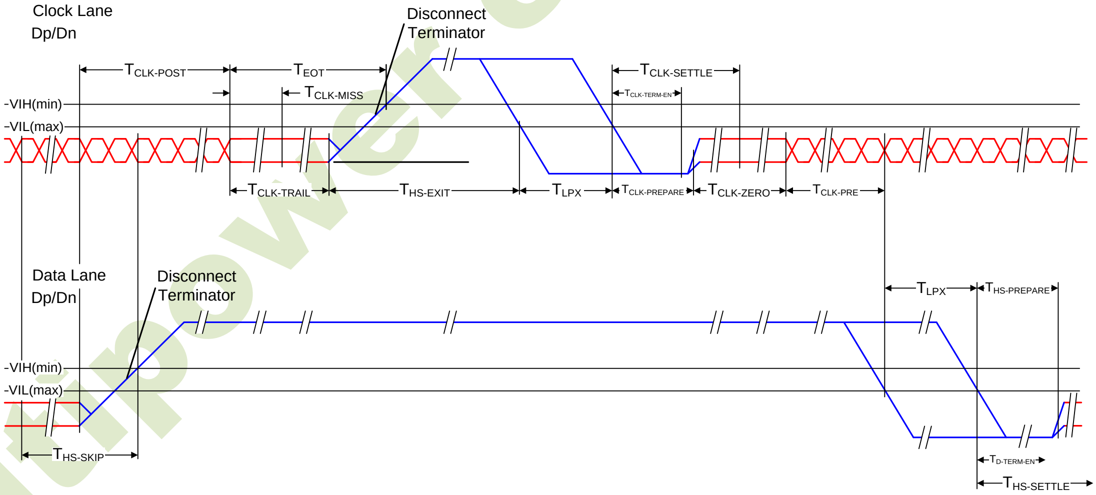


Figure. 7.27 Switching the Clock Lane between Transmission and Low-Power Mode

7.1.14. System Power state

Each Lane within a PHY configuration, that is powered and enabled, has potentially three different power consumption levels: High-Speed Transmission mode, Low-Power mode and Ultra-Low Power State.

7.1.14.1. Initialization

After power-up, the Slave side PHY shall be initialized when the Master PHY drives a Stop State (LP-11) for a period longer then TINIT. The first Stop state longer than the specified TINIT is called the Initialization period. The Master side shall ensure that a Stop State longer than TINIT does not occur on the Lines before the Master is initialized.

TINIT must larger than 500us.

7.1.14.2. Global Operation Flow Diagram

Figure 7.28 shows the operational flow diagram for a Data Lane Module. Within both TX and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround, and Initialization.

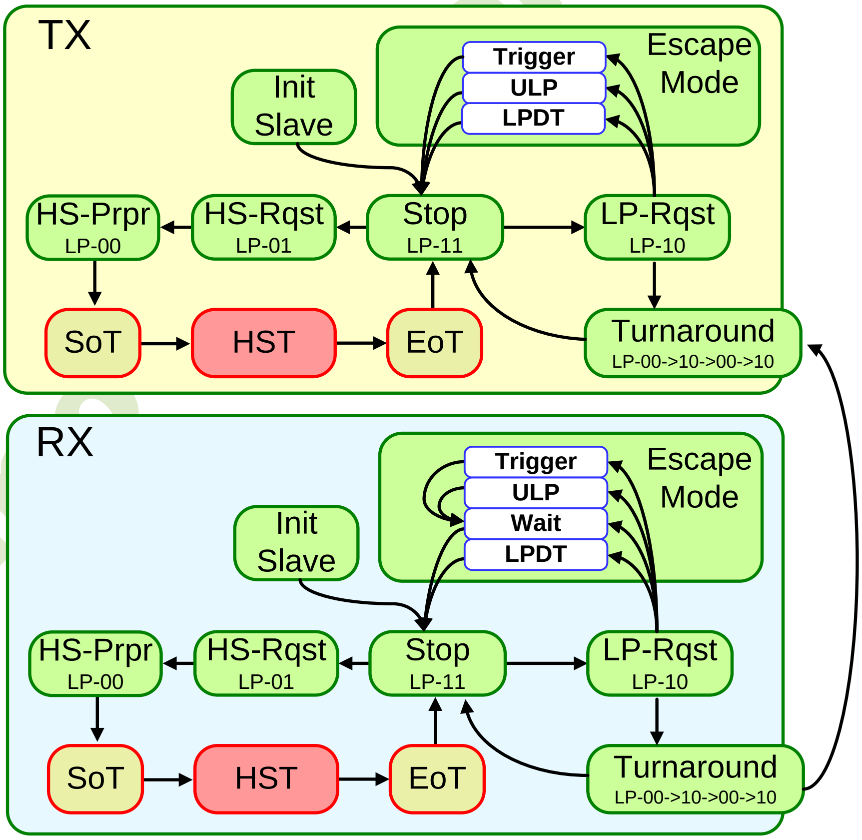


Figure. 7.28 Data Lane Module State Diagram

Figure 7.29 shows the state diagram for a Clock Lane Module. The Clock Lane Module has four major operational states: Init (of unspecified duration), Low-Power Stop state, Ultra-Low Power state, and High- Speed clock transmission.

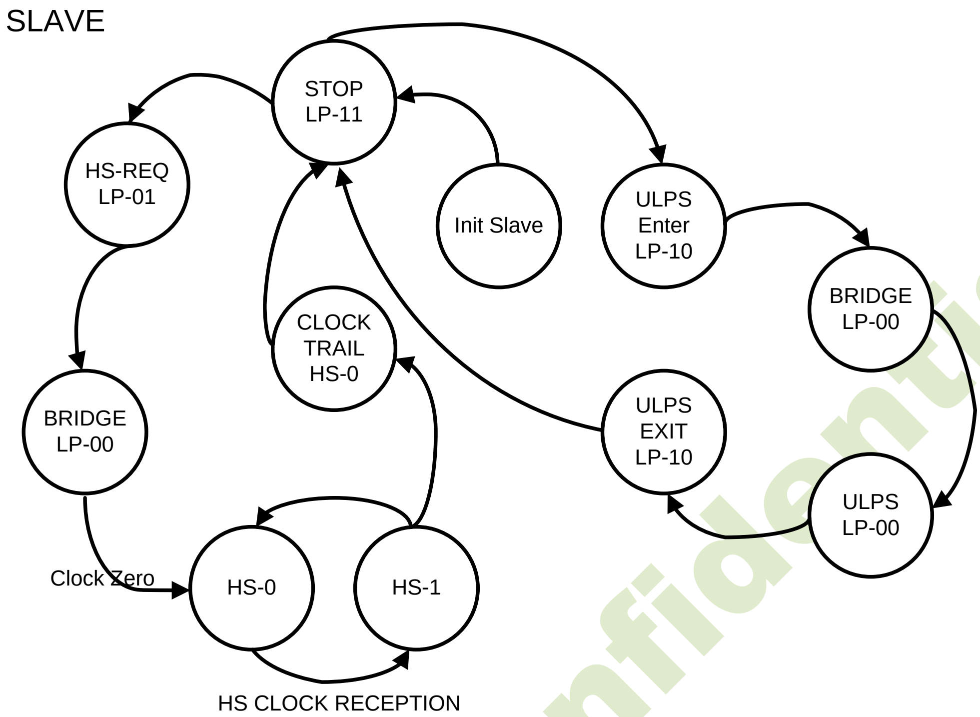


Figure. 7.29 Clock Lane Module State Diagram

7.2. MCU interfaces

JD9852 provides the 8-/9-/16-/18-bit parallel system interface for 8080-I /8080- II series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM[3:0] and the bit formal per pixel color order is selected by COLMOD(3Ah) register.

7.2.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	IM1	IM0	Interface	Data Bus Selection
0	0	0	0	8080 MCU 8-bit bus interface I	DB[7:0]
0	0	0	1	8080 MCU 16-bit bus interface I	DB[15:0]
0	0	1	0	8080 MCU 9-bit bus interface I	DB[8:0]
0	0	1	1	8080 MCU 18-bit bus interface I	DB[17:0]
0	1	0	1	3-wire 9-bit data serial interface I	SDA: in/out
				2 data lane serial interface	SDA: in/out, WRX:in
0	1	1	0	4-wire 8-bit data serial interface I	SDA: in/out
1	0	0	0	8080 MCU 16-bit bus interface II	DB[17:10], DB[8:1]
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]
1	0	1	0	8080 MCU 18-bit bus interface II	DB[17:0],
1	0	1	1	8080 MCU 9-bit bus interface II	DB[17:9]
1	1	0	1	3-wire 9-bit data serial interface II	SDA: in/ SDO: out
1	1	1	0	4-wire 8-bit data serial interface II	SDA: in/ SDO: out

7.2.2. 8080-I Series Parallel Interface

JD9852 can be accessed via 8-/9-/16-/18-bit MCU 8080-I series parallel interface. The chip select CSX (active low) is used to enable or disable JD9852 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

JD9852 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D[17:0] bits are commands.

The 8080-I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-I Interface selection is done when IM3 pin is low state (VSSC level). Interface bus width can be selected by IM [3:0] bits.

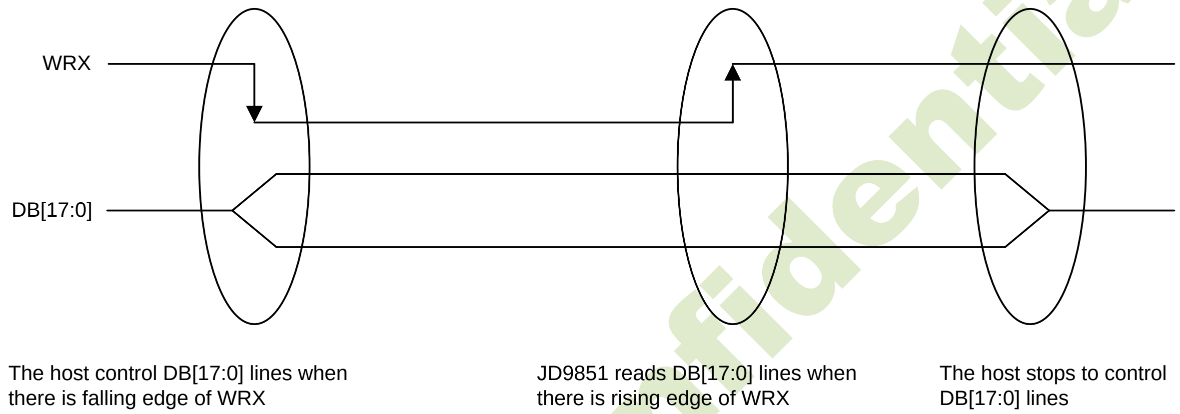
The selection of 8080-I series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	Interface	CSX	D/CX	RDX	WRX	Function
0	0	0	0	8-bit parallel	0	0	1	↑	Write 8-bit command (DB[7:0])
0	0	0	0	8-bit parallel	0	1	1	↑	Write 8-bit display data or 8-bit parameter (DB[7:0])
0	0	0	0	8-bit parallel	0	1	↑	1	Read 8-bit display data (DB[7:0])
0	0	0	0	8-bit parallel	0	1	↑	1	Read 8-bit parameter or status (DB[7:0])
0	0	0	1	16-bit parallel	0	0	1	↑	Write 8-bit command (DB[7:0])
0	0	0	1	16-bit parallel	0	1	1	↑	Write 16-bit display data or 8-bit parameter (DB[15:0])
0	0	0	1	16-bit parallel	0	1	↑	1	Read 16-bit display data (DB[15:0])
0	0	0	1	16-bit parallel	0	1	↑	1	Read 8-bit parameter or status (DB[7:0])
0	0	1	0	9-bit parallel	0	0	1	↑	Write 8-bit command (DB[7:0])
0	0	1	0	9-bit parallel	0	1	1	↑	Write 9-bit display data or 8-bit parameter (DB[8:0])
0	0	1	0	9-bit parallel	0	1	↑	1	Read 9-bit display data (DB[8:0])
0	0	1	0	9-bit parallel	0	1	↑	1	Read 8-bit parameter or status (DB[7:0])
0	0	1	1	18-bit parallel	0	0	1	↑	Write 8-bit command (DB[7:0]).
0	0	1	1	18-bit parallel	0	1	1	↑	Write 18-bit display data or 8-bit parameter (DB[17:0])
0	0	1	1	18-bit parallel	0	1	↑	1	Read 18-bit display data (DB[17:0])
0	0	1	1	18-bit parallel	0	1	↑	1	Read 8-bit parameter or status (DB[17:0])

7.2.2.1. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is GRAM data or command's parameter.

The following figure shows a write cycle for the 8080-I MCU interface.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure. 7.30 8080-Series WRX Protocol

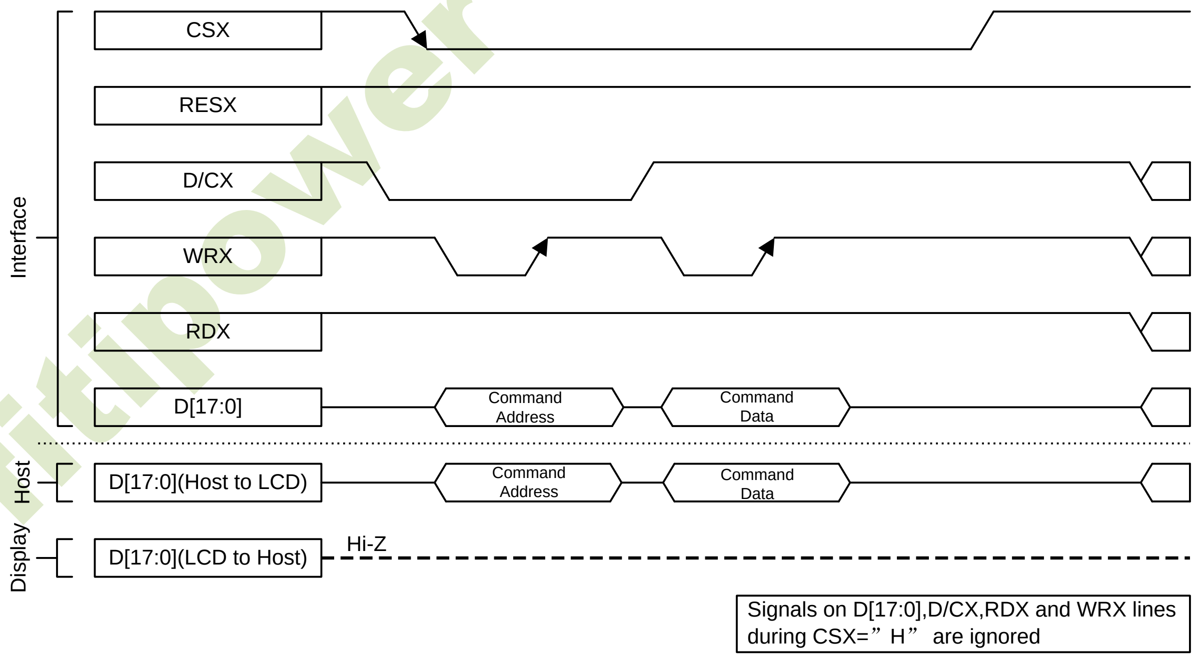
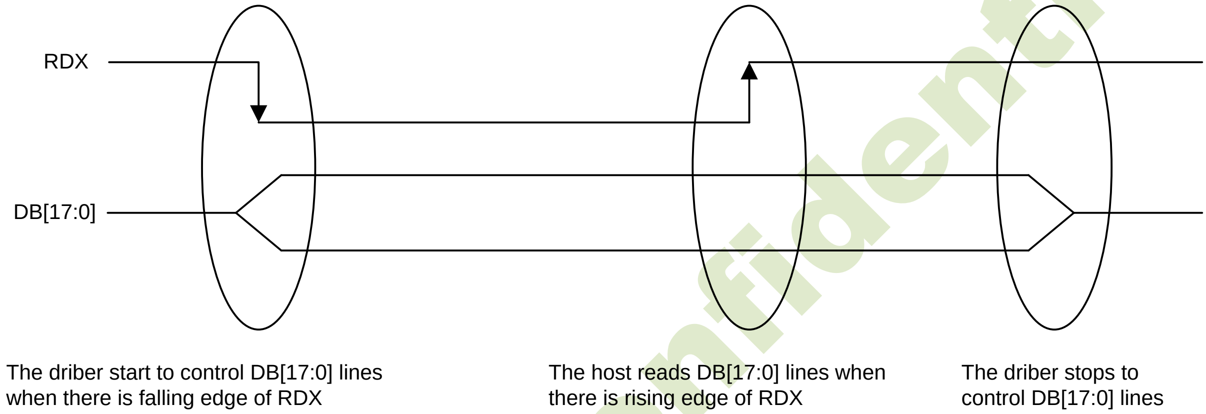


Figure. 7.31 8080-Series Parallel Bus Protocol, Write Register or Display RAM

7.2.2.2. Read Cycle Sequence

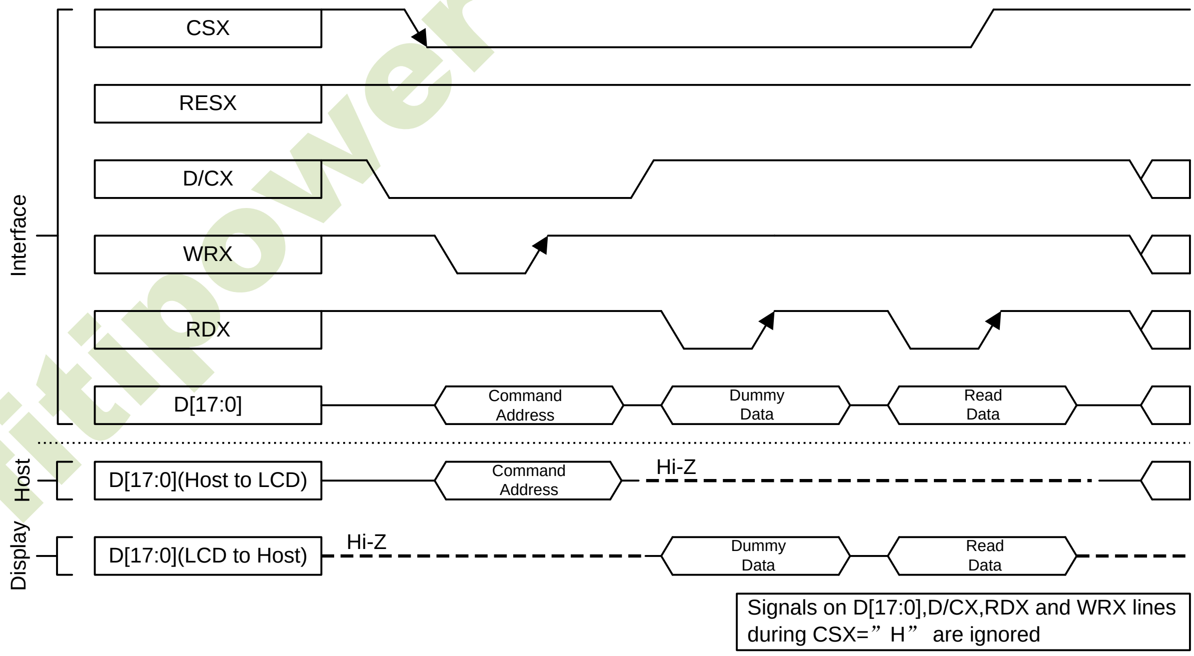
The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle, while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-I MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped)

Figure. 7.32 8080-Series RDX Protocol



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

Figure. 7.33 8080-Series Parallel Bus Protocol, Read Register or Display RAM

7.2.3. 8080-Ⅱ Series Parallel Interface

JD9852 can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅱ series parallel interface. The chip select CSX (active low) is used to enable or disable JD9852 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

JD9852 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D[17:0] bits are commands.

The 8080-II series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-II Interface selection is done when IM3 pin is high state (IOVCC level). Interface bus width can be selected by IM [3:0] bits.

The selection of 8080-II series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
1	0	0	0	16-bit parallel	0	1	↑	Write 8-bit command (DB[8:1])
					1	1	↑	Write 16-bit display data or 8-bit parameter(DB[17:10],DB[8:1])
					1	↑	1	Read 16-bit Display data (DB[17:10], DB[8:1])
					1	↑	1	Read 8-bit parameter or status (DB[8:1])
1	0	0	1	8-bit parallel	0	1	↑	Write 8-bit command (DB[17:10])
					1	1	↑	Write 8-bit display data or 8-bit parameter (DB[17:10])
					1	↑	1	Read 8-bit Display data (DB[17:10])
					1	↑	1	Read 8-bit parameter or status (DB[17:10])
1	0	1	0	18-bit parallel	0	1	↑	Write 8-bit command (DB[8:1])
					1	1	↑	Write 18-bit display data or 8-bit parameter (DB[17:0], DB[8:1])
					1	↑	1	Read 18-bit Display data (DB[17:0])
					1	↑	1	Read 8-bit parameter or status (DB[8:1])
1	0	1	1	9-bit parallel	0	1	↑	Write 8-bit command (DB[17:10])
					1	1	↑	Write 9-bit display data or 8-bit parameter (DB[17:9])
					1	↑	1	Read 9-bit Display data (DB[17:9])
					1	↑	1	Read 8-bit parameter or status (DB[17:10])

7.2.4. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MCU-Interface Mode</th><th>Read back selection</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-line serial interface</td><td rowspan="4">Via the read instruction</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-line serial interface</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-line serial interface</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-line serial interface</td></tr>
</table>

JD9852 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and JD9852. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/ Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

7.2.4.1. Pin Description

3-line serial interface I

Pin Name	Description
CSX	Chip selection signal
DCX_SCL	Clock signal
SDA	Serial input/output data

4-line serial interface I

Pin Name	Description
CSX	Chip selection signal
WRX	Data is regarded as a command when WRX is low Data is regarded as a parameter or data when WRX is high
DCX_SCL	Clock signal
SDA	Serial input/output data

3-line serial interface II

Pin Name	Description
CSX	Chip selection signal
DCX_SCL	Clock signal
SDA	Serial input data
SDO	Serial output data

4-line serial interface II

Pin Name	Description
CSX	Chip selection signal
WRX	Data is regarded as a command when WRX is low Data is regarded as a parameter or data when WRX is high
DCX_SCL	Clock signal
SDA	Serial input data
SDO	Serial output data

7.2.4.2. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to JD9852. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM(Memory write command),or command register as parameter.

Any instruction can be sent in any order to JD9852 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

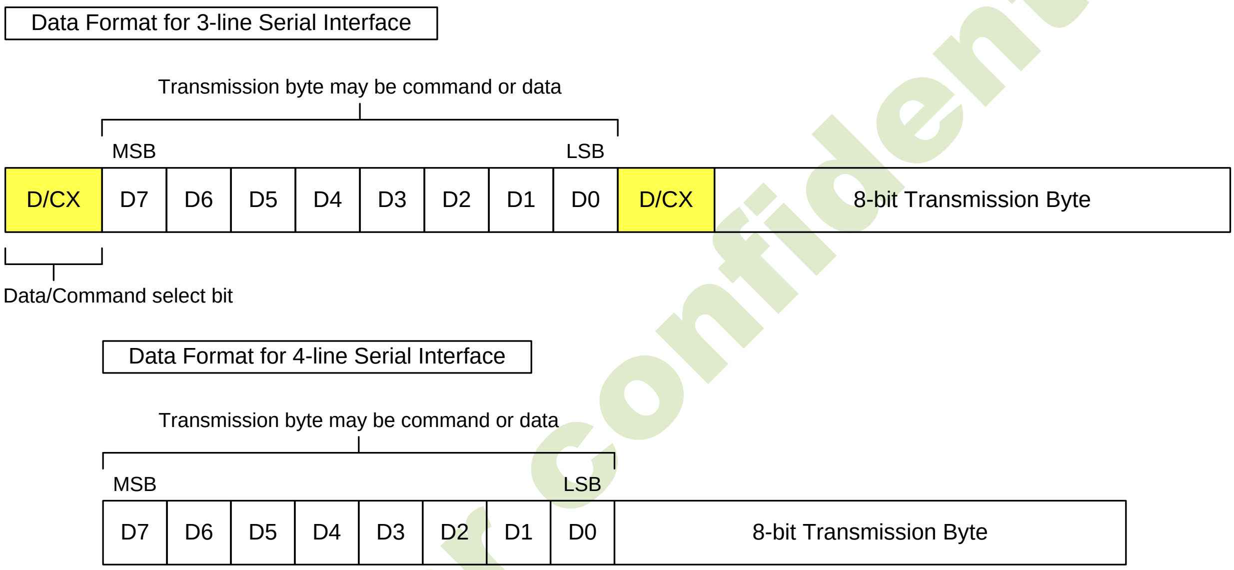


Figure. 7.34 Serial interface data stream format

Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by JD9852 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

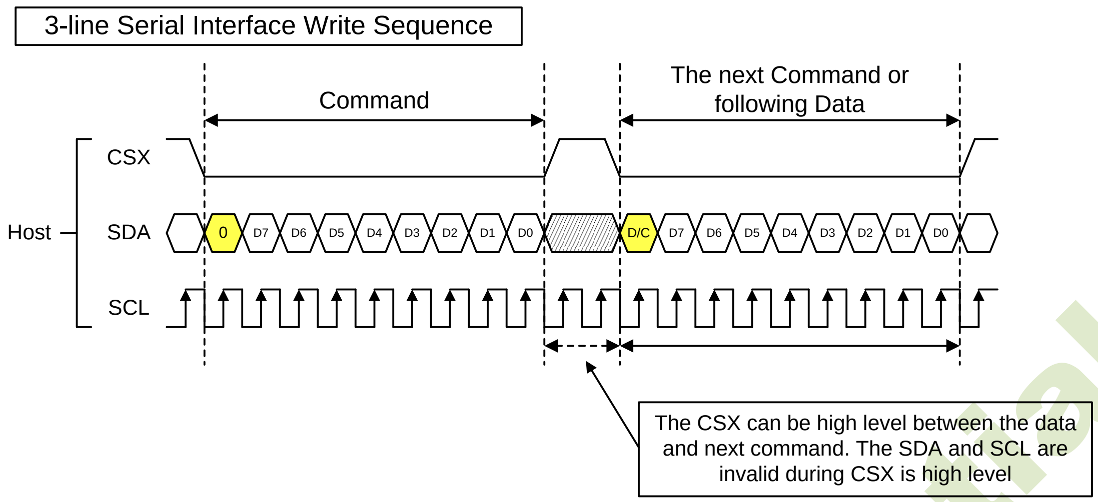


Figure. 7.35 3-line serial interface write protocol

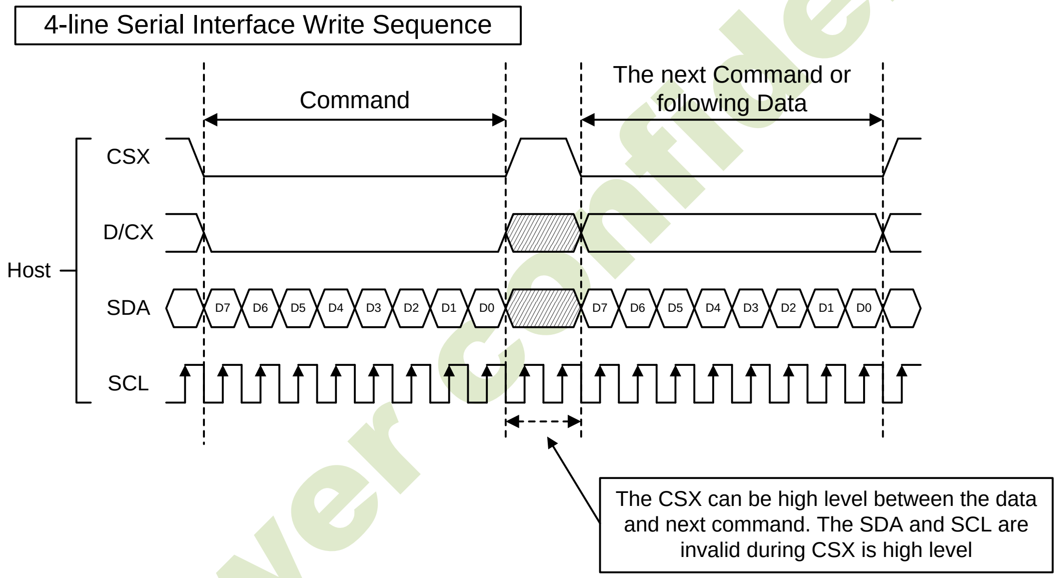


Figure. 7.36 4-line serial interface write protocol

7.2.4.3. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter from JD9852. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. JD9852 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

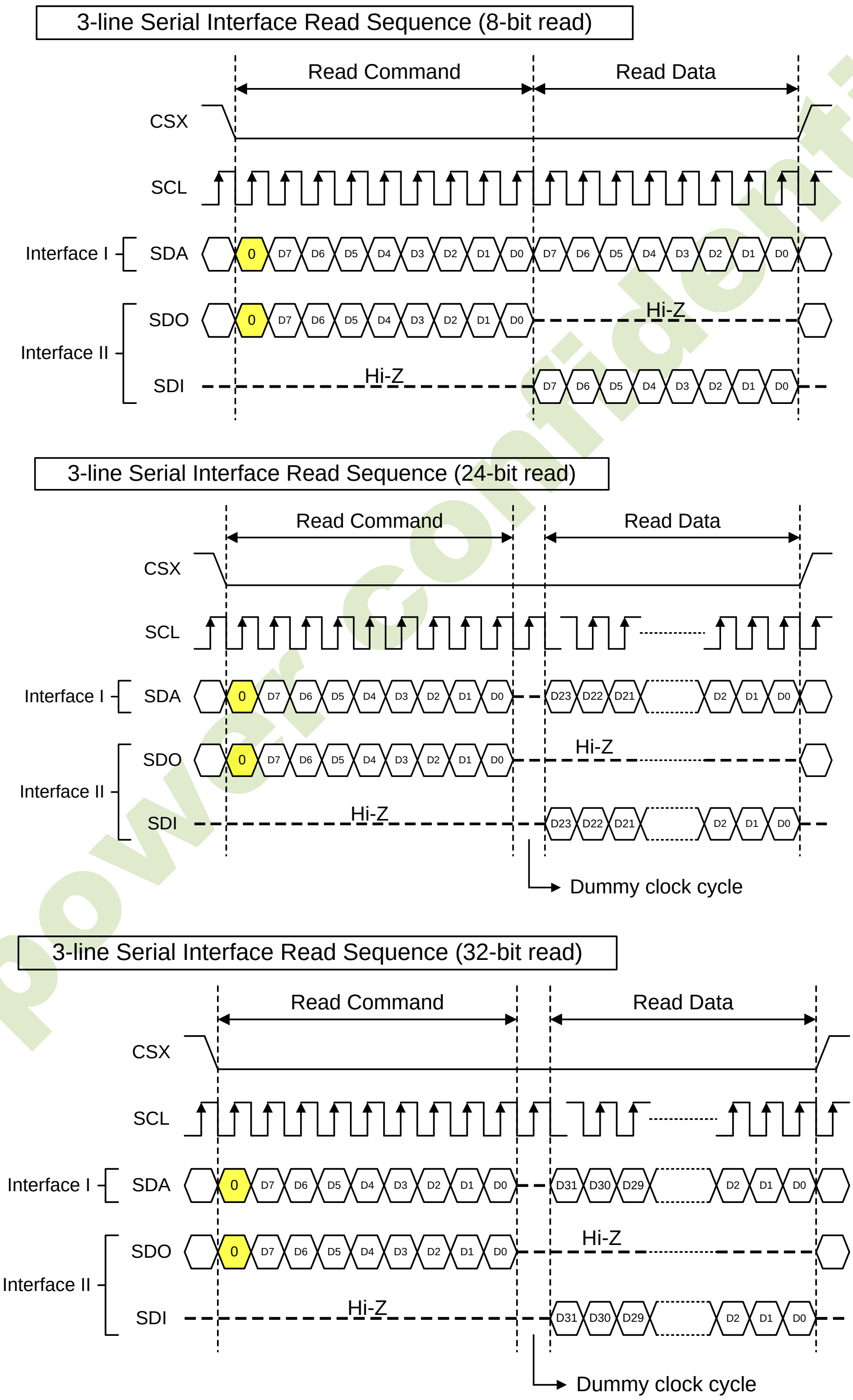
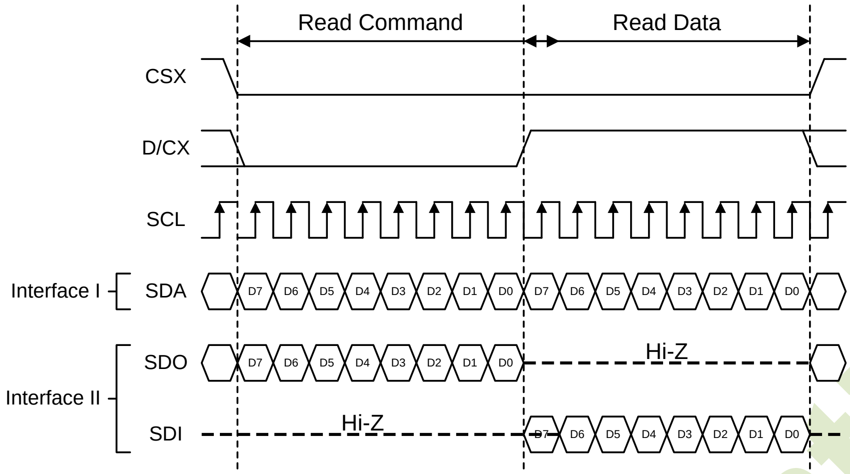
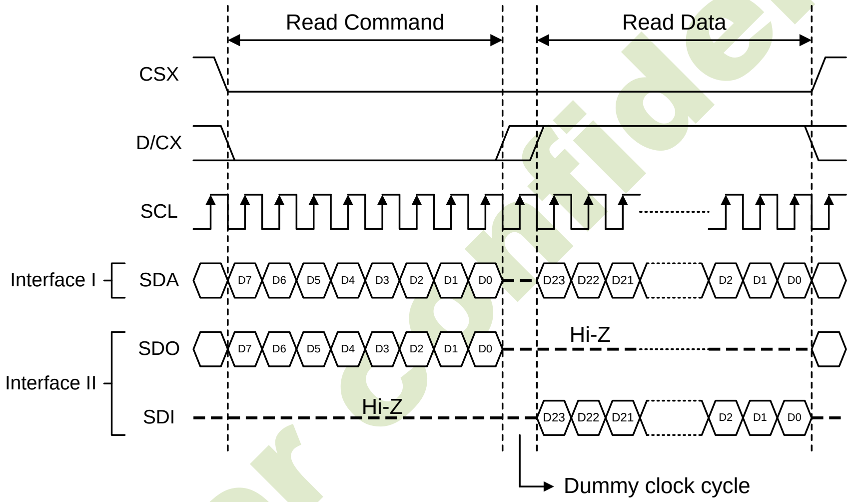


Figure. 7.37 3-line serial interface read protocol

4-line Serial Interface Read Sequence (8-bit read)



4-line Serial Interface Read Sequence (24-bit read)



4-line Serial Interface Read Sequence (32-bit read)

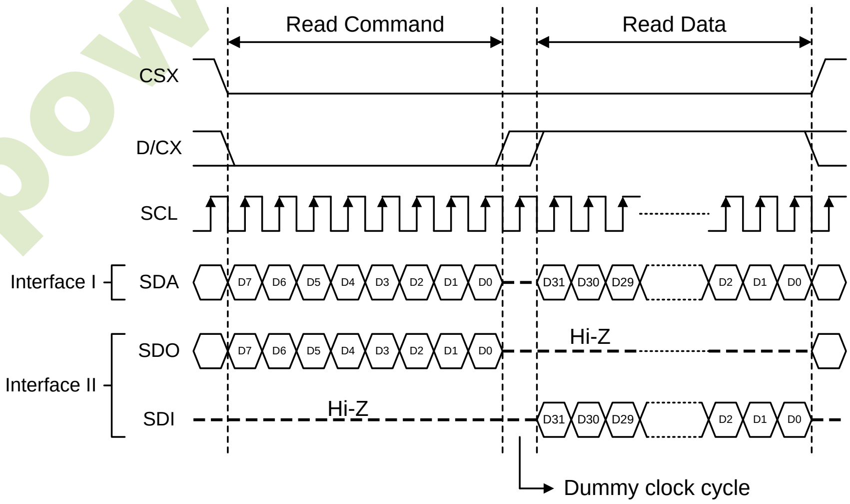


Figure. 7.38 4-line serial interface read protocol

7.2.5. 2 Data Lane Interface

IM3	IM2	IM1	IM0	MCU-Interface Mode	Read back selection
0	1	0	1	2 data lane serial interface	Via the read instruction (8-bit, 24-bit and 32-bitread)

7.2.5.1. Write Cycle Sequence

The command write protocol of 2-wire data lane serial interface is the same with the 3-line serial interface, so users can ignore the input data of WRX.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

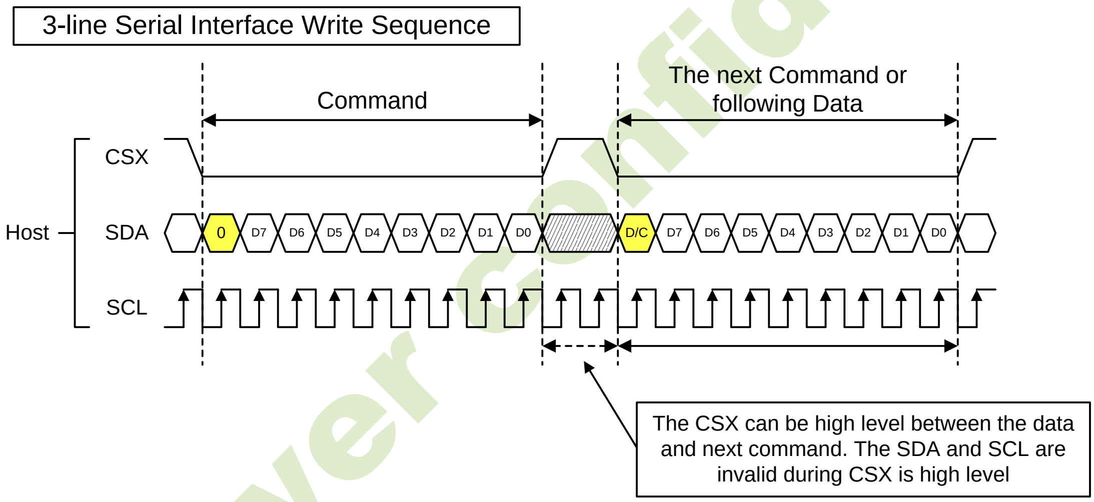


Figure. 7.39 3-line serial interface write protocol

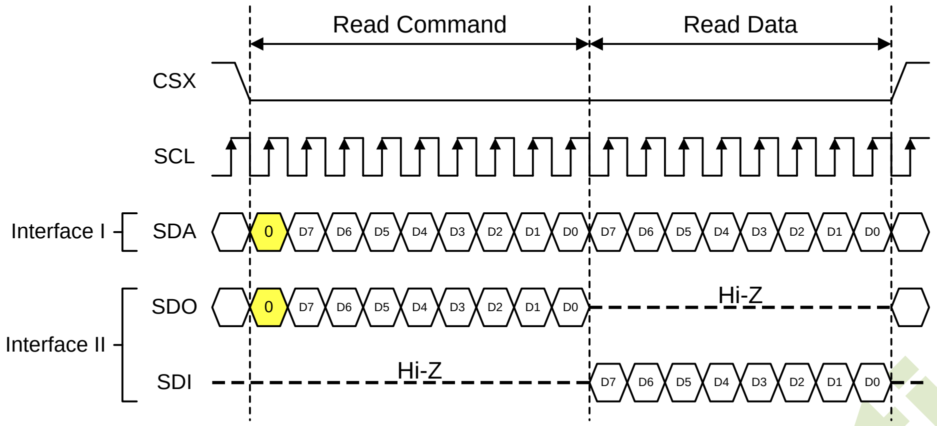
7.2.5.2. Read Cycle Sequence

The read mode of 2-wire data lane serial interface is the same with the 3-line serial interface and WRX pin can be ignored.

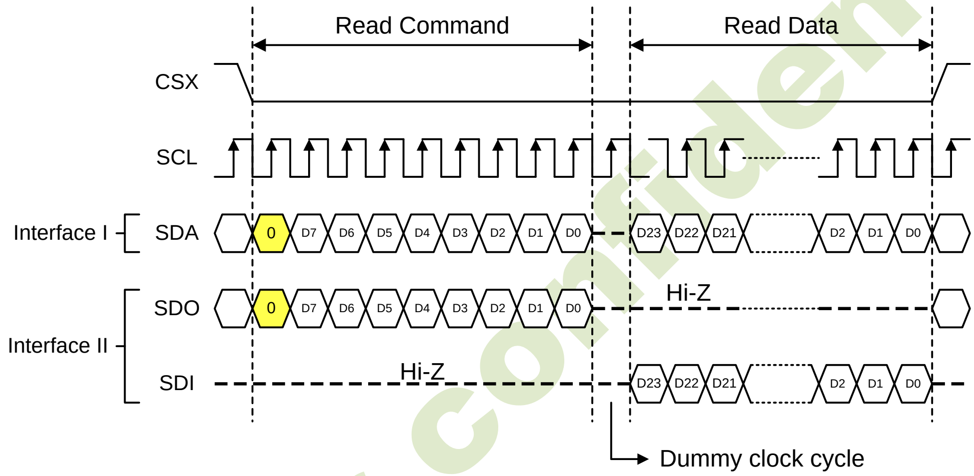
To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

3-line Serial Interface Read Sequence (8-bit read)



3-line Serial Interface Read Sequence (24-bit read)



3-line Serial Interface Read Sequence (32-bit read)

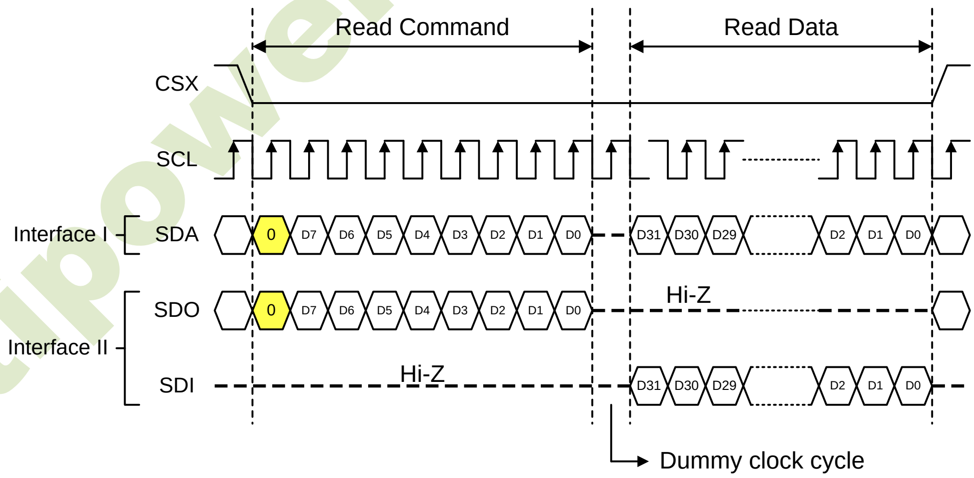
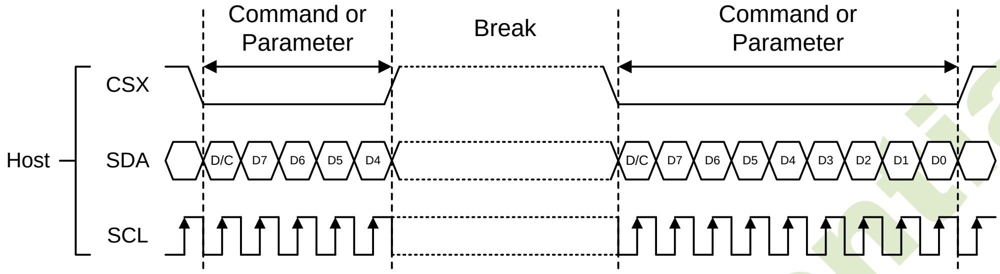


Figure. 7.40 3-line serial interface read protocol

7.2.6.Data Transfer Break and Recovery

If there is a break in data transmission while transferring a Command or Parameter or Frame Memory Data before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte retransmitted when the chip select line (CSX) is next activated. See the following example:



If a 1 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

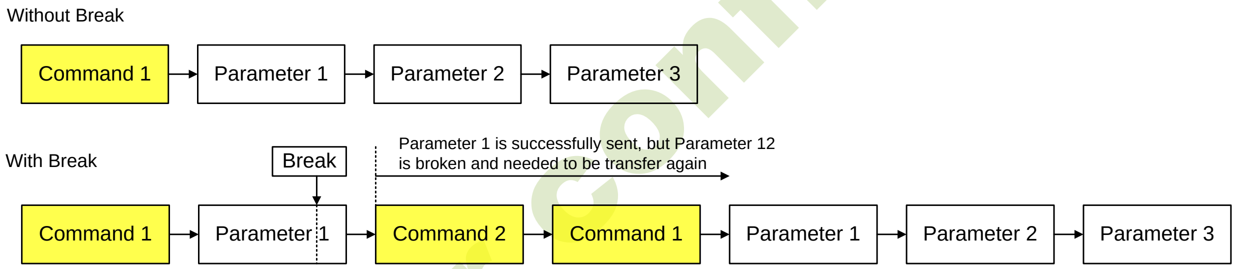


Figure. 7.41 Write interrupts recovery, case 1

If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

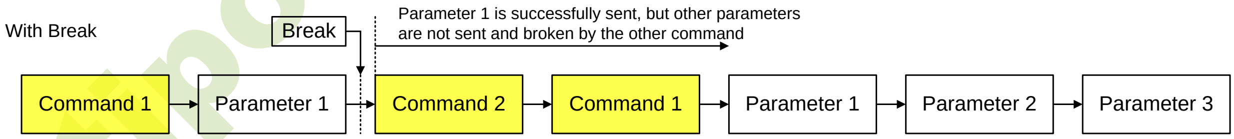


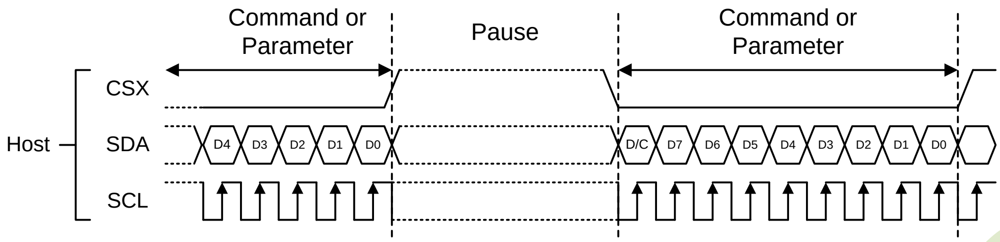
Figure. 7.42 Write interrupts recovery, case 2

7.2.7.Data Transfer Pause

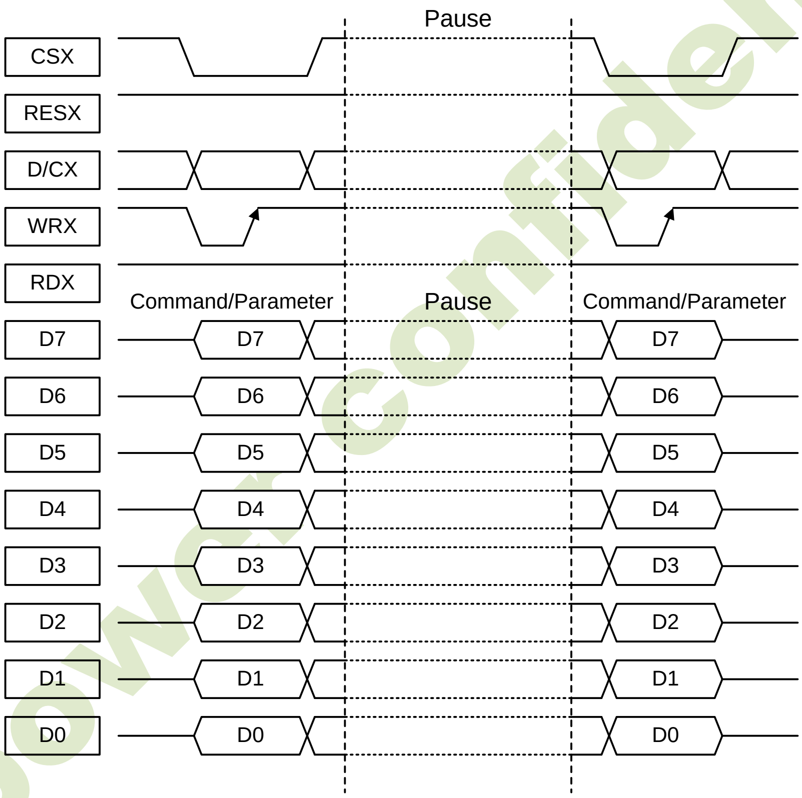
It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then JD9852 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.

This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

7.2.7.1. Serial Interface Pause



7.2.7.2. Parallel Interface Pause

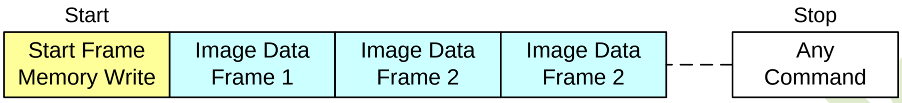


7.2.8. Data Transfer Mode

JD9852 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

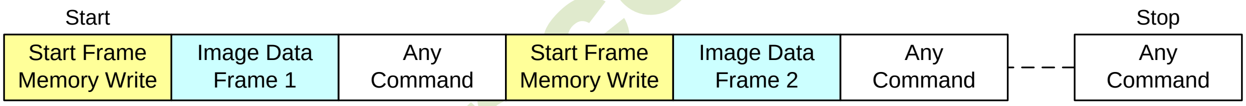
7.2.8.1. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



7.2.8.2. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

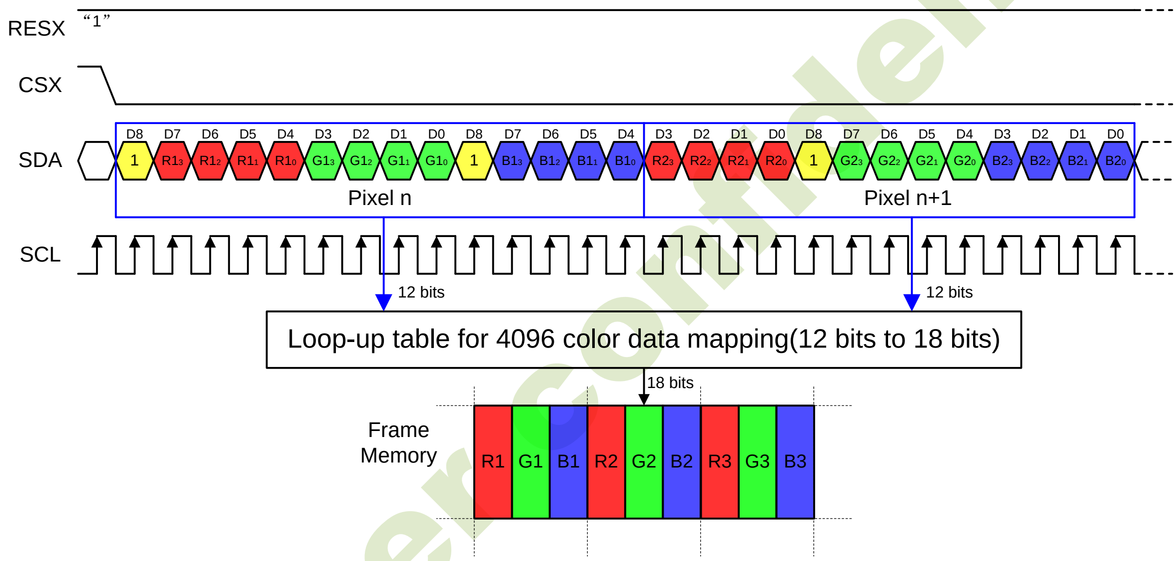
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

7.2.9. Display Module Data Color Coding

7.2.9.1. 3-Line Serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.
4k colors, RGB 4-4-4-bit input
65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input

7.2.9.1.1. R 4-bit, G 4-bit, B 4-bit, 4,096 colors(3Ah=”03h”)

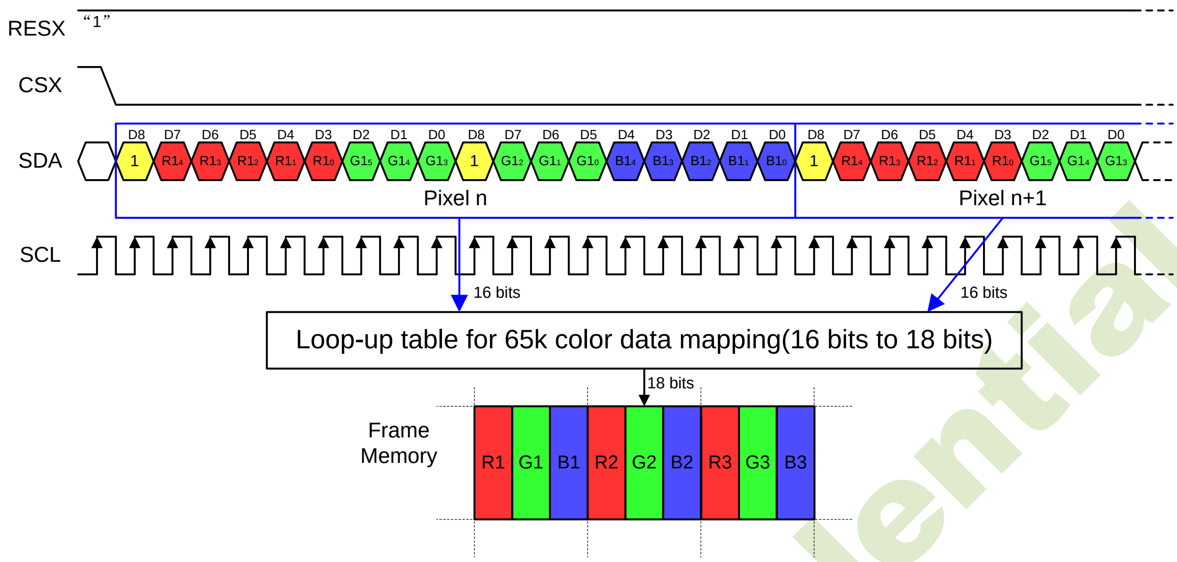


Note 1: Pixel data with the 12-bit color depth information

Note 2: The most significant bits are: Rx3, Gx3 and Bx3

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

7.2.9.1.2. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")

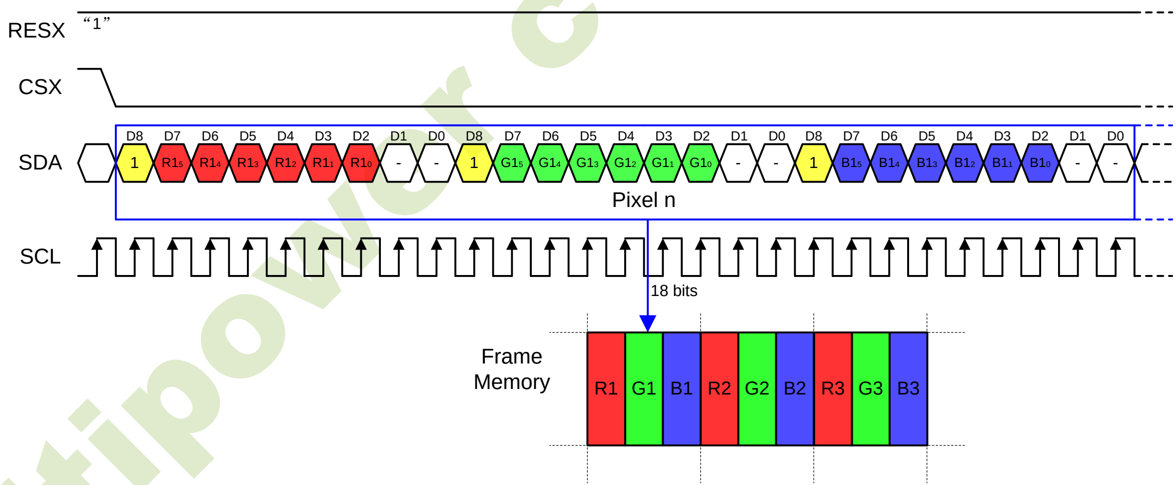


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

7.2.9.1.3. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah="06h")



Note 1: Pixel data with the 18-bit color depth information

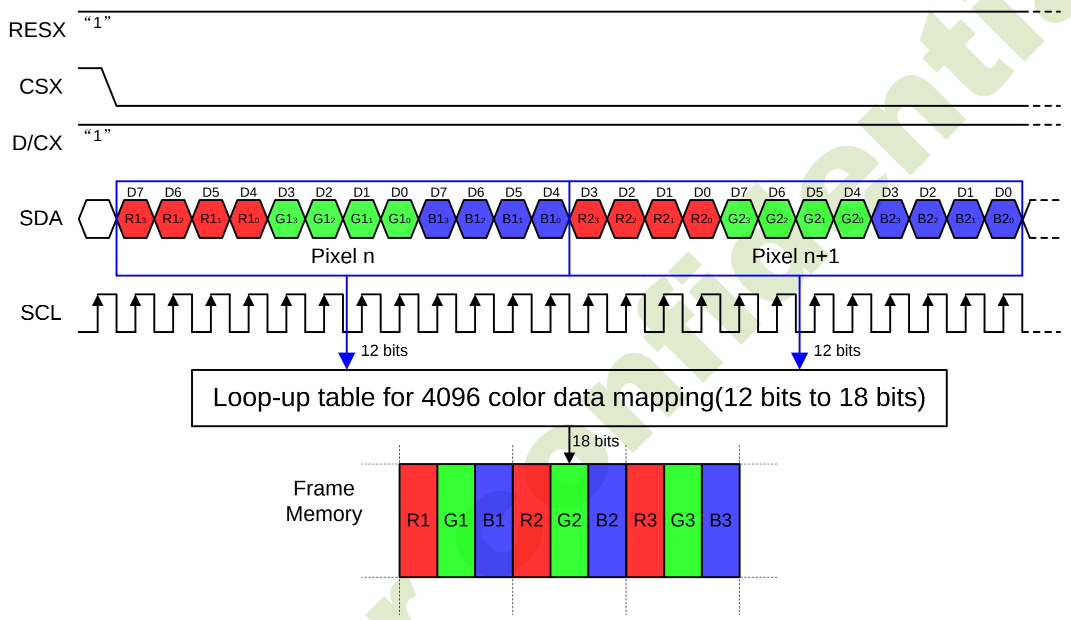
Note 2: The most significant bits are: Rx5, Gx5 and Bx5

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

7.2.9.2. 4-Line Serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.
4k colors, RGB 4-4-4-bit input
65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input

7.2.9.2.1. R 4-bit, G 4-bit, B 4-bit, 4,096 colors(3Ah="03h")

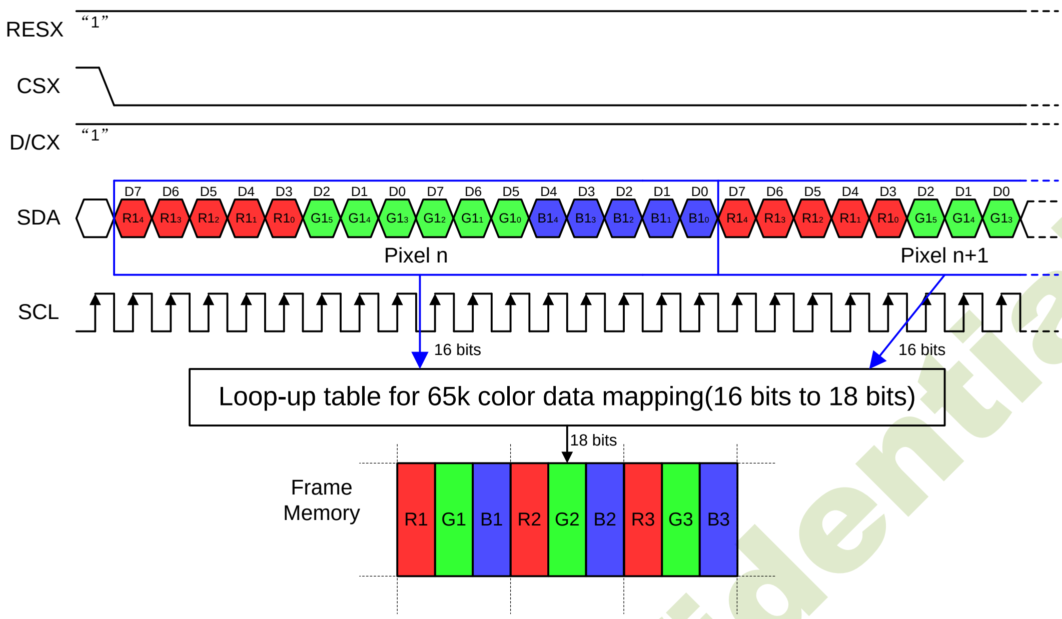


Note 1. pixel data with the 12-bit color depth information

Note 2. The most significant bits are: Rx3, Gx3 and Bx3

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

7.2.9.2.2. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")

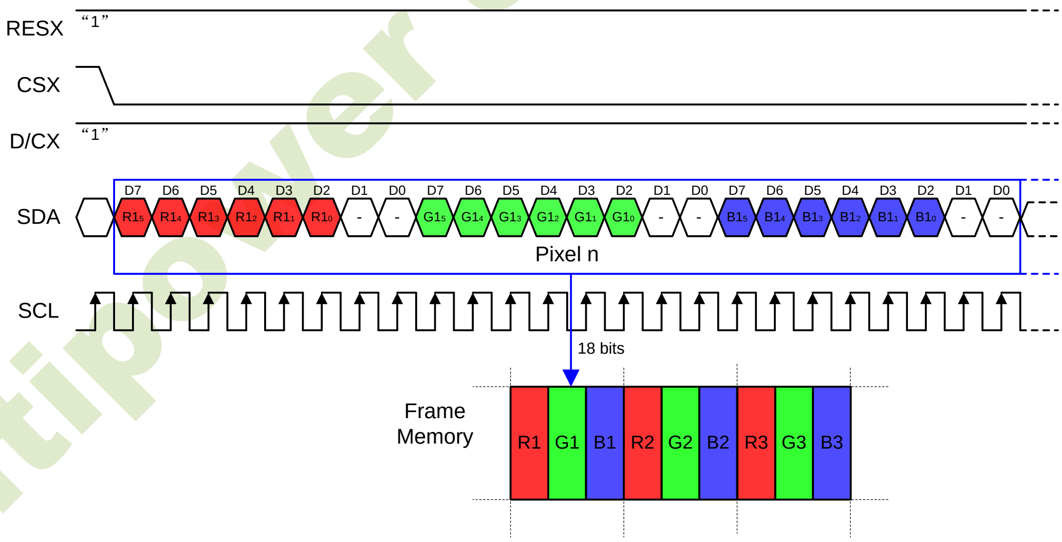


Note 1. pixel data with the 16-bit color depth information

Note 2. The most significant bits are: Rx4, Gx5 and Bx4

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

7.2.9.2.3. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah="06h")



Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

7.2.9.3. 2 Data Lane Interface

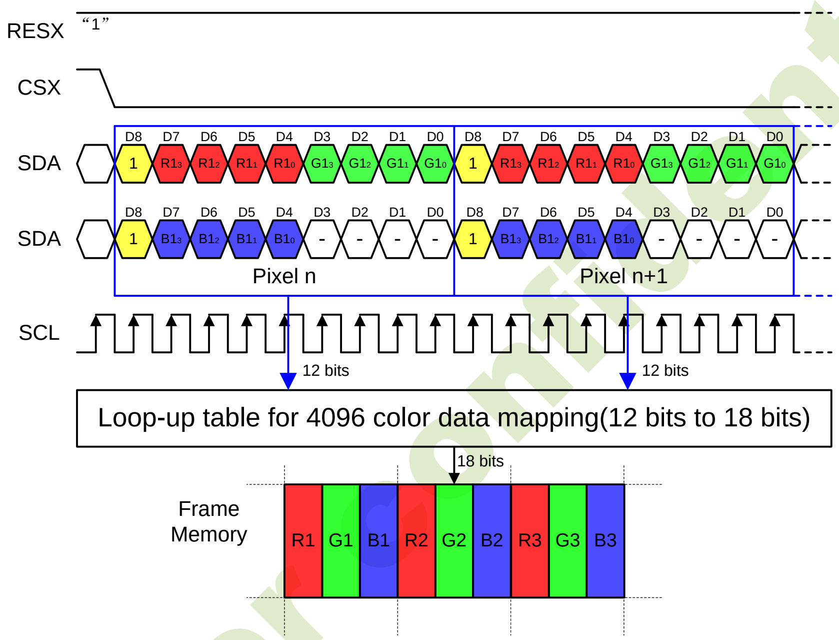
Different display data formats are available for three colors depth supported by the LCM listed below.

4k colors, RGB 4-4-4-bit input

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

7.2.9.3.1. R 4-bit, G 4-bit, B 4-bit, 4,096 colors(3Ah=”03h”)

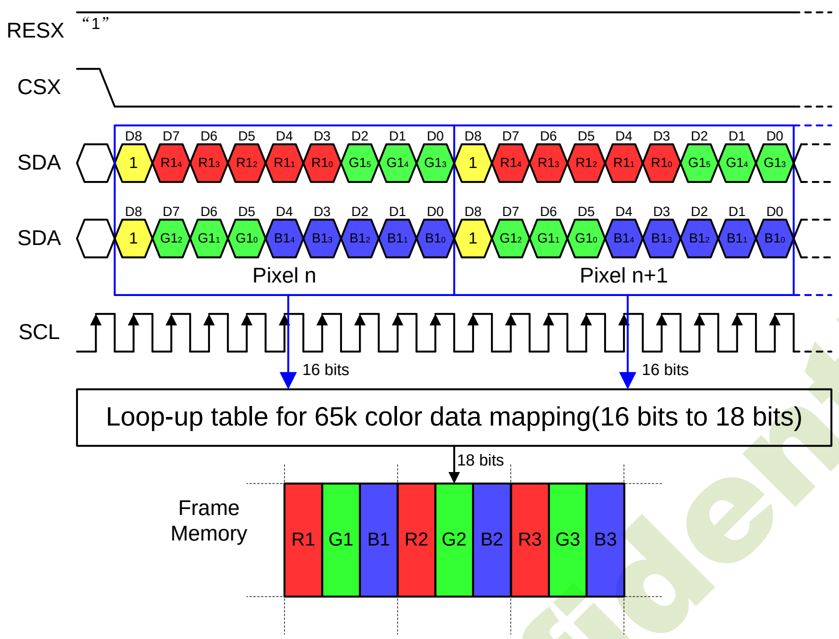


Note 1: Pixel data with the 12-bit color depth information

Note 2: The most significant bits are: Rx3, Gx3 and Bx3

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

7.2.9.3.2. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")

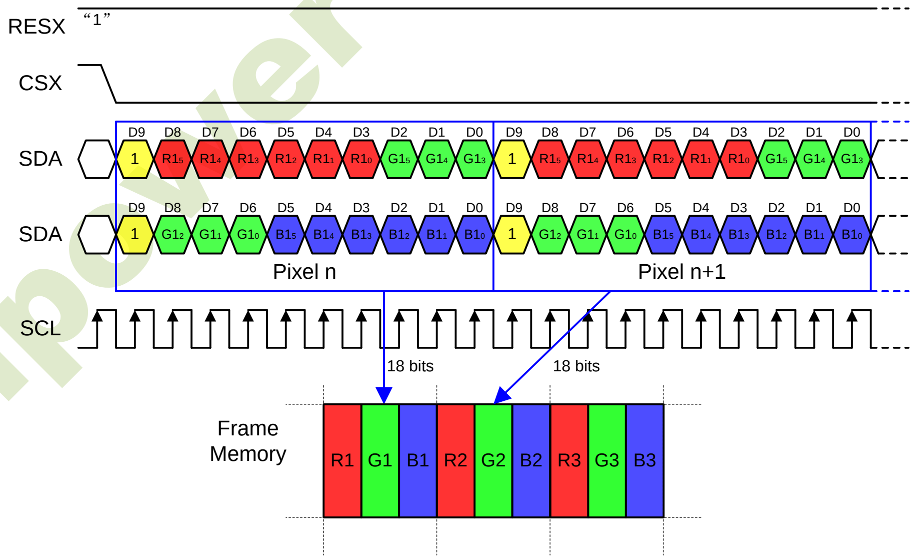


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

7.2.9.3.3. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah="06h")



Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

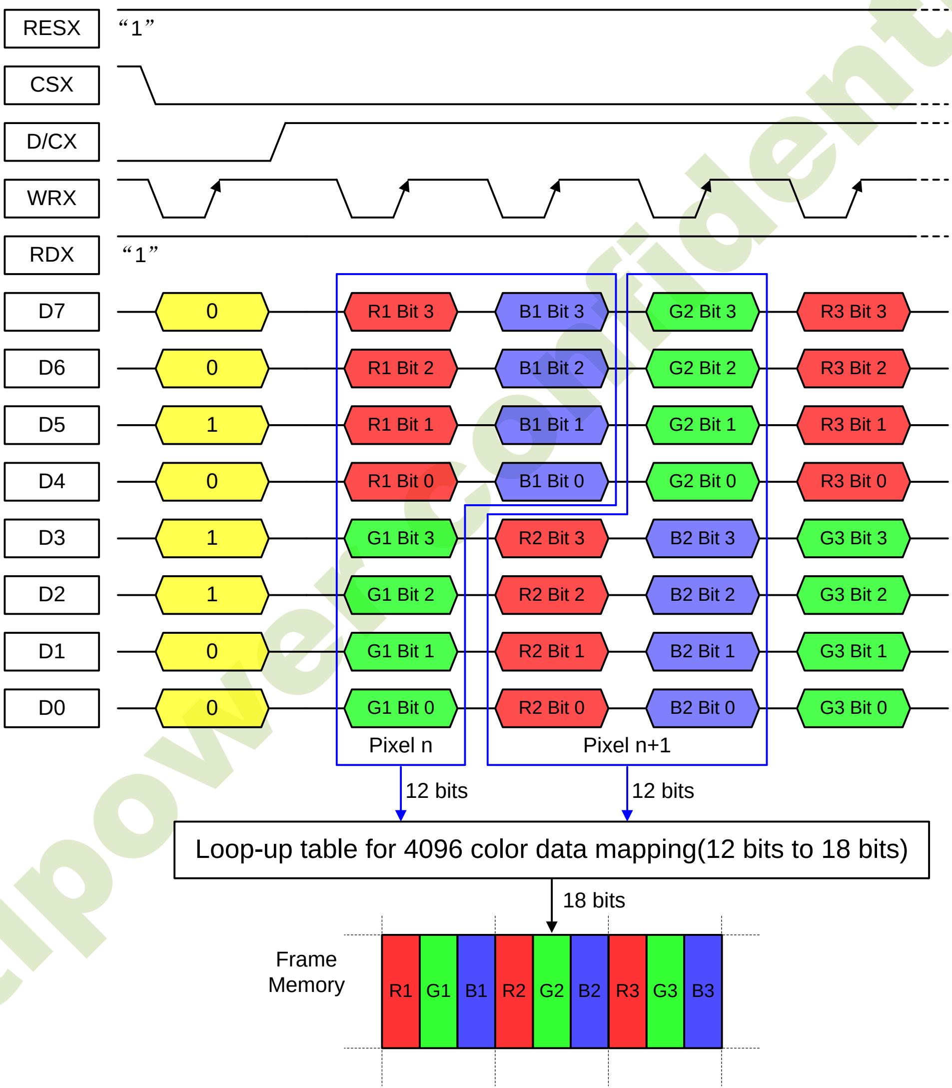
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

7.2.9.4. 8080-Ⅰ series 8-bit Parallel Interface

The 8080-Ⅰ series 8-bit parallel interface of JD9852 can be used by setting IM[3:0]="0000b". Different display data formats are available for three Colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input.
- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

7.2.9.4.1. R 4-bit, G 4-bit, B 4-bit, 4,096 colors(3Ah="03h")

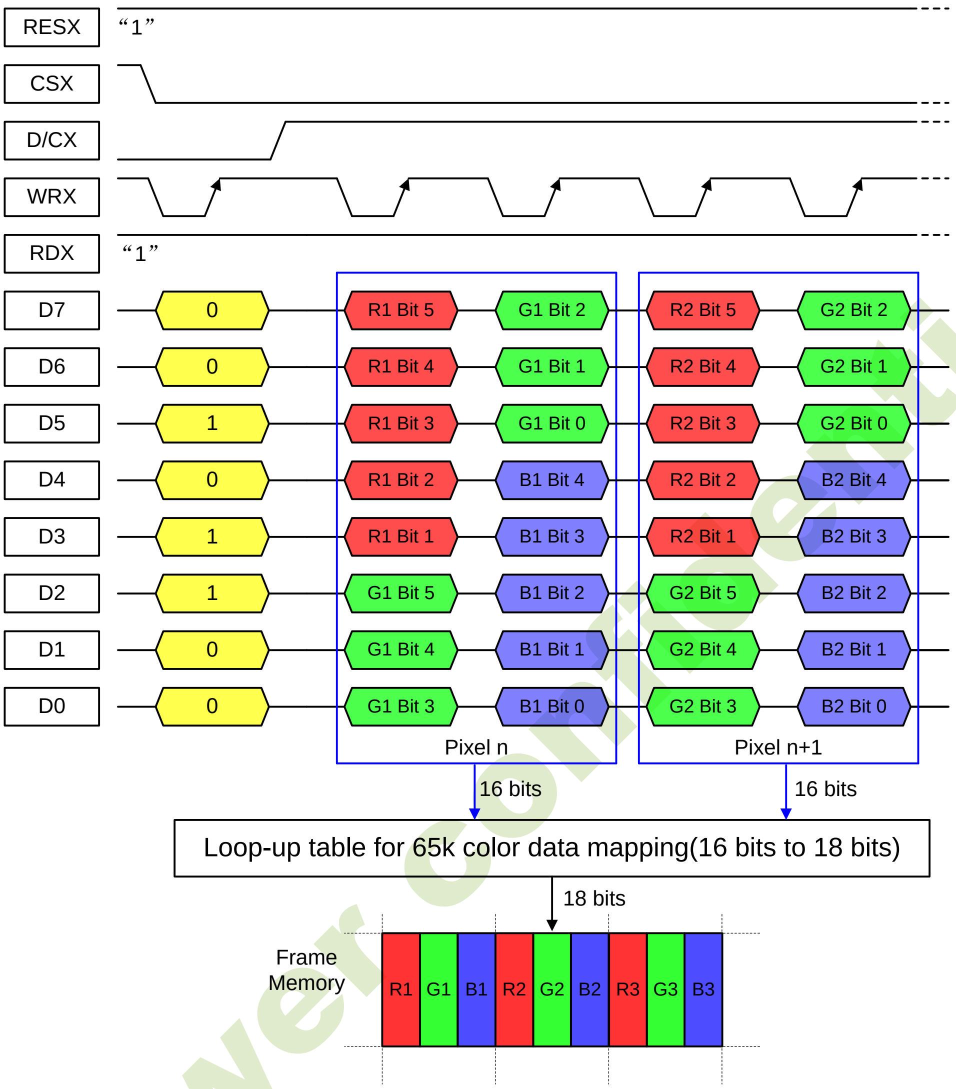


Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-time transfer is used to transmit 2 pixel data with the 12-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

7.2.9.4.2. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")

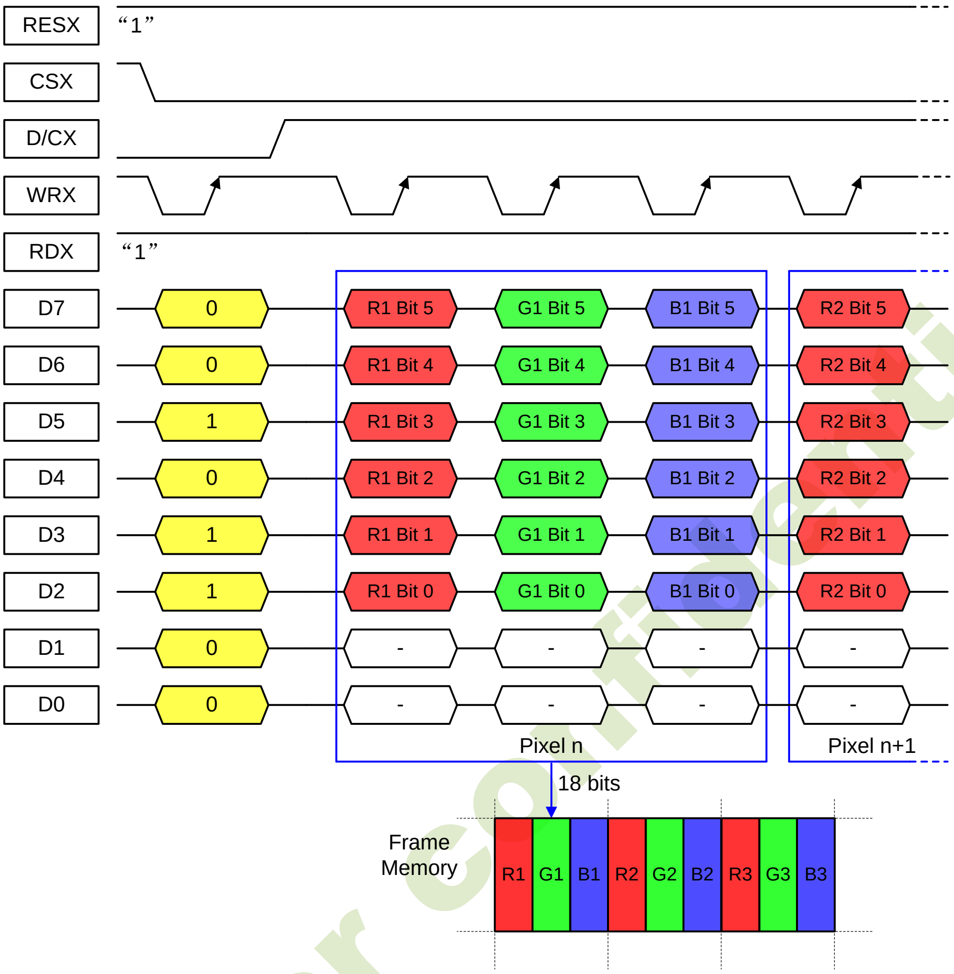


Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

7.2.9.4.3. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h”)



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

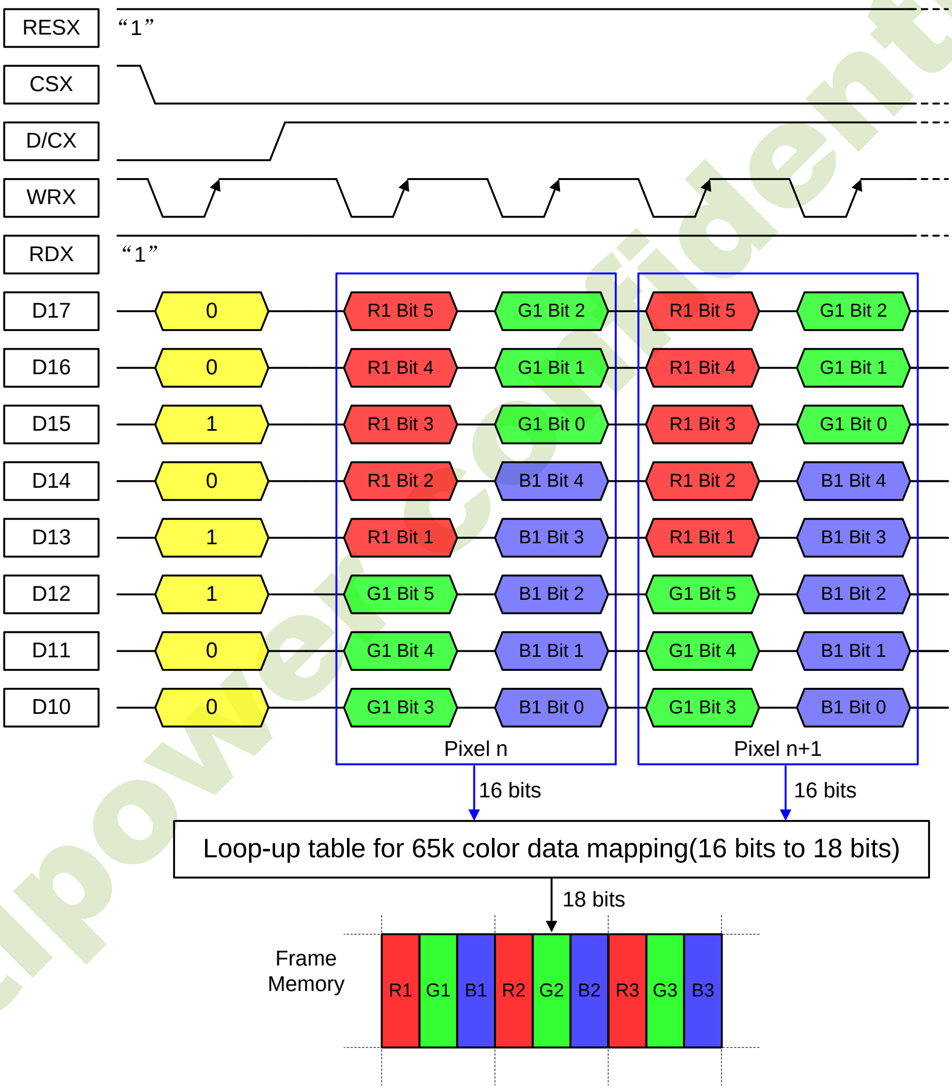
Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.5. 8080-Ⅱ series 8-bit Parallel Interface

The 8080-Ⅱ series 8-bit parallel interface of JD9852 can be used by setting IM[3:0]="1001b". Different display data formats are available for three Colors depth supported by listed below.
- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

7.2.9.5.1. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")

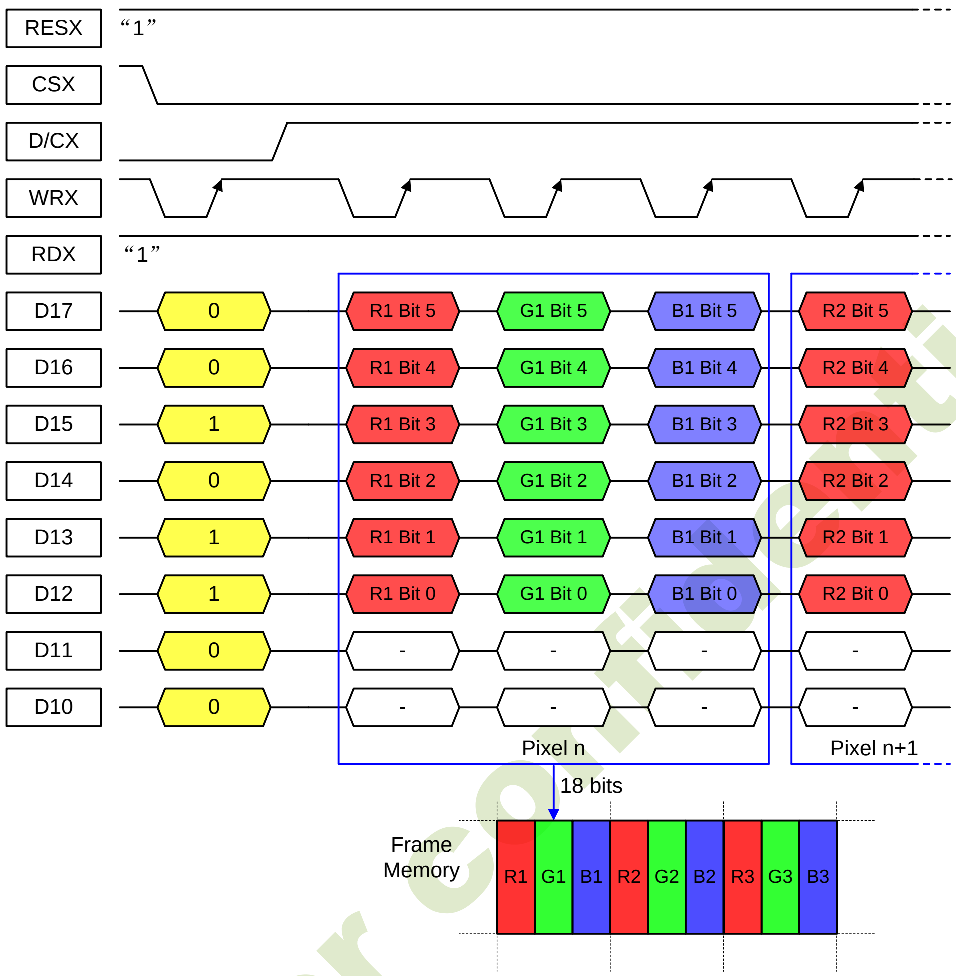


Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

7.2.9.5.2. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h”)



Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

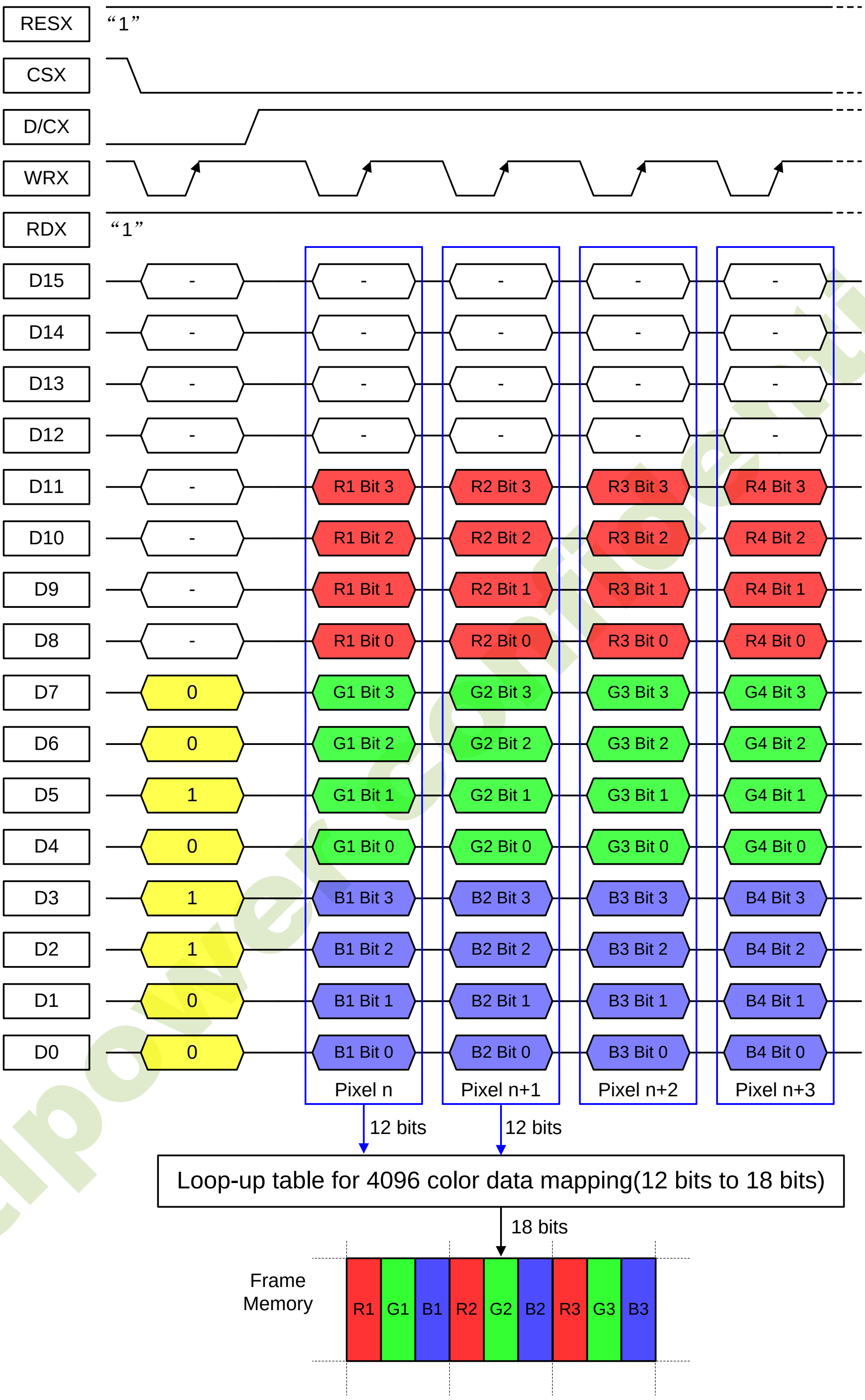
Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.6. 8080-Ⅰ series 16-Bit Parallel Interface

The 8080-Ⅰ series 16-bit parallel interface of JD9852 can be used by setting IM[3:0]="0001b".
Different display data formats are available for three colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

7.2.9.6.1. R 4-bit, G 4-bit, B 4-bit, 4,096 colors(3Ah=”03h”)

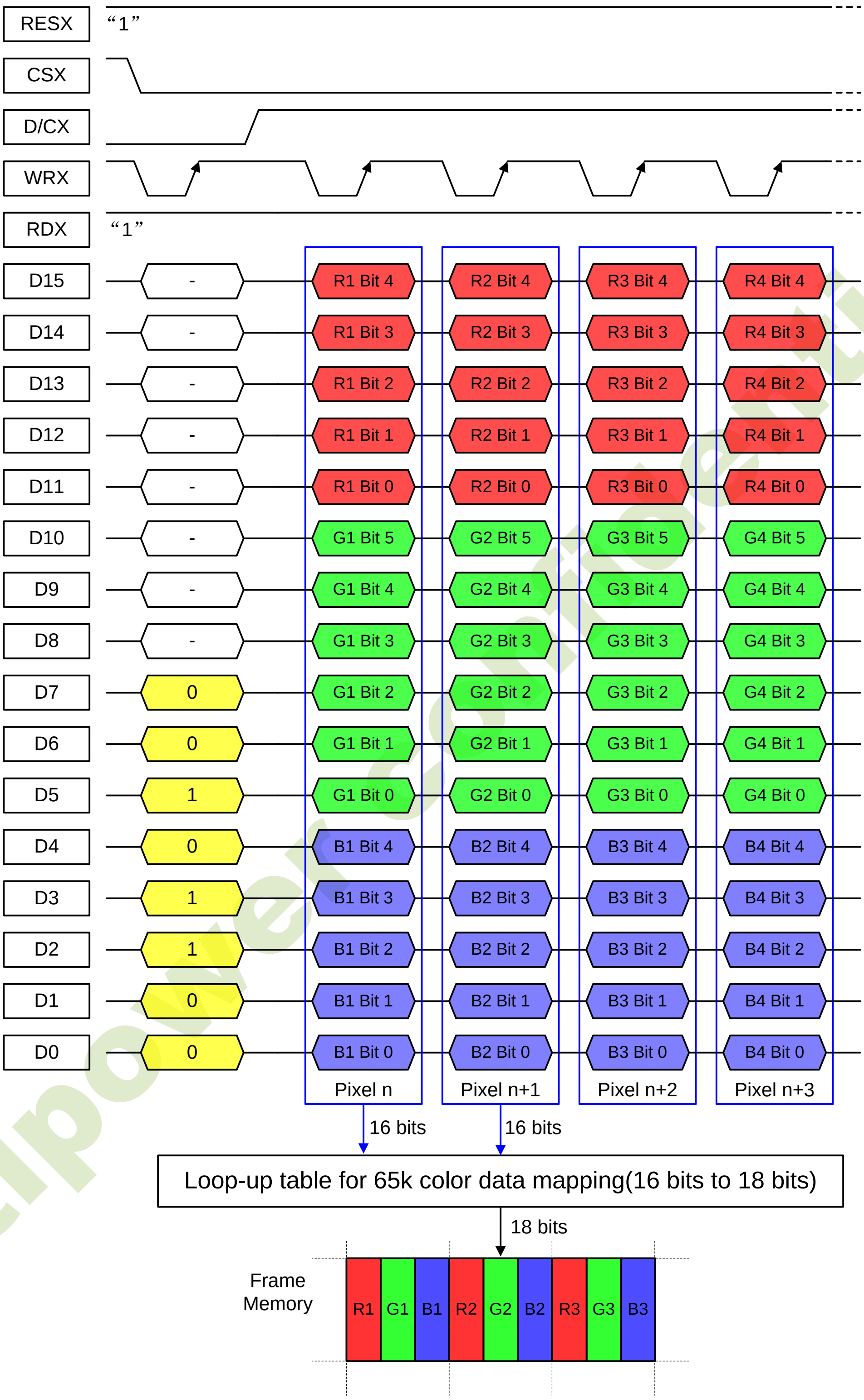


Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 1-time transfer (D11 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.6.2. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah=”05h”)

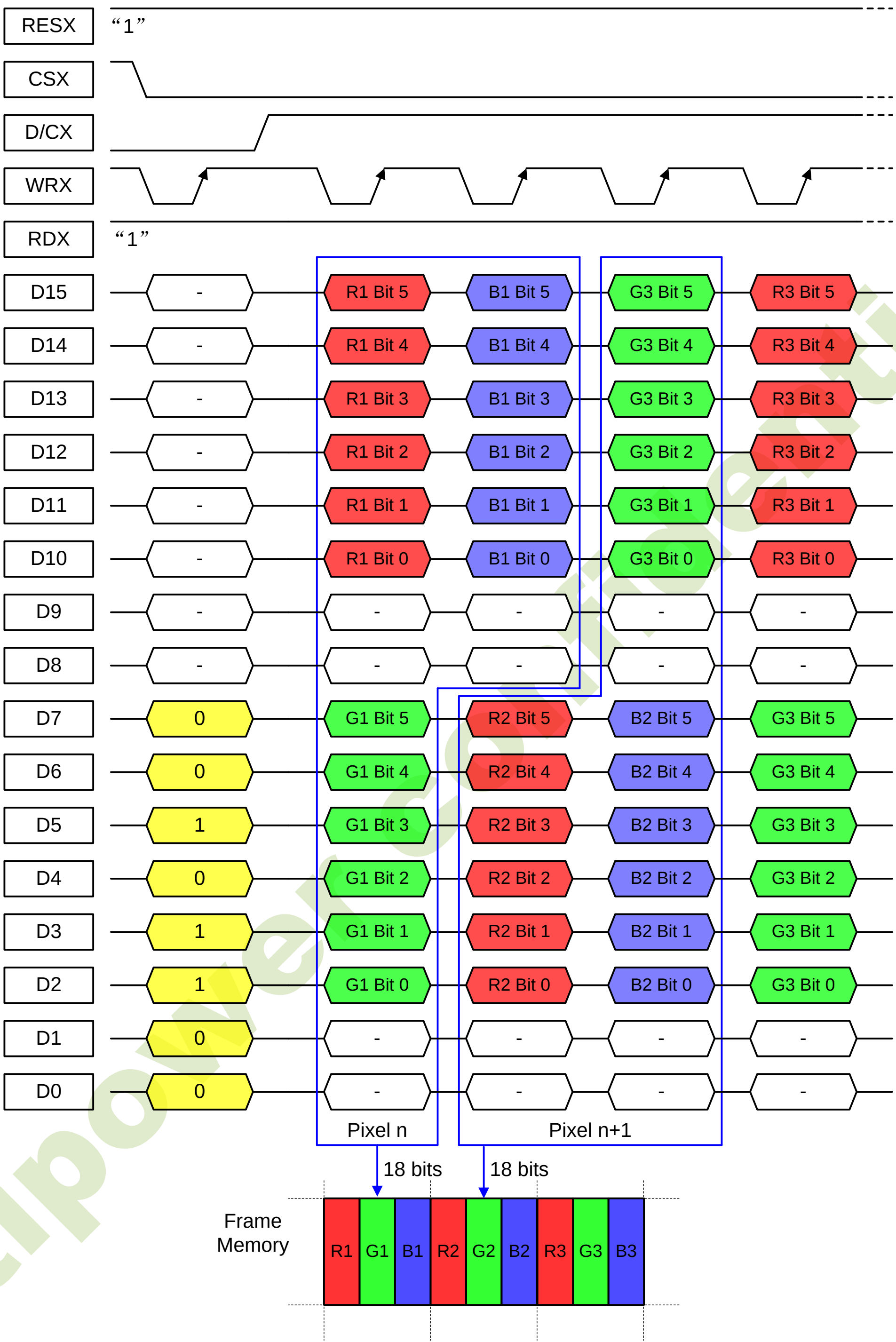


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.6.3. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah="06h", MDT="00b")

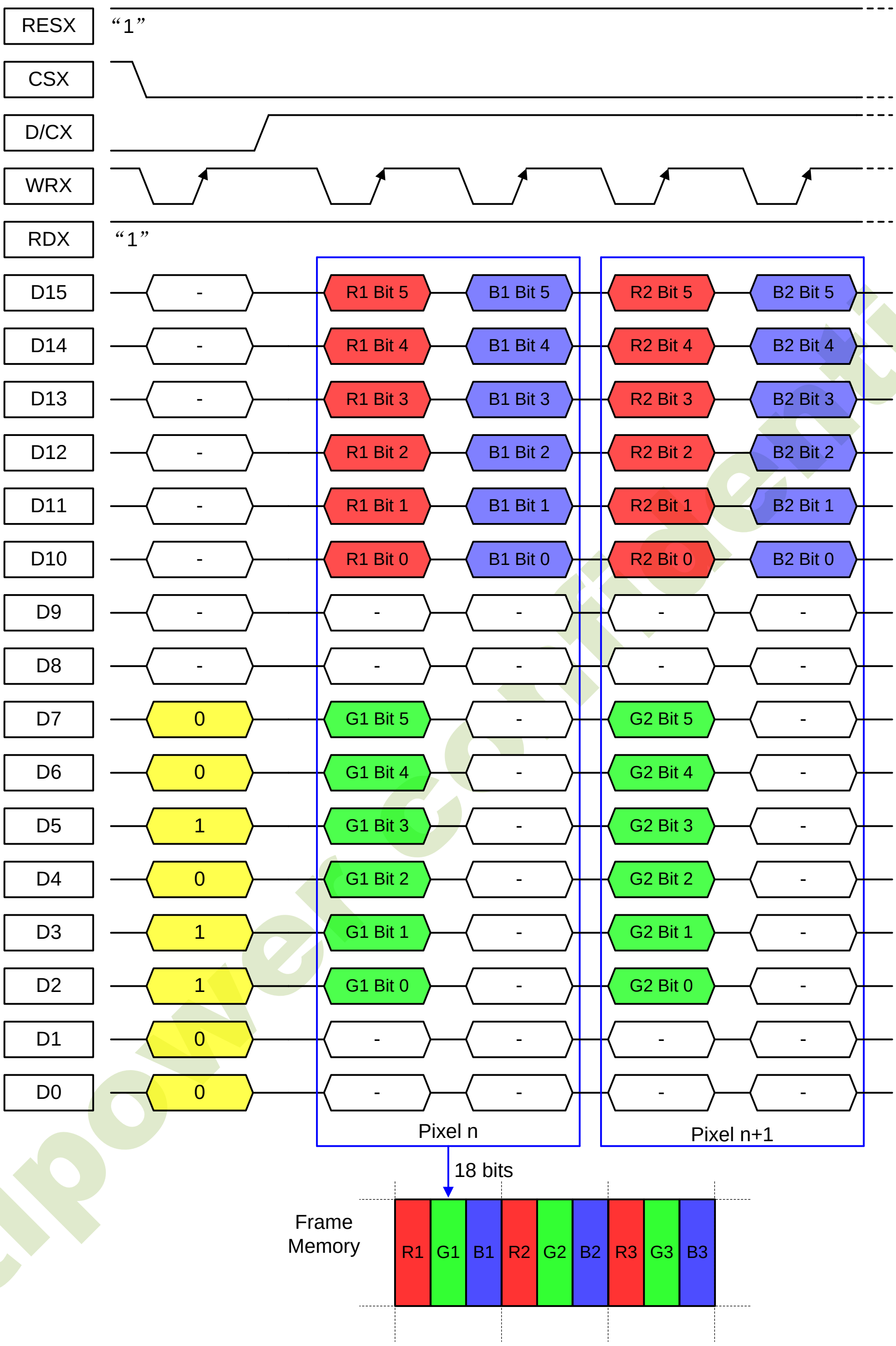


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 2 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

7.2.9.6.4. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h”, MDT=”01b”)

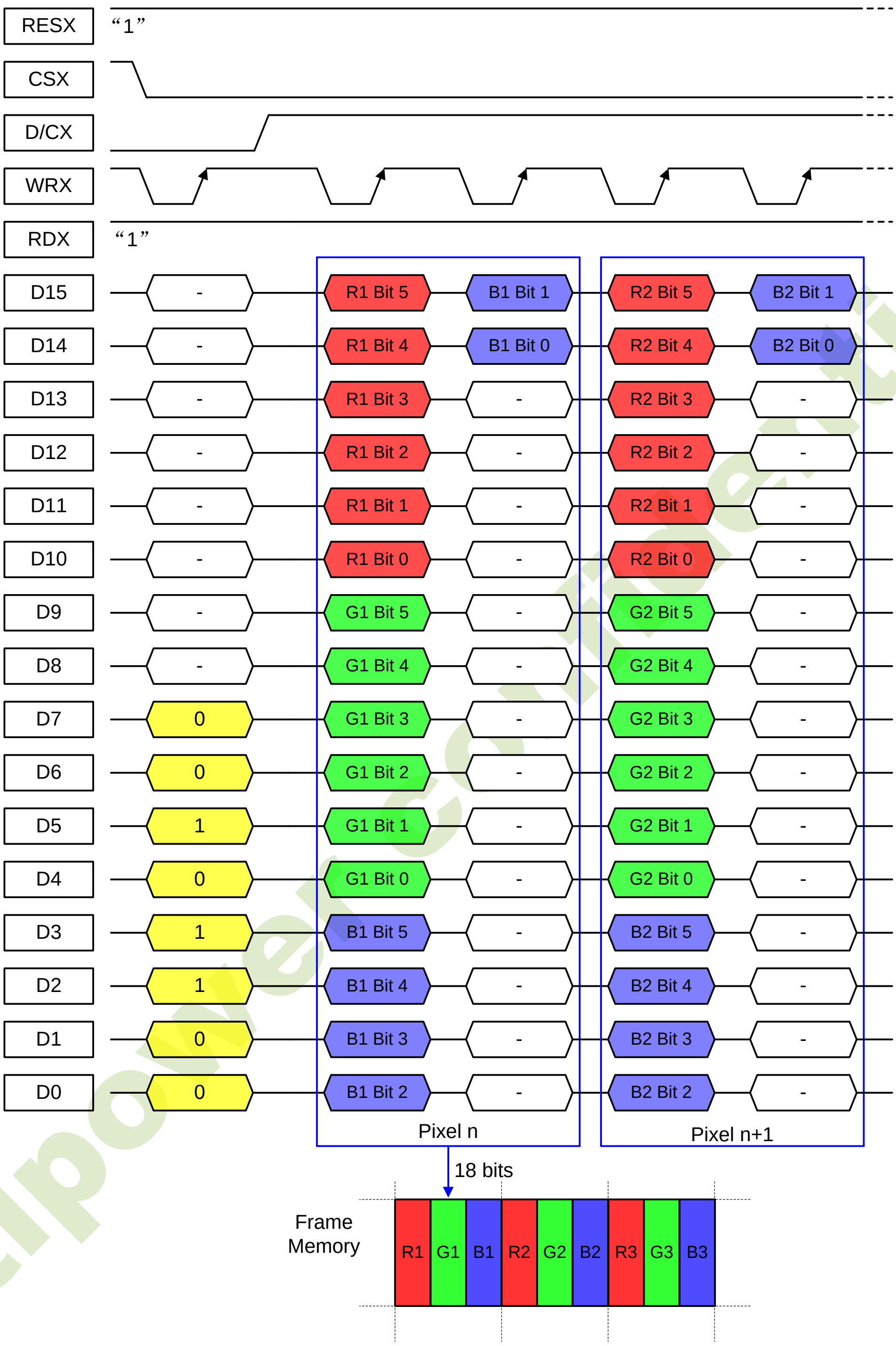


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.6.5. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h”, MDT=”10b”)

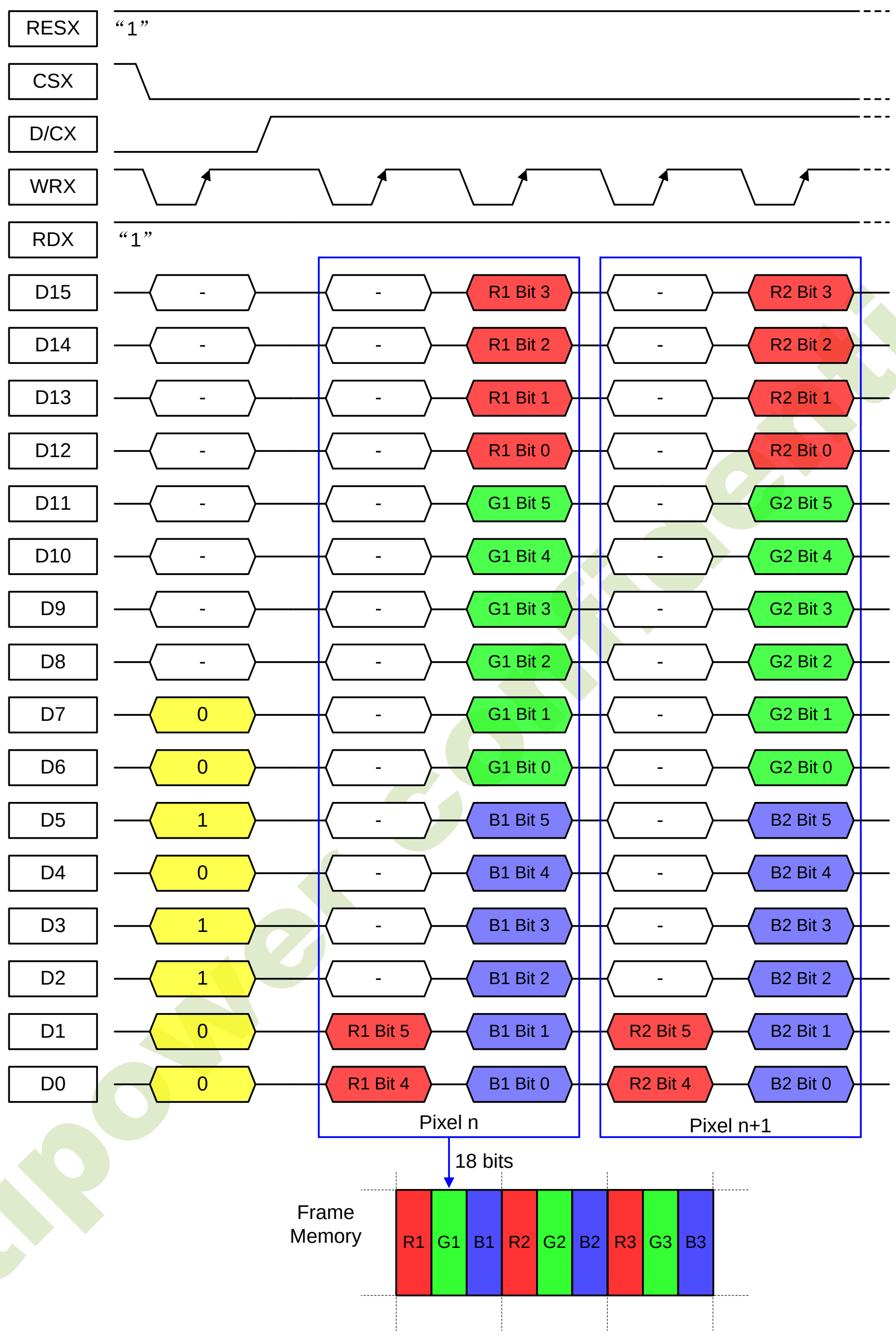


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.6.6. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h”, MDT=”11b”)



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

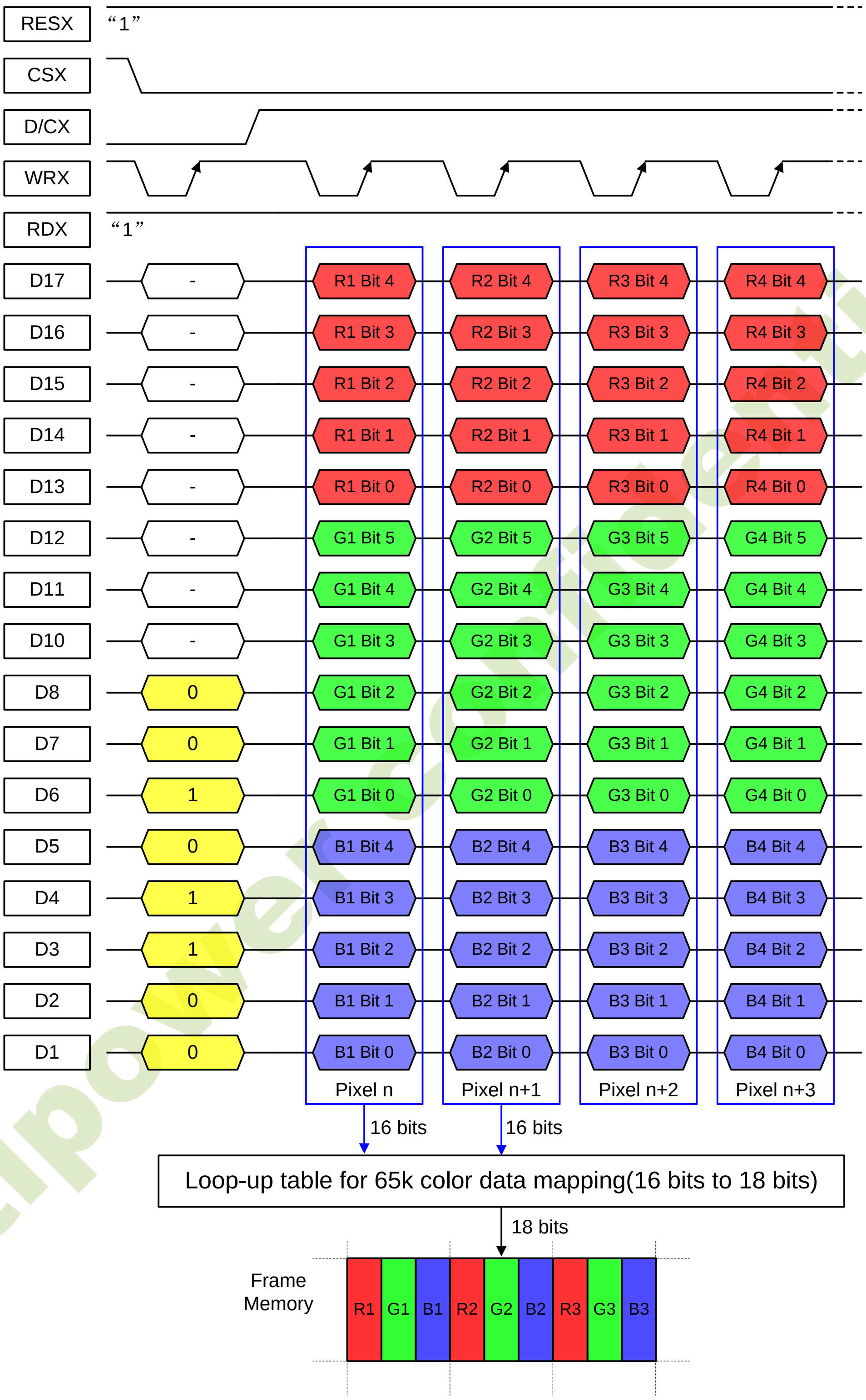
Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.7. 8080-Ⅱ series 16-Bit Parallel Interface

The 8080-Ⅱ series 16-bit parallel interface of JD9852 can be used by setting IM[3:0]="1000b".
Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

7.2.9.7.1. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah=”05h”)

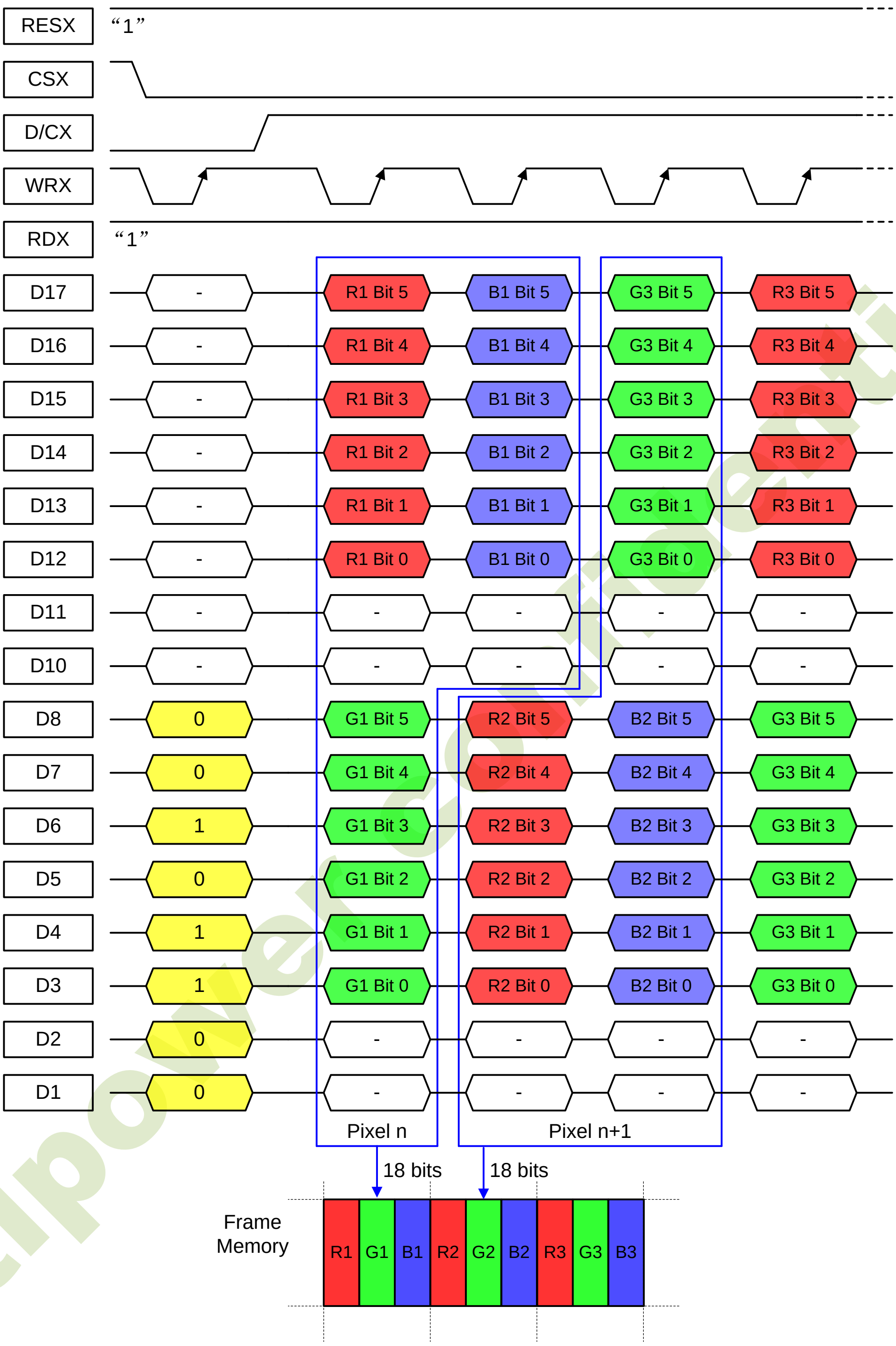


Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer (D17~D10, D8~D1) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.7.2. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah="06h, MDT="00b")

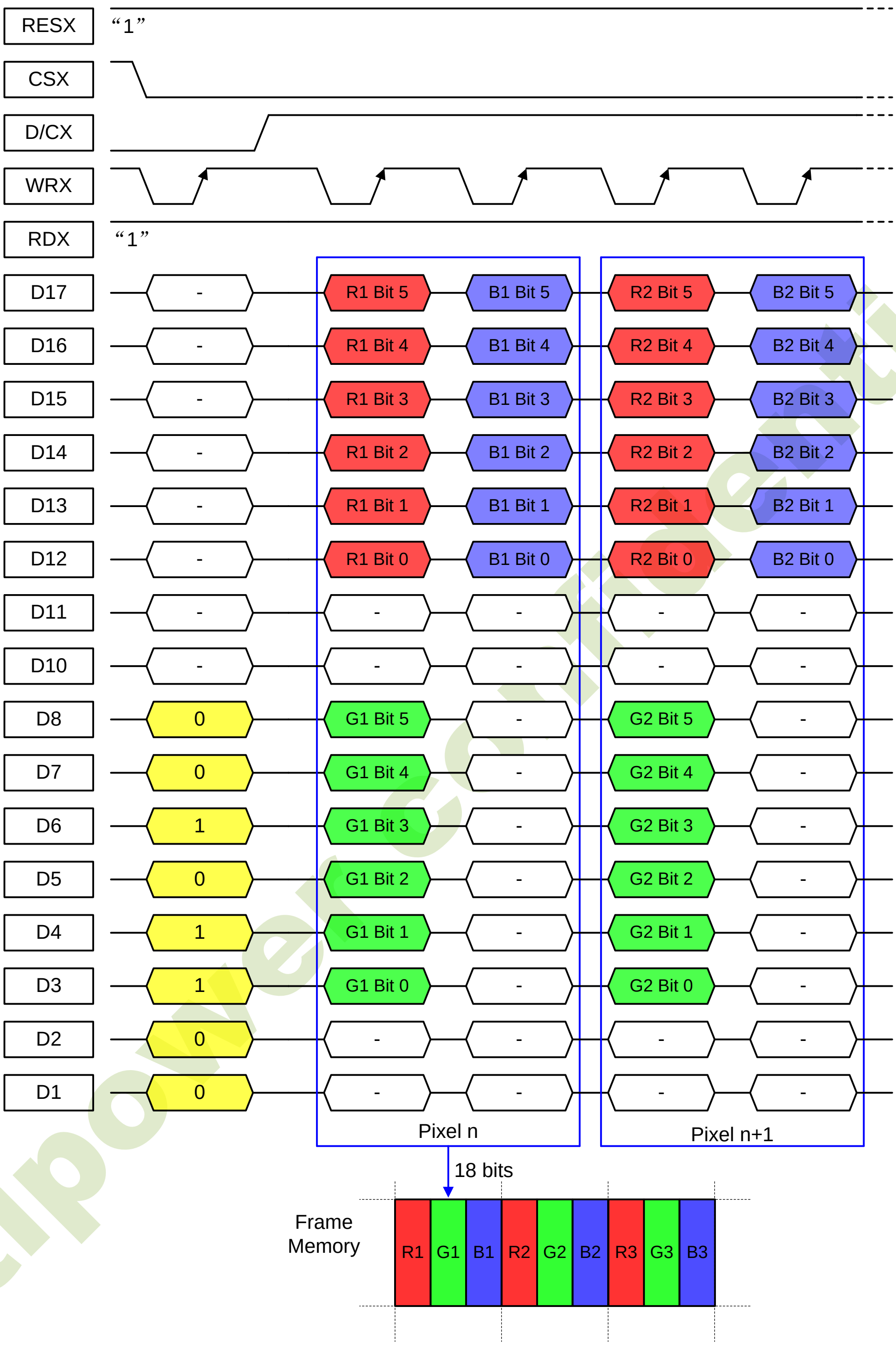


Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 2 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

7.2.9.7.3. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h, MDT=”01b”)

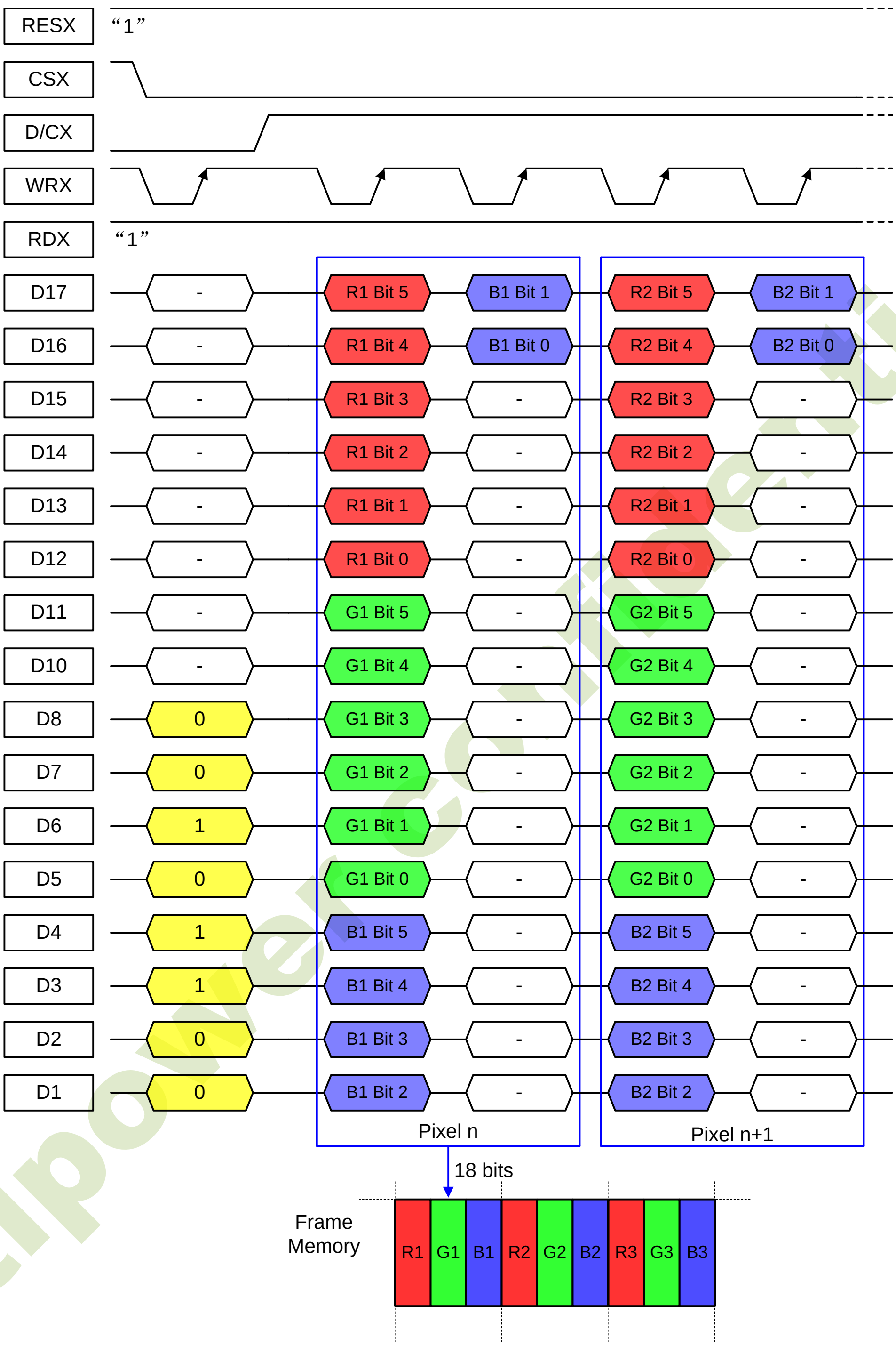


Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.7.4. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h, MDT=”10b”)

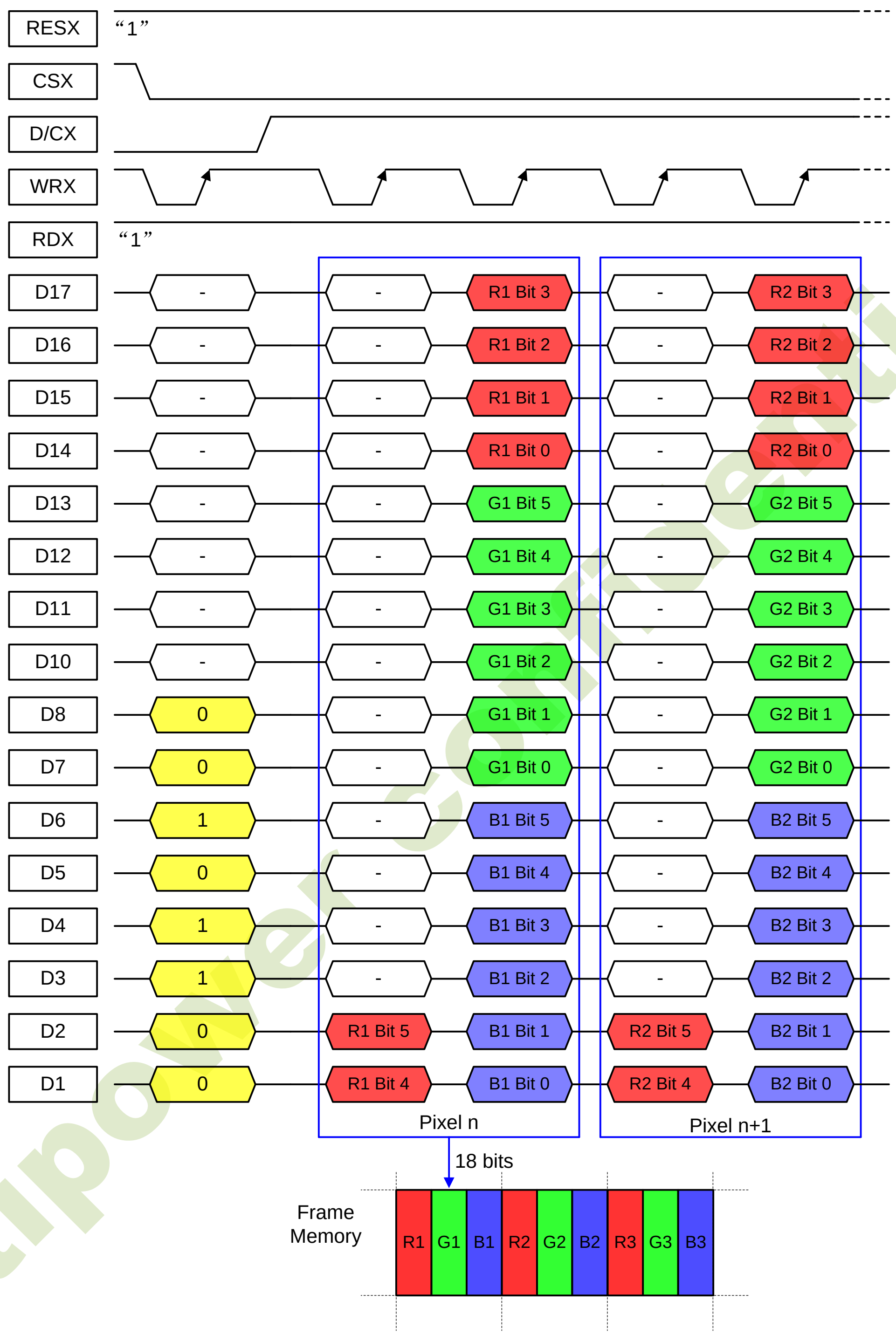


Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.7.5. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h, MDT=”11b”)



Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

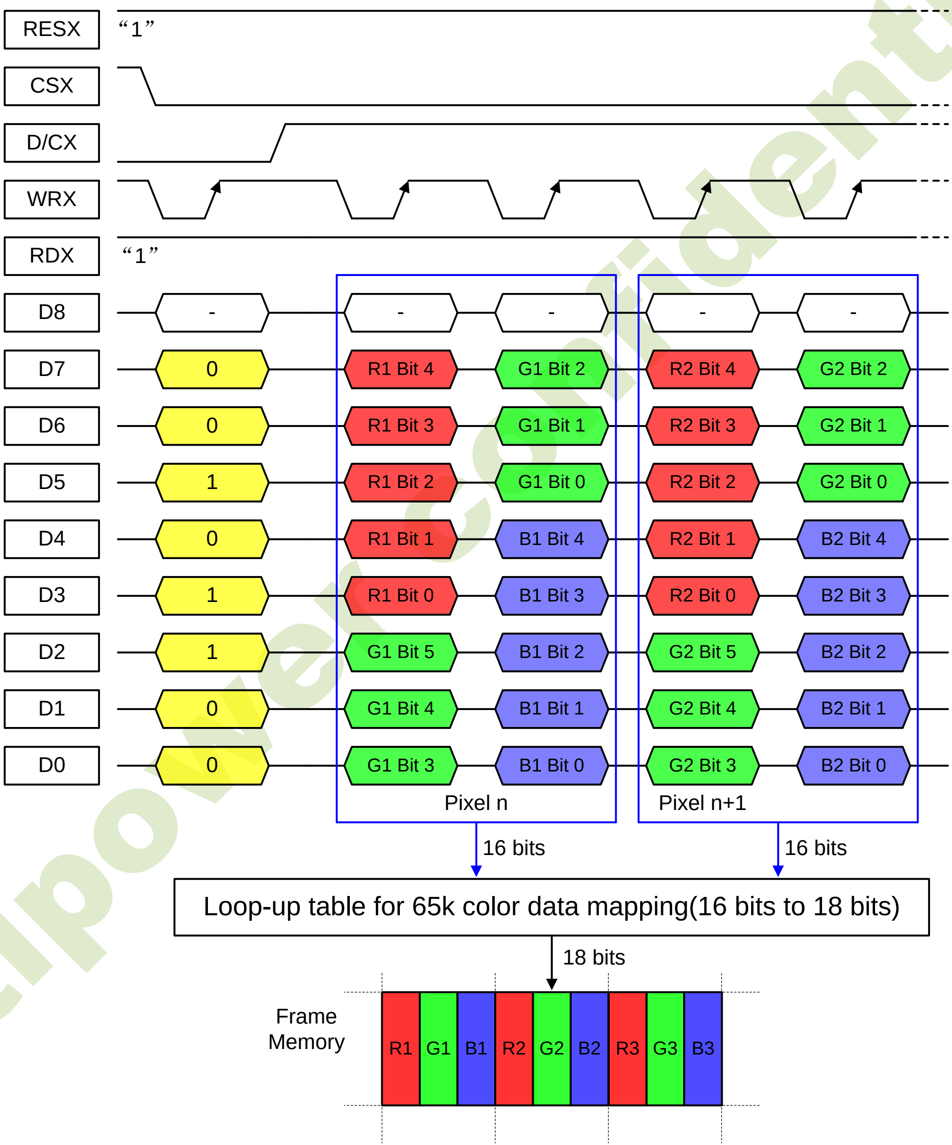
7.2.9.8. 8080- Ⅰ series 9-Bit Parallel Interface

The 8080- Ⅰ series 9-bit parallel interface of JD9852 can be used by setting IM[3:0]="0010b"Different display data formats are available for two colors depth supported by listed below.

-65k colors, RGB 5,6,5-bit input

-262k colors, RGB 6,6,6-bit input

7.2.9.8.1. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")

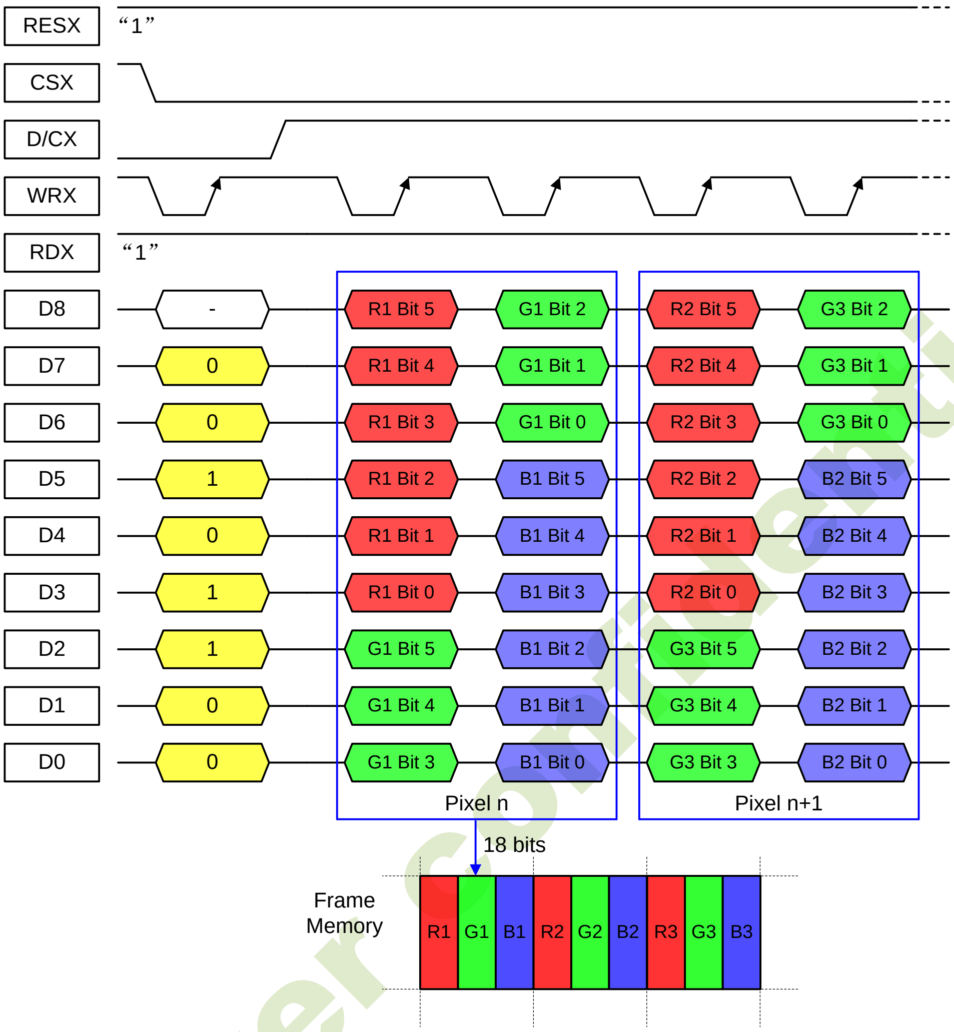


Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

7.2.9.8.2. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h, MDT=”00b”)

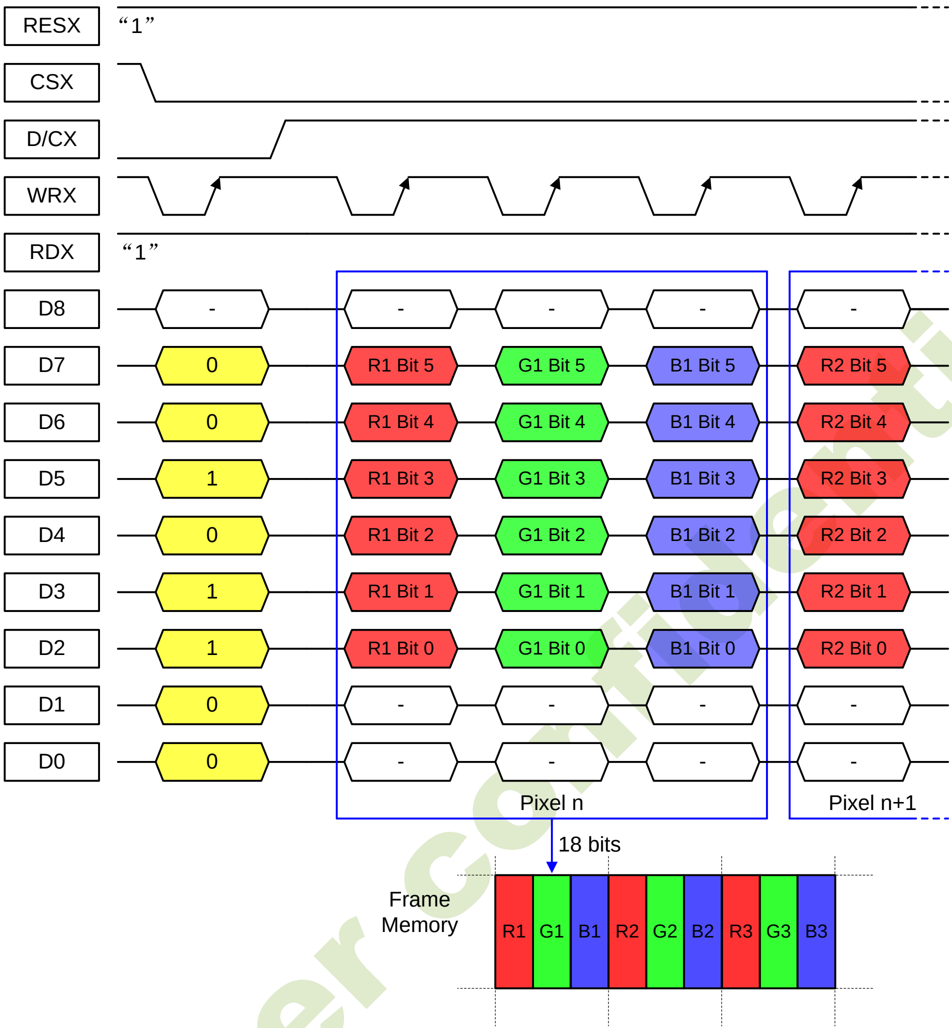


Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.8.3. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah="06h, MDT="01b")



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

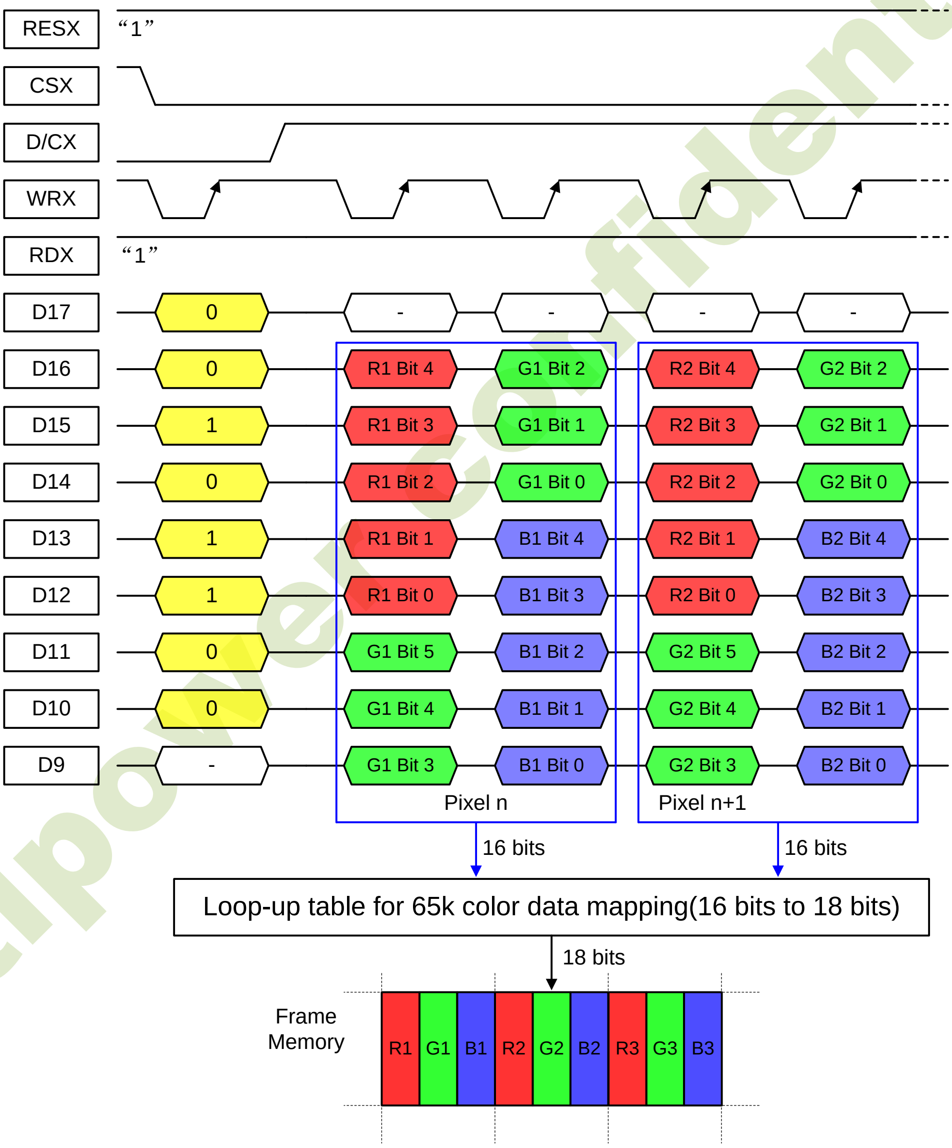
7.2.9.9. 8080-Ⅱ series 9-bit Parallel Interface

The 8080-Ⅱ series 9-bit parallel interface of JD9852 can be used by setting IM[3:0]="1011b"Different display data formats are available for two colors depth supported by listed below.

-65k colors, RGB 5,6,5-bit input

-262k colors, RGB 6,6,6-bit input

7.2.9.9.1. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah="05h")

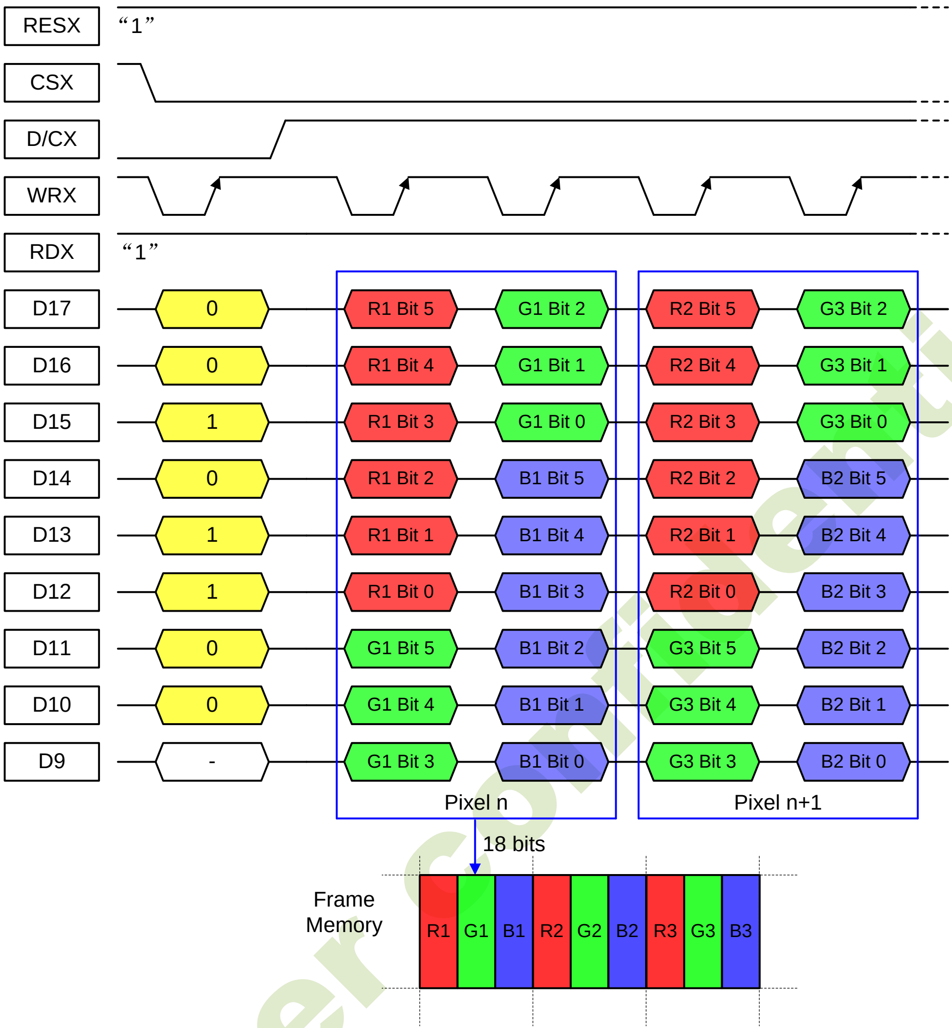


Note 1: The data order is as follows, MSB=D17, LSB=D9 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data..

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

7.2.9.9.2. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h, MDT=”00b”)

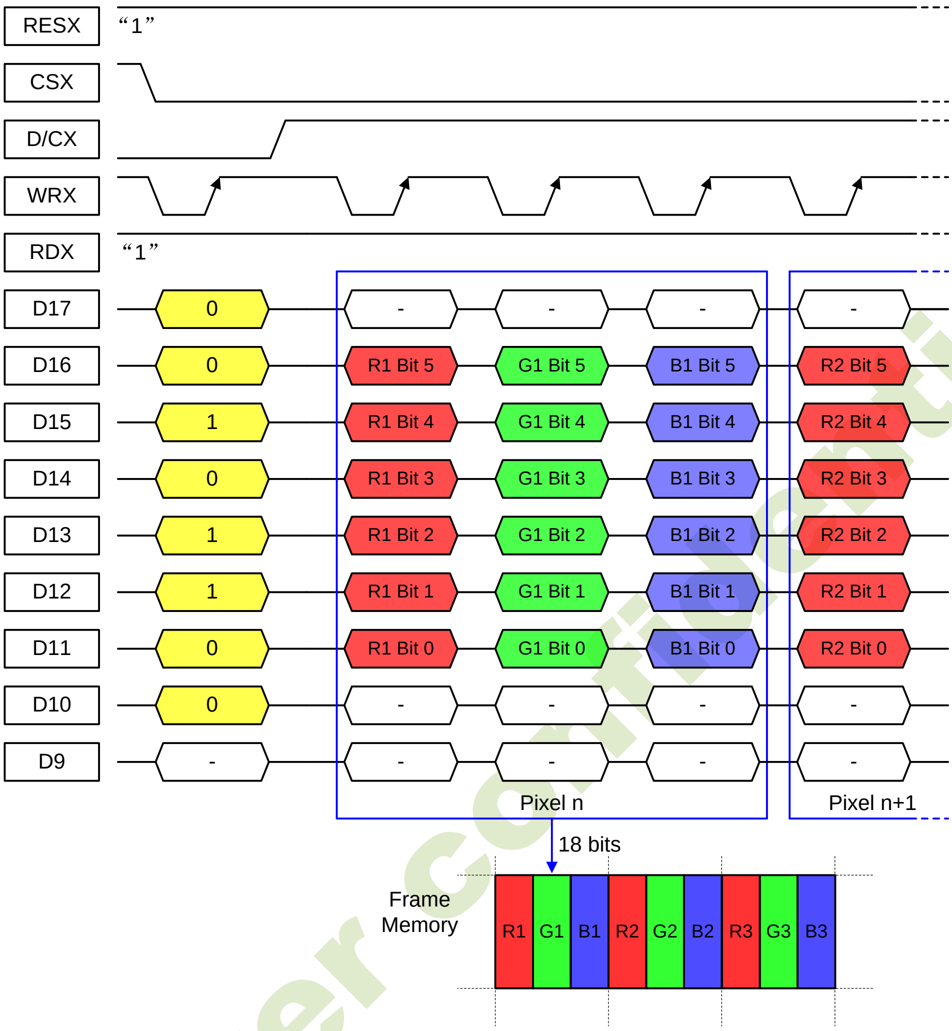


Note 1: The data order is as follows, MSB=D17, LSB=D9 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.9.3. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h, MDT=”01b”)



Note 1: The data order is as follows, MSB=D17, LSB=D9 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

7.2.9.10. 8080-Ⅰ series 18-Bit Parallel Interface

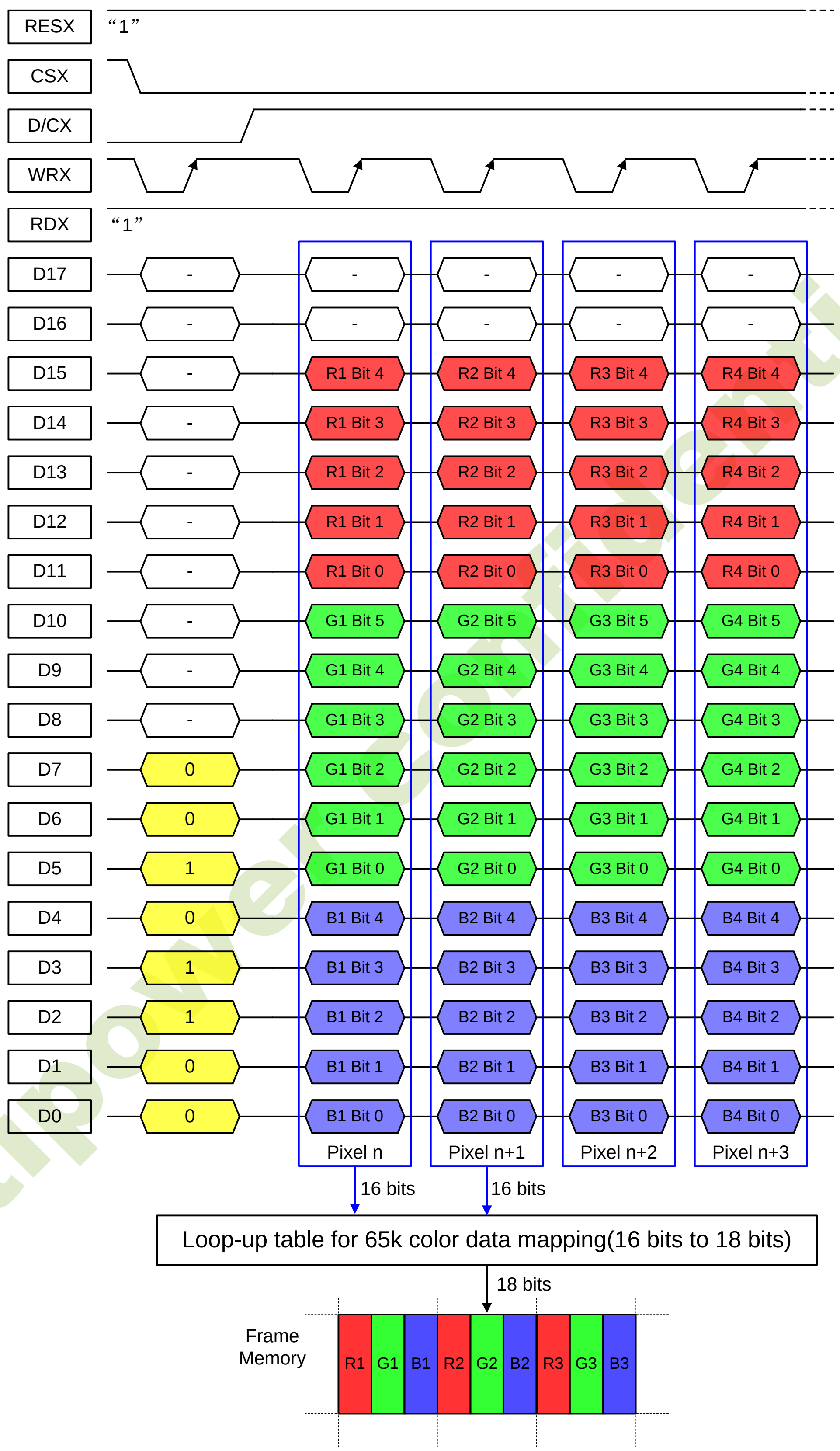
The 8080-Ⅰ series 18-bit parallel interface of JD9852 can be used by setting IM[3:0]="0011b".
Different display data formats are available for three colors depth supported by listed below.
- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

7.2.9.10.1. R 4-bit, G 4-bit, B 4-bit, 4,096 colors(3Ah="03h")

Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 12-bit color depth information.

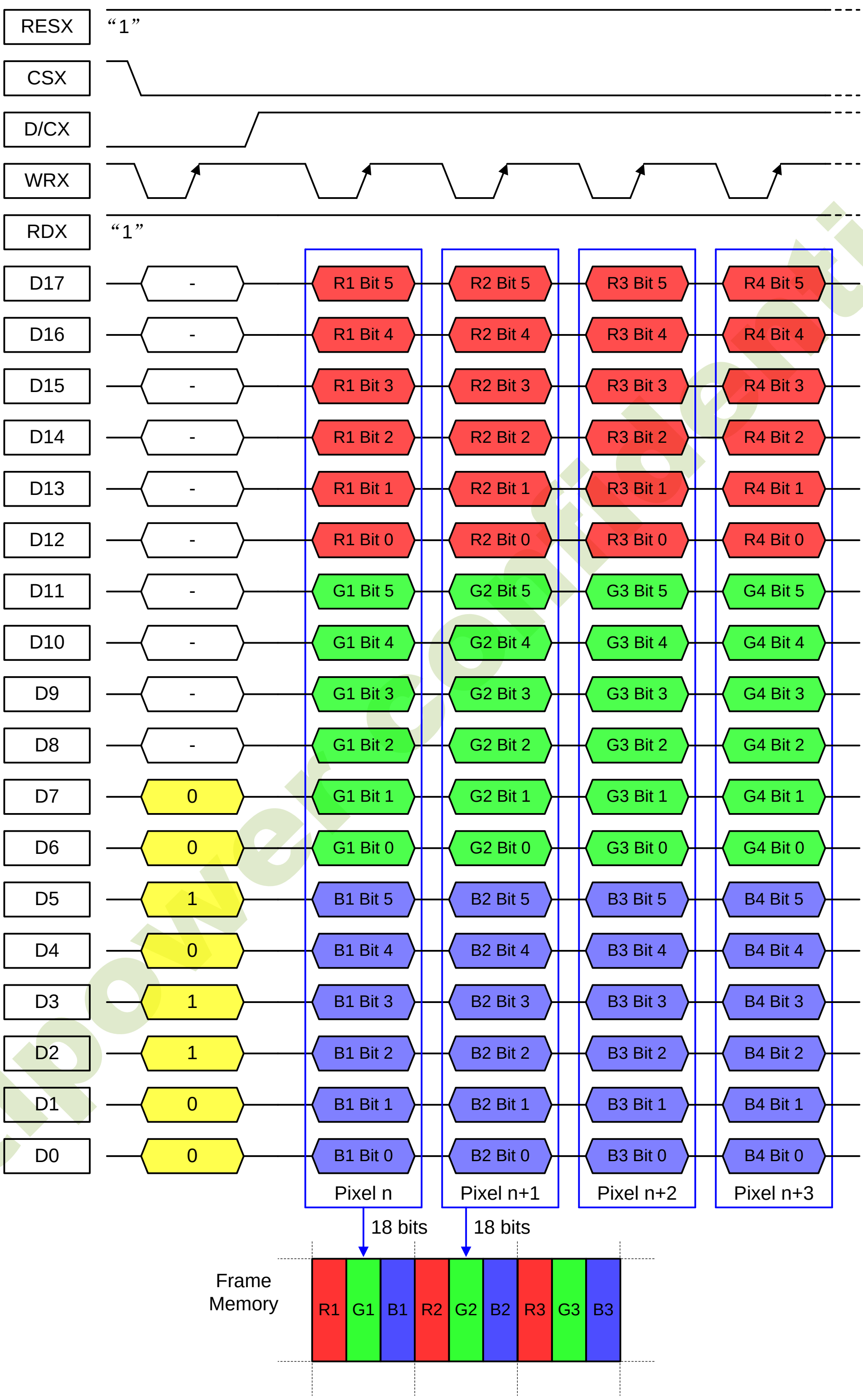
7.2.9.10.2. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah=”05h”)



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

7.2.9.10.3. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h”)



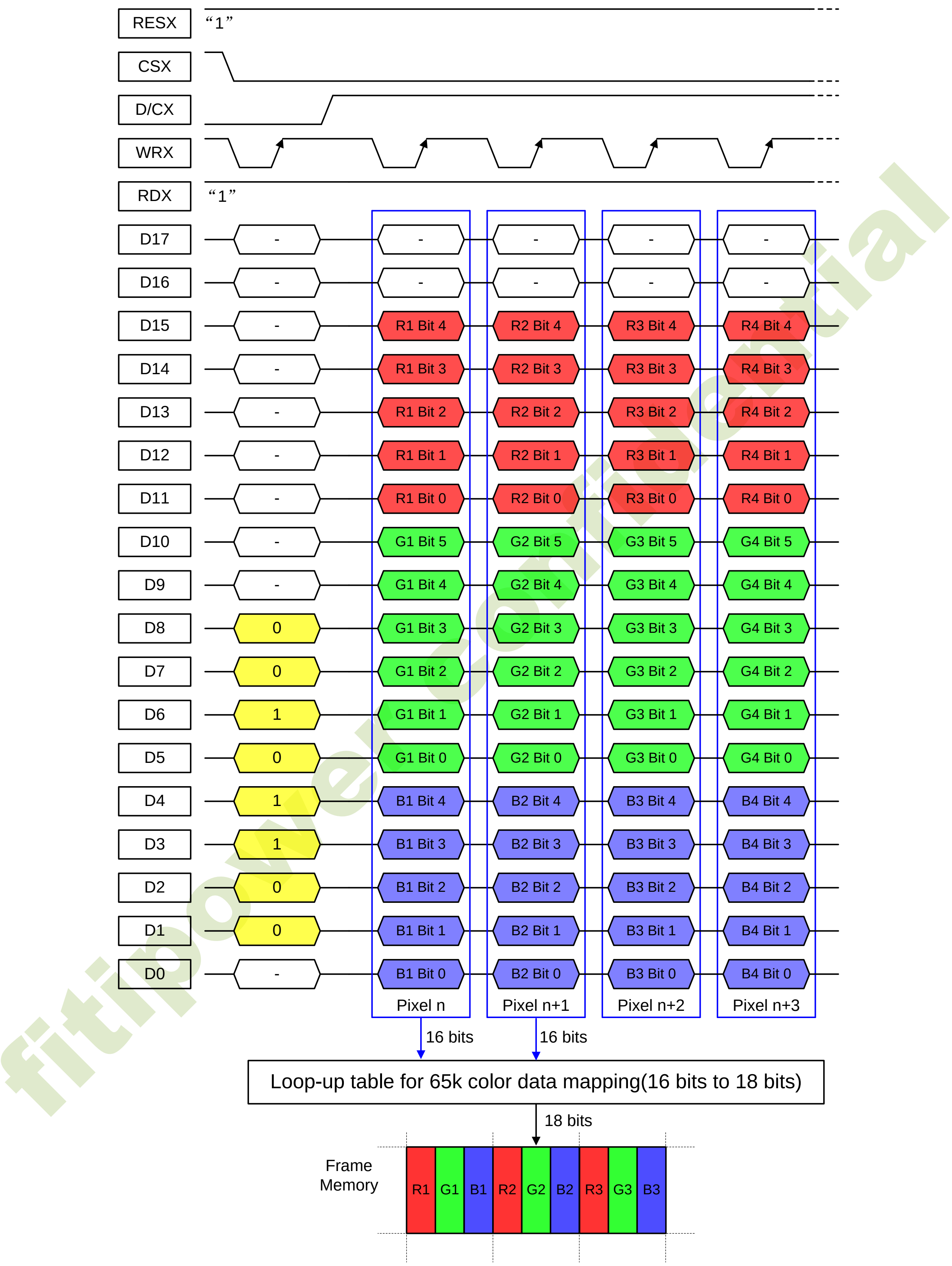
Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

7.2.9.11. 8080-Ⅱ series 18-Bit Parallel Interface

The 8080-Ⅱ series 18-bit parallel interface of JD9852 can be used by setting IM[3:0]=”1010b”.
Different display data formats are available for two colors depth supported by listed below.
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

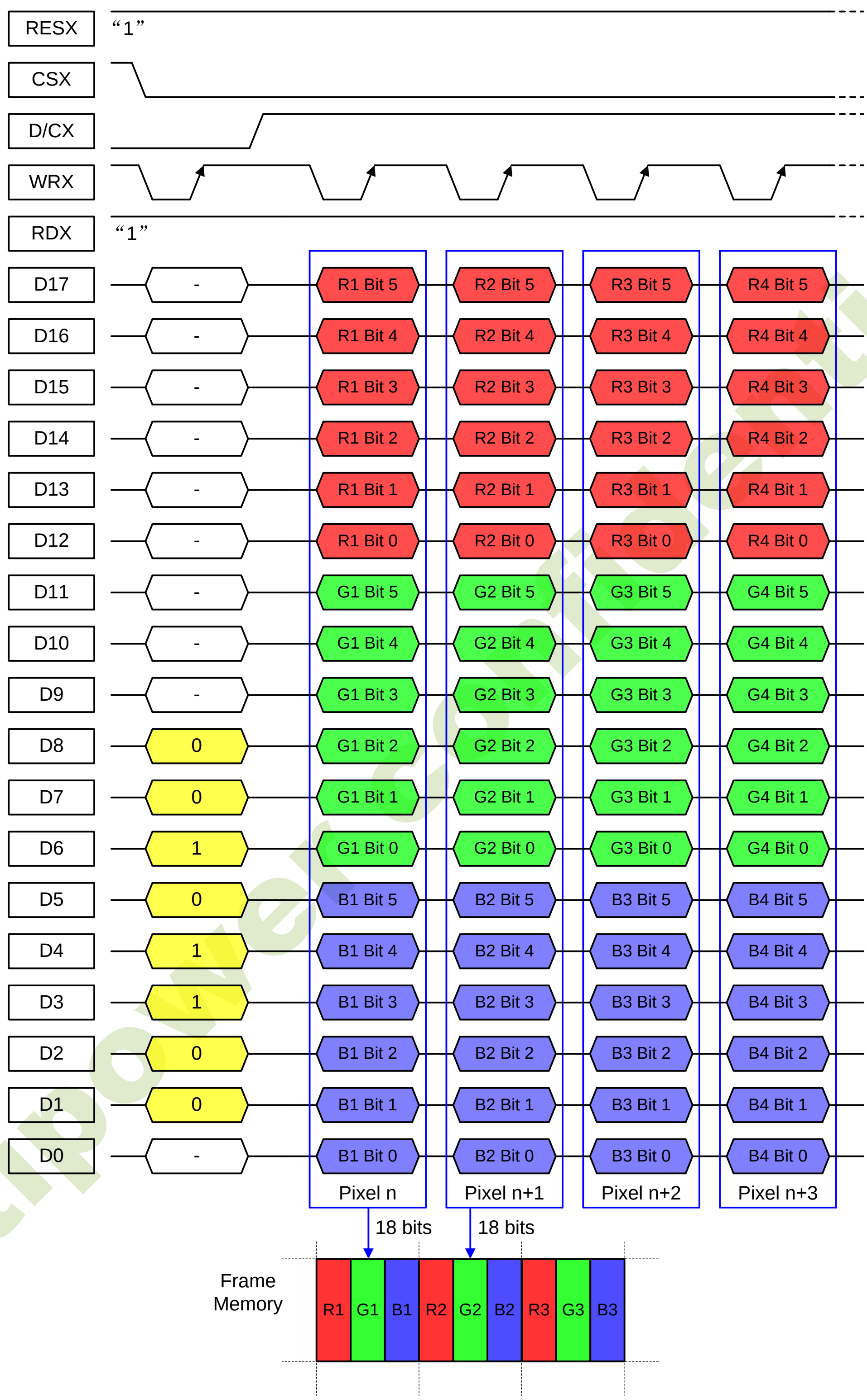
7.2.9.11.1. R 5-bit, G 6-bit, B 5-bit, 65,536 colors (3Ah=”05h”)



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

7.2.9.11.2. R 6-bit, G 6-bit, B 6-bit, 262,144 colors(3Ah=”06h”)



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

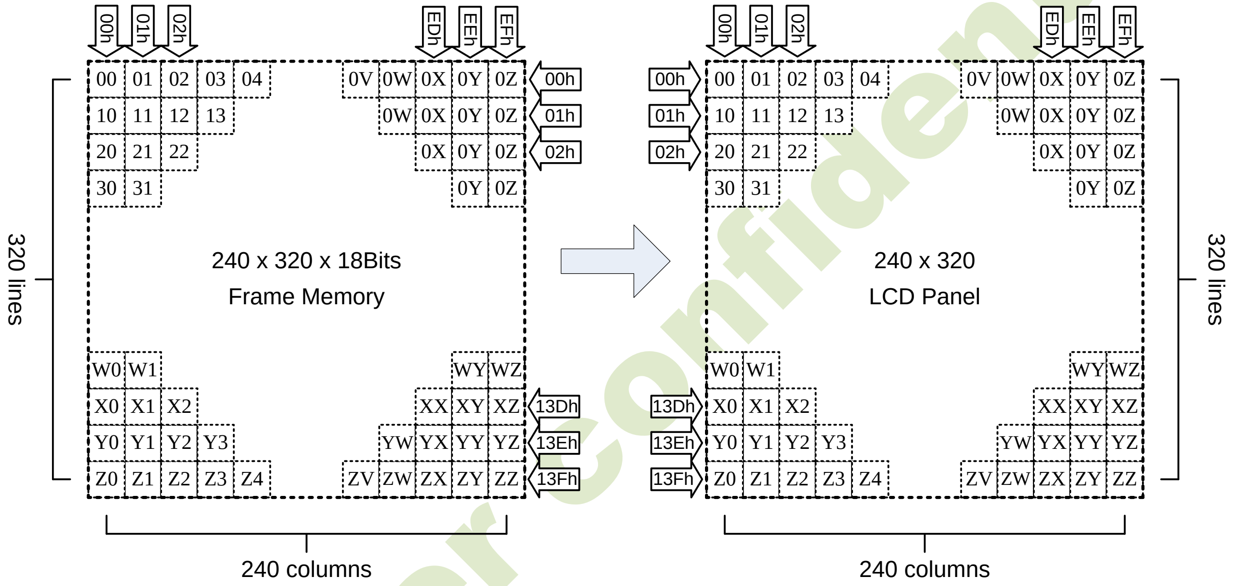
8. Function Description

8.1. Memory to Display Address Mapping

8.1.1. Normal Display On or Partial Mode On, Vertical Scroll Off

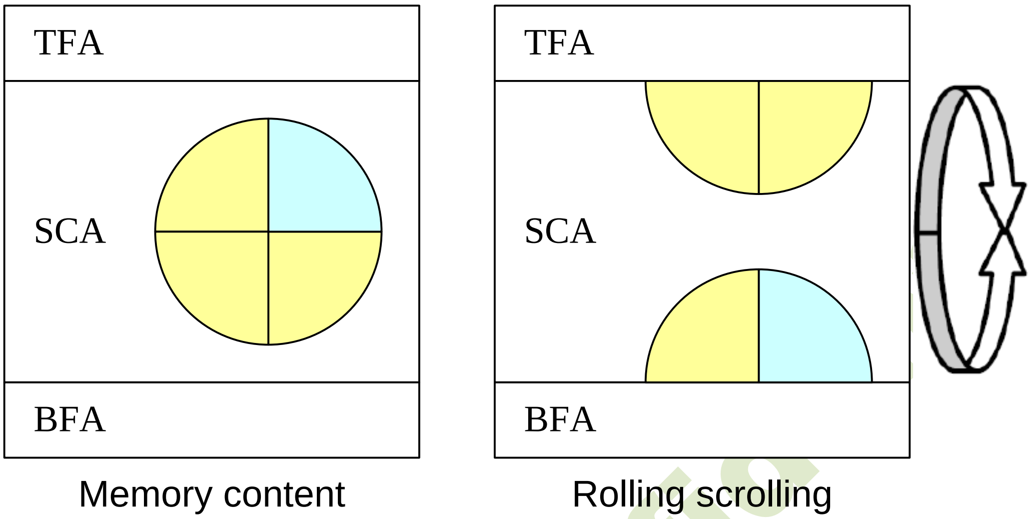
In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0).



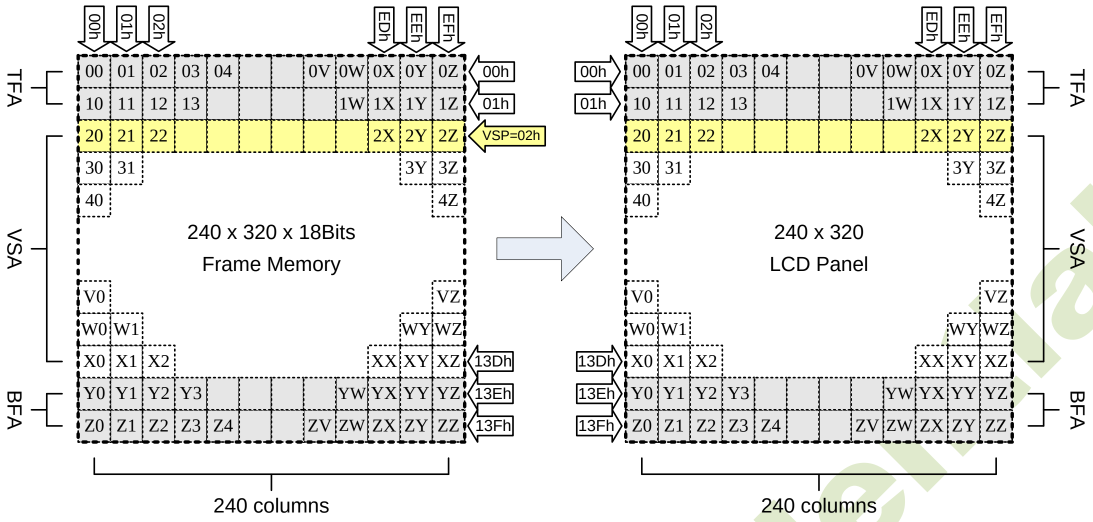
8.1.2.Vertical Scroll mode

There are one type of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

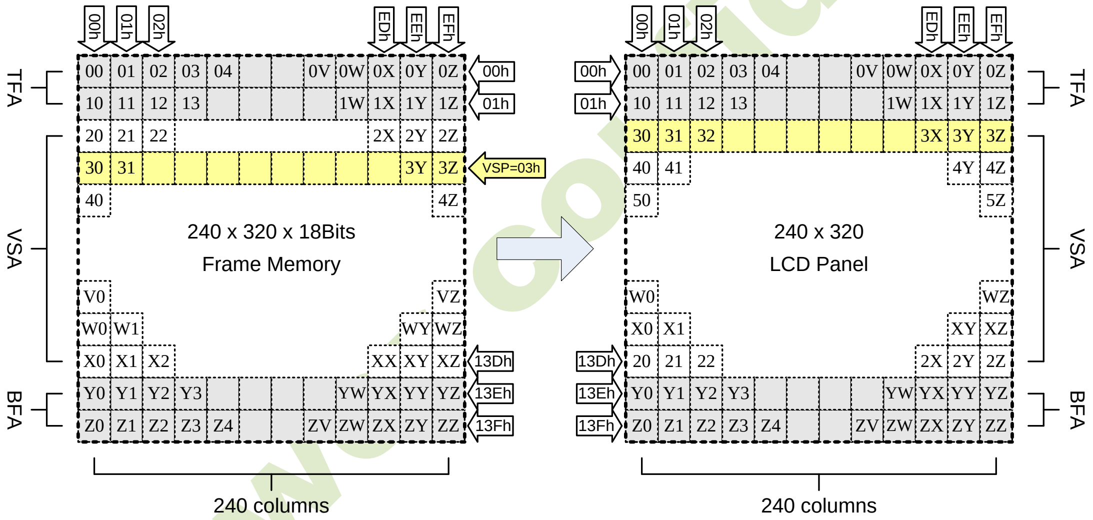


When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=320. In this case, 'rolling' scrolling is applied as shown below.

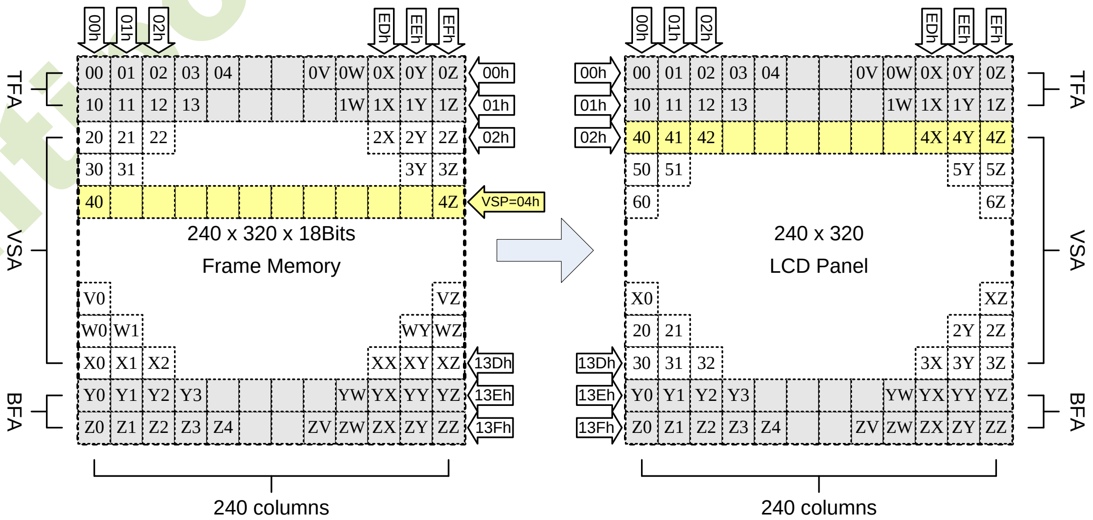
Example 1: TFA=2, VSA=316, BFA=2, VSP=2 when MADCTL Bit B4(ML)=0



Example 2: TFA=2, VSA=316, BFA=2, VSP=3 when MADCTL Bit B4(ML)=0



Example 3: TFA=2, VSA=316, BFA=2, VSP=3 when MADCTL Bit B4(ML)=0



Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)≠320, Scrolling Mode is undefined.

8.1.3. Vertical Scroll exaple

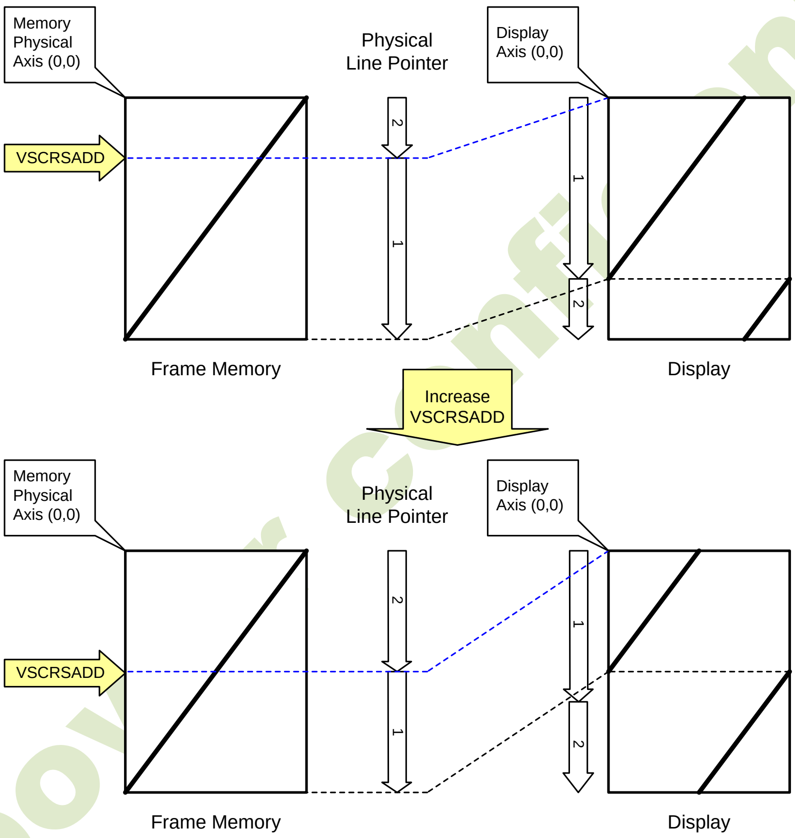
8.1.3.1. Case1: TFA+VSA+BFA≠320

N/A. Do not set TFA+VSA+BFA≠320, unless unexpected picture will be shown.

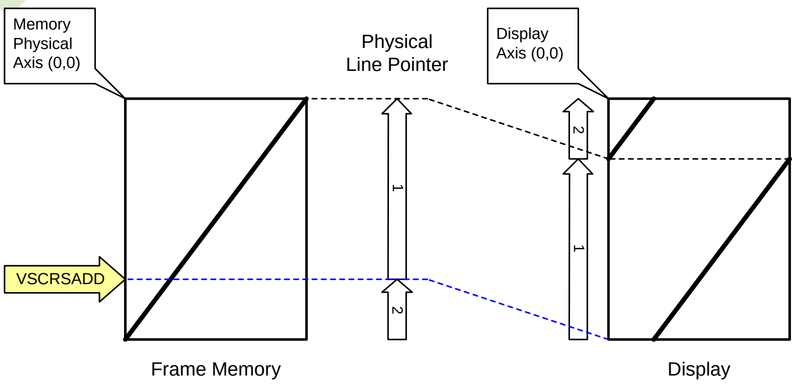
8.1.3.2. Case2: TFA+VSA+BFA = 320

Example 1. When TFA=0, VSA=320, BFA=0 and VSCRSADD=80.

MADCTL B4(ML) = "0"

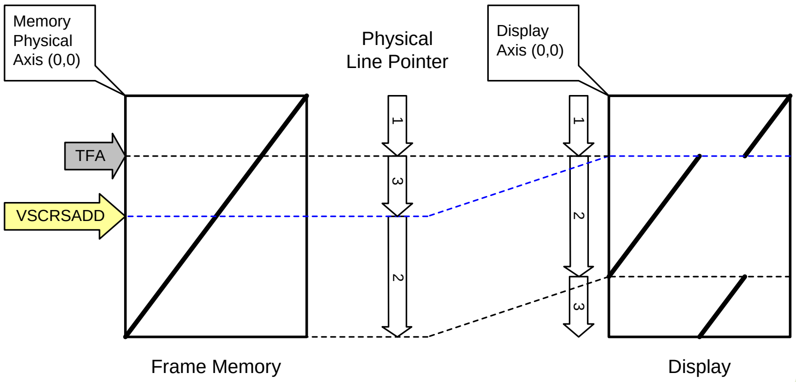


MADCTL B4(ML) = "1"

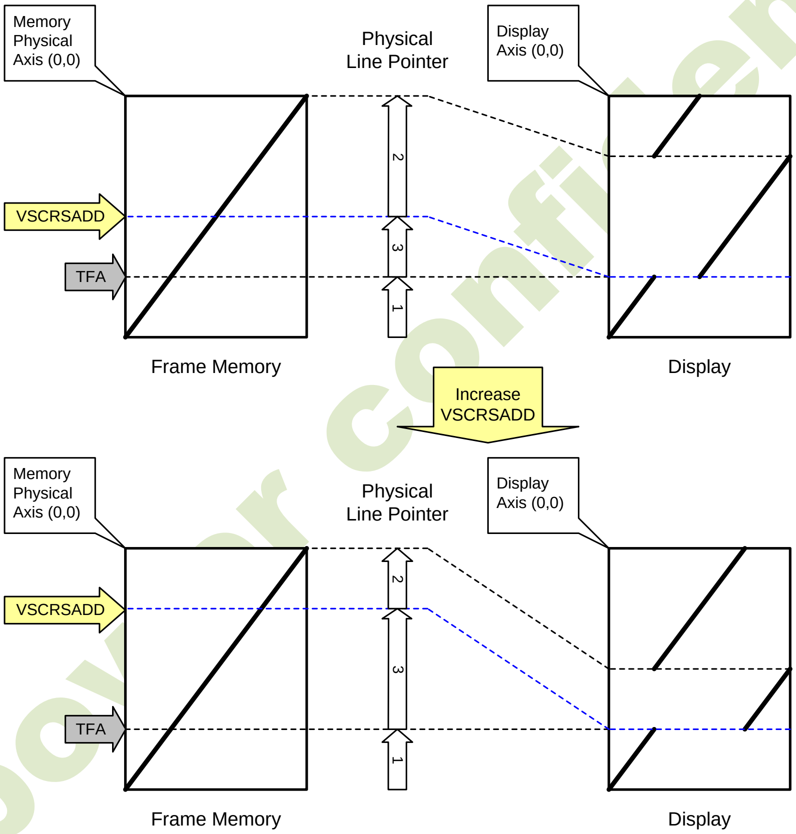


Example 2. When TFA=80, VSA=240, BFA=0 and VSCRSADD=160.

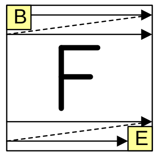
MADCTL B4(ML) = "0"



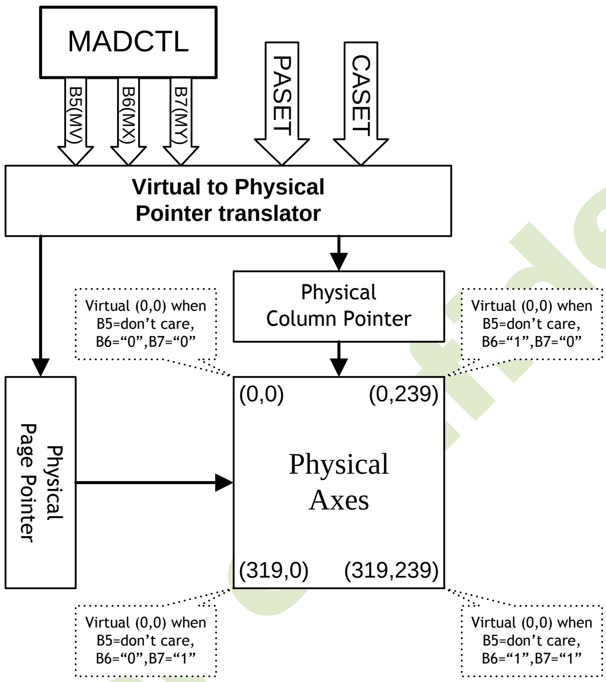
MADCTL B4(ML) = "1"



8.2. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command(36h), Bits B5, B6, B7(MV, MX, MY) as described below.

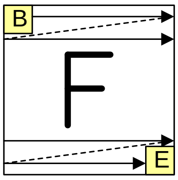
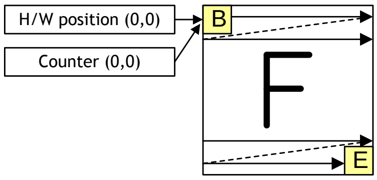
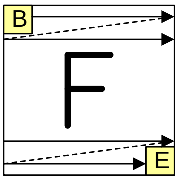
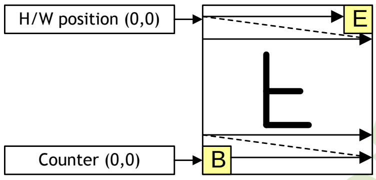
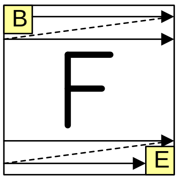
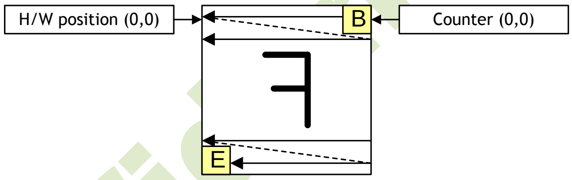
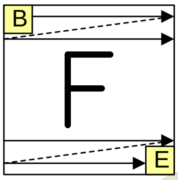
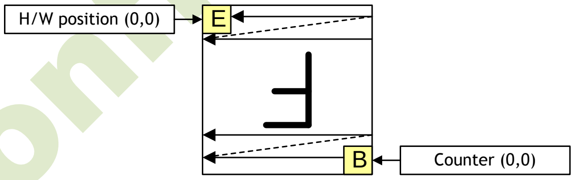
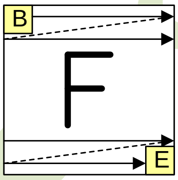
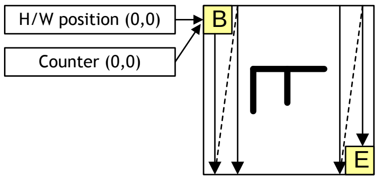
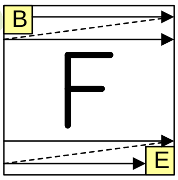
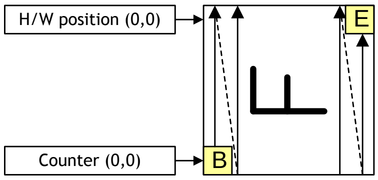
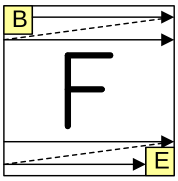
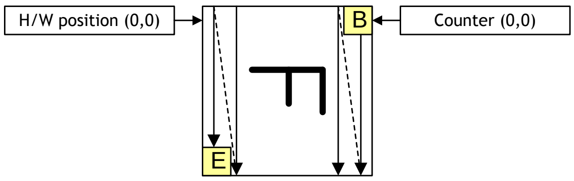
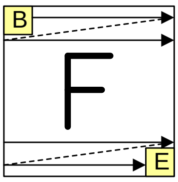
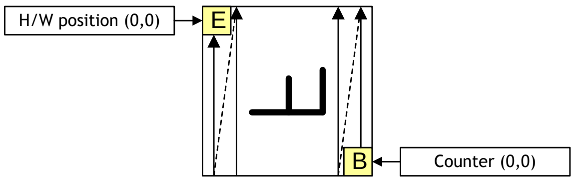


B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted.	Return to "Start Column"	Return to "Start Page"
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than "End column."	Return to "Start Column"	Increment by 1
The Column counter value is larger than "End column" and the Page counter value is larger than "End page".	Return to "Start Column"	Return to "Start Page"

The resultant image for each setting is illustrated below:

Display Data Direction	MADCTL			Image in the Host	Image in Frame Memory
	MV	MX	MY		
Normal	0	0	0		
Y-Invert	0	0	1		
X-Invert	0	1	0		
X-Invert Y-Invert	0	1	1		
X-Y exchange	1	0	0		
X-Y exchange Y-Invert	1	0	1		
X-Y exchange X-Invert	1	1	0		
X-Y exchange X-Invert Y-Invert	1	1	1		

8.3. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

8.3.1. Tearing effect line modes

Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:

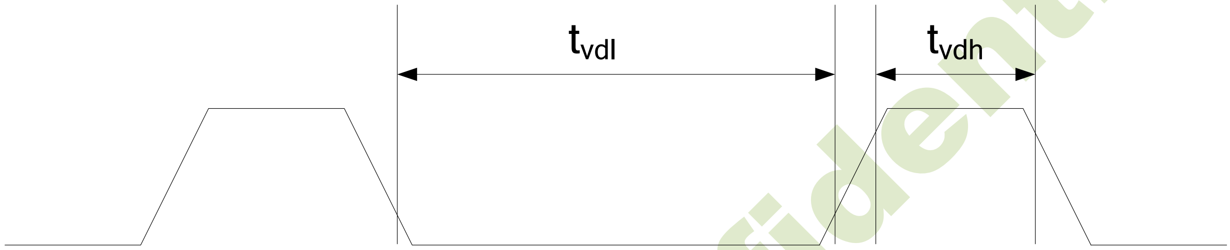


Figure. 8.1 Tearing Effect Line mode 1

tvdh= The LCD display is not updated from the Frame Memory

tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-sync and H-sync Information, there is one V-sync and N H-sync pulses per field.

N: If the resolution is 240 RGB X 320, the N=320.

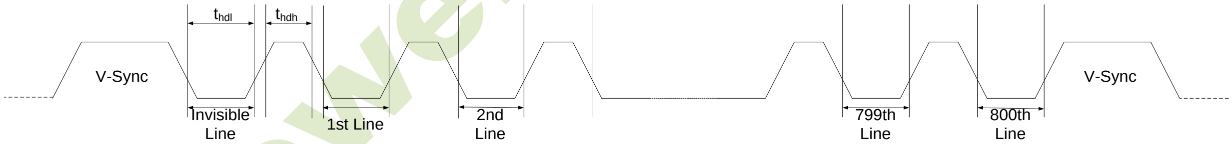


Figure. 8.2 Tearing Effect Line mode 2

thdh= The LCD display is not updated from the Frame Memory

thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

8.3.2. Tearing effect line timing

The Tearing Effect signal is described below.

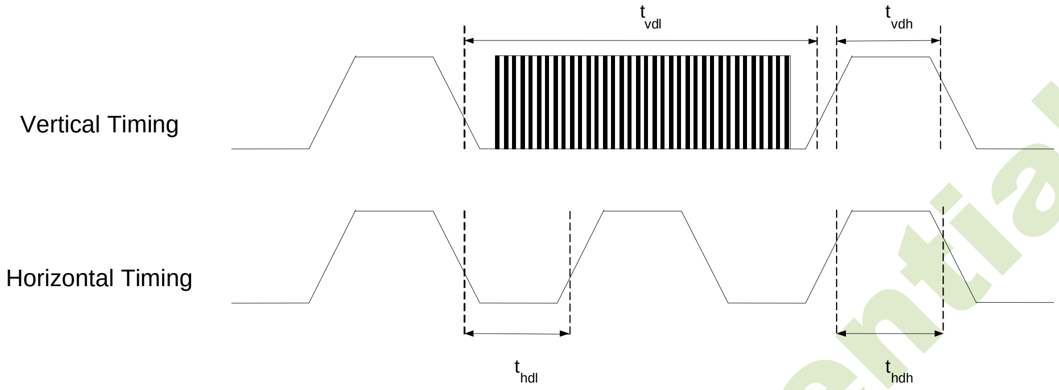


Figure. 8.3 Tearing Effect Line timing

Idle Mode Off/On (Frame Rate = 60 Hz)

Symbol	Parameter	Min.	Max.	Unit
tvdl	Vertical Timing Low Duration	TBD	-	ms
tvdh	Vertical Timing High Duration	1000	-	us
thdl	Horizontal Timing Low Duration	TBD	-	us
thdh	Horizontal Timing High Duration	TBD	500	us
tr	Rise time	-	15	ns
tf	Fall time	-	15	Ns

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

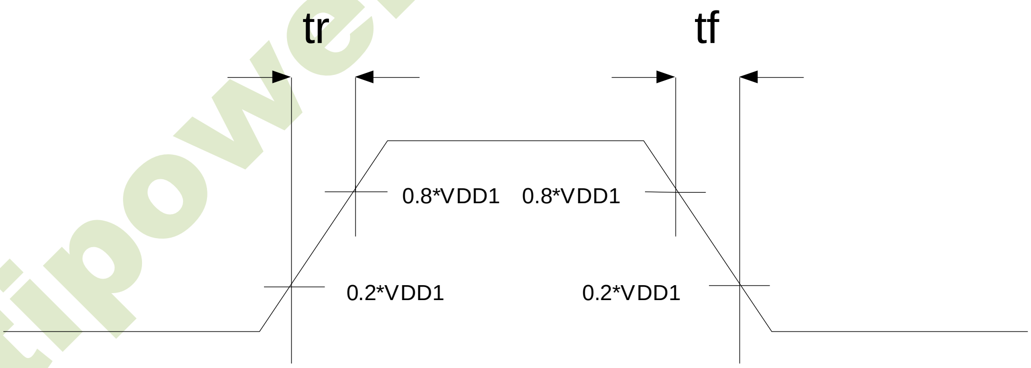


Figure. 8.4 Tearing Effect Line definition of tf, tr

8.4. Gamma Structure Description

8.4.1. Adjustable gamma

The JD9852 includes gamma adjustment function for the 262k colors display (128 grayscale for R-/G-/B-color). Gamma adjustment operation is implemented by 19 gamma adjustment control registers to meet the characteristic of LCD panel. Then total 128 grayscale levels are generated in Positive-/Negative-grayscale voltage. These registers are available for both polarities.

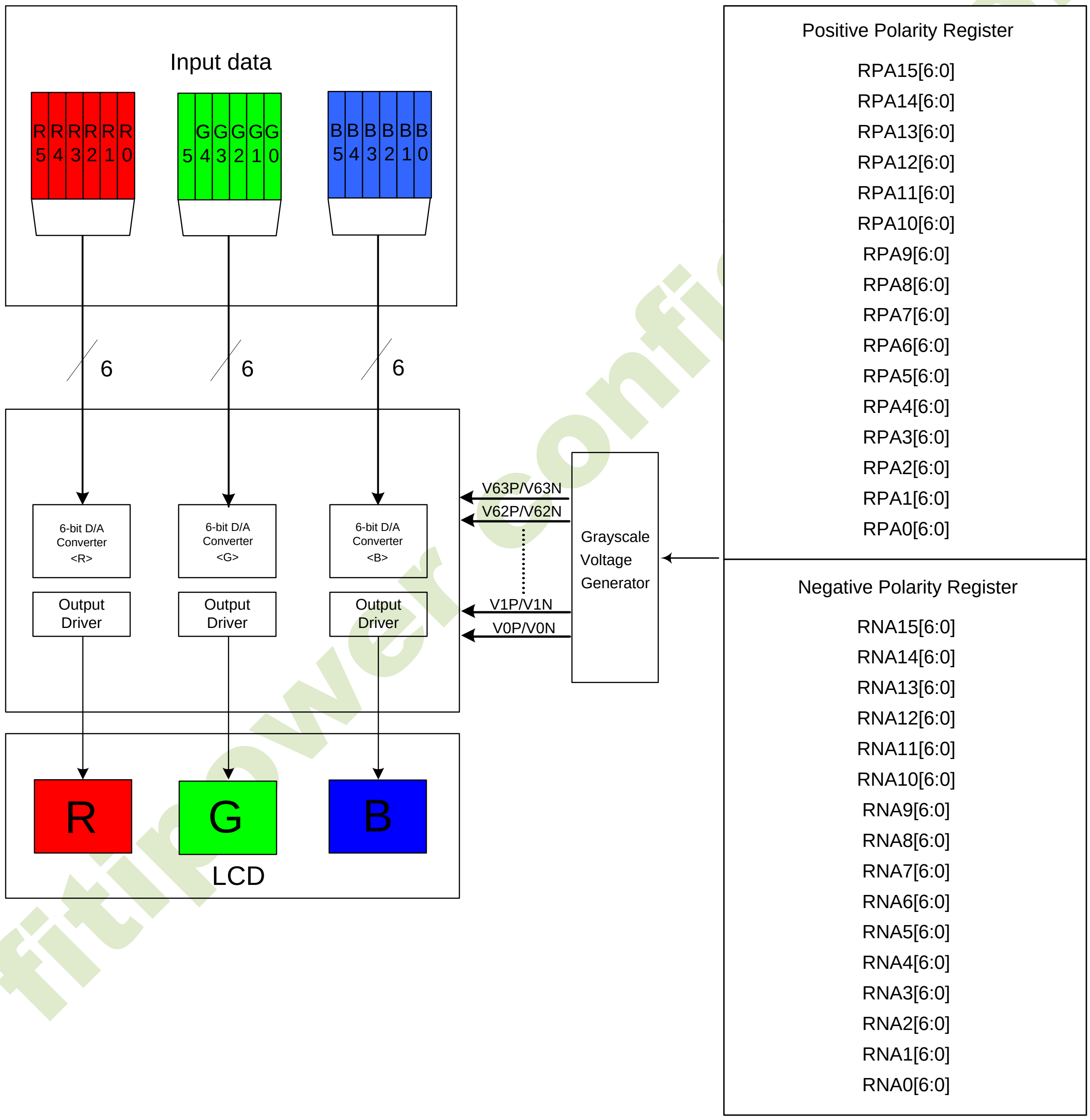


Figure. 8.5 Grayscale control

8.4.2. Grayscale-Level adjustment control

The JD9852 has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel. These registers are belong amplitude adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

Amplitude adjustment registers

The amplitude adjustment variable registers are used to adjust the amplitude of the grayscale voltage. his function is implemented by controlling the 63-to-1 selectors (RPA/RNA0~15), each one of whole has 6 bits and generates one reference voltage output (VO(P/N)0, 1, 2, 4, 6, 13, 20, 27, 36, 43, 50, 57, 59, 61, 62, 63). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
	RPA15 5-0	RNA15 5-0	Variable resistor(RPA/RNA15) for VO(P/N)63
	RPA14 5-0	RNA14 5-0	Variable resistor(RPA/RNA14) for VO(P/N)62
	RPA13 5-0	RNA13 5-0	Variable resistor(RPA/RNA13) for VO(P/N)61
	RPA12 5-0	RNA12 5-0	Variable resistor(RPA/RNA12) for VO(P/N)59
	RPA11 5-0	RNA11 5-0	Variable resistor(RPA/RNA11) for VO(P/N)57
	RPA10 5-0	RNA10 5-0	Variable resistor(RPA/RNA10) for VO(P/N)50
	RPA9 5-0	RNA9 5-0	Variable resistor(RPA/RNA9) for VO(P/N)43
	RPA8 5-0	RNA8 5-0	Variable resistor(RPA/RNA8) for VO(P/N)36
	RPA7 5-0	RNA7 5-0	Variable resistor(RPA/RNA7) for VO(P/N)27
	RPA6 5-0	RNA6 5-0	Variable resistor(RPA/RNA6) for VO(P/N)20
	RPA5 5-0	RNA5 5-0	Variable resistor(RPA/RNA5) for VO(P/N)13
	RPA4 5-0	RNA4 5-0	Variable resistor(RPA/RNA4) for VO(P/N)6
	RPA3 5-0	RNA3 5-0	Variable resistor(RPA/RNA3) for VO(P/N)4
	RPA2 5-0	RNA2 5-0	Variable resistor(RPA/RNA2) for VO(P/N)2
	RPA1 5-0	RNA1 5-0	Variable resistor(RPA/RNA1) for VO(P/N)1
	RPA0 5-0	RNA0 5-0	Variable resistor(RPA/RNA0) for VO(P/N)0

Table 8.1 Gamma-Adjustment registers

Gamma resistor stream and 63 to 1 selector

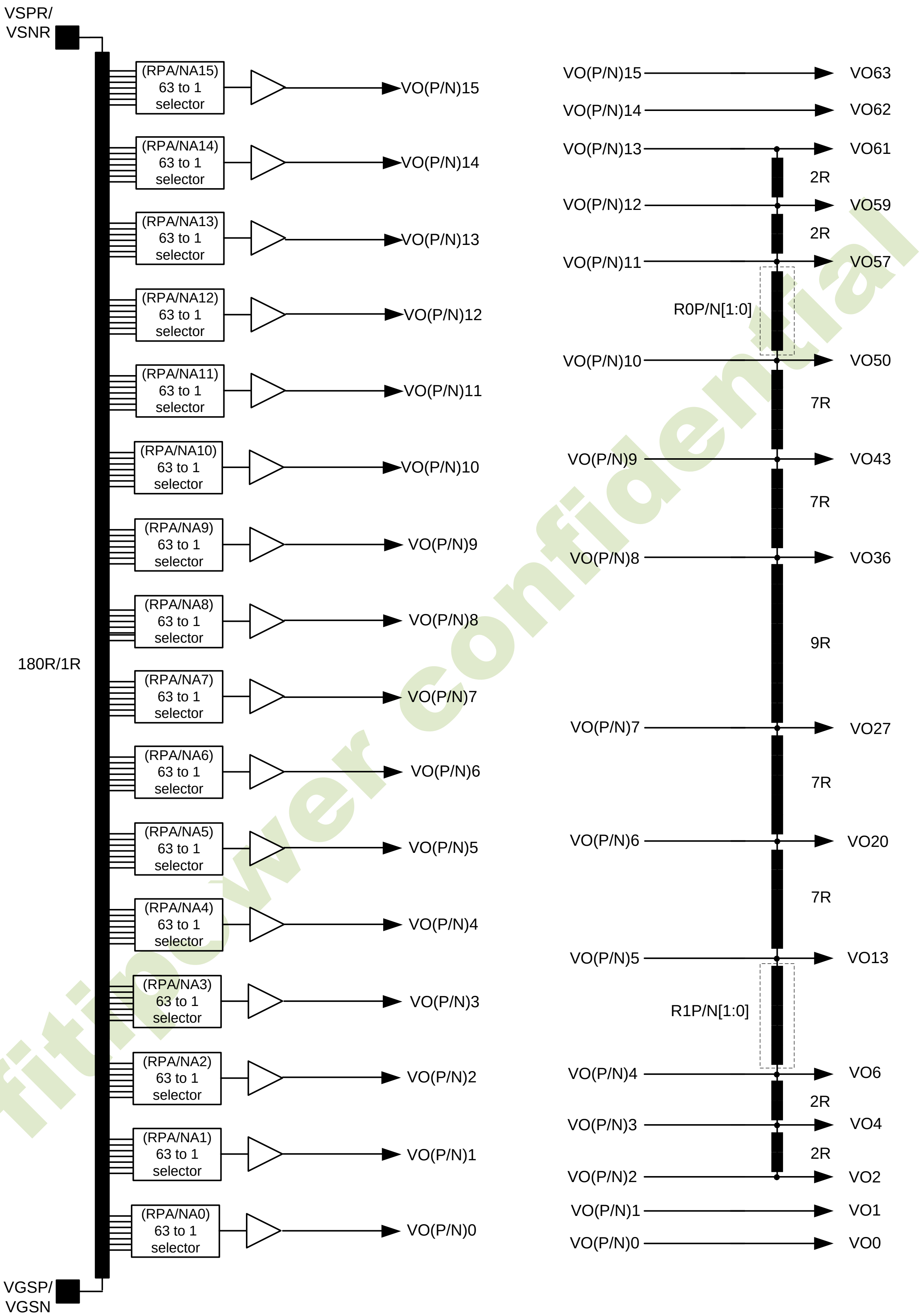


Figure. 8.6 Gamma resister stream and gamma reference voltage

8.4.3.Variable resister ratio & Voltage levels

The resistances are decided by setting values in the Amplitude adjustment register.
The relationships are the same for RPA/RNA 0 ~15, shown below.

Value in Register RPA/RNA 0~15 (5-0)	Resistance RPA/RNA 0~15
000000	0R
000001	1R
000010	2R
000011	3R
:	:
100000	32R
100001	33R
100010	34R
100011	35R
:	:
111100	60R
111101	61R
111110	62R
111111	63R

VOP voltage levels are determined by the following formulas:

Reference voltage	Register	Amplitude adjustment value	Formula
VOP13~15	RPA13~15[5:0]	000000	((180R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((180R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((180R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((180R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((180R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((180R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((180R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((180R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((180R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP12	RPA12[5:0]	000000	((172R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((172R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((172R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((172R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((172R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((172R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((172R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((172R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((172R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP11	RPA11[5:0]	000000	((162R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((162R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((162R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((162R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((162R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((162R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((162R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((162R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((162R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP10	RPA10[5:0]	000000	((140R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((140R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((140R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((140R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((140R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((140R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((140R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((140R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((140R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP9	RPA9[5:0]	000000	((132R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((132R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((132R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((132R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((132R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((132R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((132R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((132R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((132R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP8	RPA8[5:0]	000000	((122R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((122R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((122R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((122R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((122R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((122R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((122R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((122R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((122R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP7	RPA7[5:0]	000000	((112R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((112R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((112R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((112R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((112R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((112R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((112R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((112R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((112R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP6	RPA6[5:0]	000000	((104R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((104R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((104R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((104R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((104R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((104R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((104R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((104R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((104R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP5	RPA5[5:0]	000000	((96R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((96R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((96R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((96R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((96R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((96R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((96R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((96R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((96R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP4	RPA4[5:0]	000000	((90R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((90R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((90R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((90R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((90R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((90R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((90R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((90R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((90R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP3	RPA3[5:0]	000000	((86R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((86R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((86R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((86R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((86R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((86R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((86R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((86R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((86R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP2	RPA2[5:0]	000000	((80R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((80R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((80R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((80R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((80R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((80R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((80R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((80R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((80R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP1	RPA1[5:0]	000000	((76R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((76R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((76R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((76R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((76R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((76R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((76R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((76R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((76R -1R) / 180R) * (VGMP - VGSP) + VGSP

Reference voltage	Register	Amplitude adjustment value	Formula
VOP0	RPA0[5:0]	000000	((64R-64R) / 180R) * (VGMP - VGSP) + VGSP
		000001	((64R -63R) / 180R) * (VGMP - VGSP) + VGSP
		000010	((64R -62R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		100000	((64R -32R) / 180R) * (VGMP - VGSP) + VGSP
		100001	((64R -31R) / 180R) * (VGMP - VGSP) + VGSP
		100010	((64R -30R) / 180R) * (VGMP - VGSP) + VGSP
		:	:
		111101	((64R -3R) / 180R) * (VGMP - VGSP) + VGSP
		111110	((64R -2R) / 180R) * (VGMP - VGSP) + VGSP
		111111	((64R -1R) / 180R) * (VGMP - VGSP) + VGSP

VON voltage levels are determined by the following formulas:

Reference voltage	Register	Amplitude adjustment value	Formula
VON13~15	RNA13~15[5:0]	000000	((180R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((180R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((180R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((180R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((180R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((180R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((180R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((180R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((180R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON12	RNA12[5:0]	000000	((172R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((172R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((172R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((172R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((172R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((172R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((172R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((172R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((172R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON11	RNA11[5:0]	000000	((162R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((162R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((162R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((162R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((162R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((162R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((162R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((162R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((162R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON10	RNA10[5:0]	000000	((140R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((140R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((140R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((140R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((140R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((140R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((140R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((140R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((140R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON9	RNA9[5:0]	000000	((132R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((132R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((132R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((132R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((132R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((132R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((132R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((132R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((132R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON8	RNA8[5:0]	000000	((122R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((122R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((122R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((122R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((122R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((122R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((122R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((122R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((122R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON7	RNA7[5:0]	000000	((112R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((112R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((112R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((112R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((112R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((112R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((112R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((112R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((112R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON6	RNA6[5:0]	000000	((104R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((104R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((104R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((104R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((104R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((104R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((104R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((104R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((104R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON5	RNA5[5:0]	000000	((96R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((96R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((96R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((96R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((96R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((96R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((96R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((96R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((96R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON4	RNA4[5:0]	000000	((90R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((90R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((90R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((90R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((90R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((90R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((90R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((90R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((90R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON3	RNA3[5:0]	000000	((86R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((86R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((86R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((86R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((86R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((86R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((86R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((86R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((86R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON2	RNA2[5:0]	000000	((80R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((80R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((80R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((80R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((80R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((80R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((80R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((80R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((80R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON1	RNA1[5:0]	000000	((76R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((76R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((76R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((76R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((76R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((76R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((76R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((76R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((76R -1R) / 180R) * (VGMN - VGSN) + VGSN

Reference voltage	Register	Amplitude adjustment value	Formula
VON0	RNA0[5:0]	000000	((64R-64R) / 180R) * (VGMN - VGSN) + VGSN
		000001	((64R -63R) / 180R) * (VGMN - VGSN) + VGSN
		000010	((64R -62R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		100000	((64R -32R) / 180R) * (VGMN - VGSN) + VGSN
		100001	((64R -31R) / 180R) * (VGMN - VGSN) + VGSN
		100010	((64R -30R) / 180R) * (VGMN - VGSN) + VGSN
		:	:
		111101	((64R -3R) / 180R) * (VGMN - VGSN) + VGSN
		111110	((64R -2R) / 180R) * (VGMN - VGSN) + VGSN
		111111	((64R -1R) / 180R) * (VGMN - VGSN) + VGSN

8.5. Power Level Definition

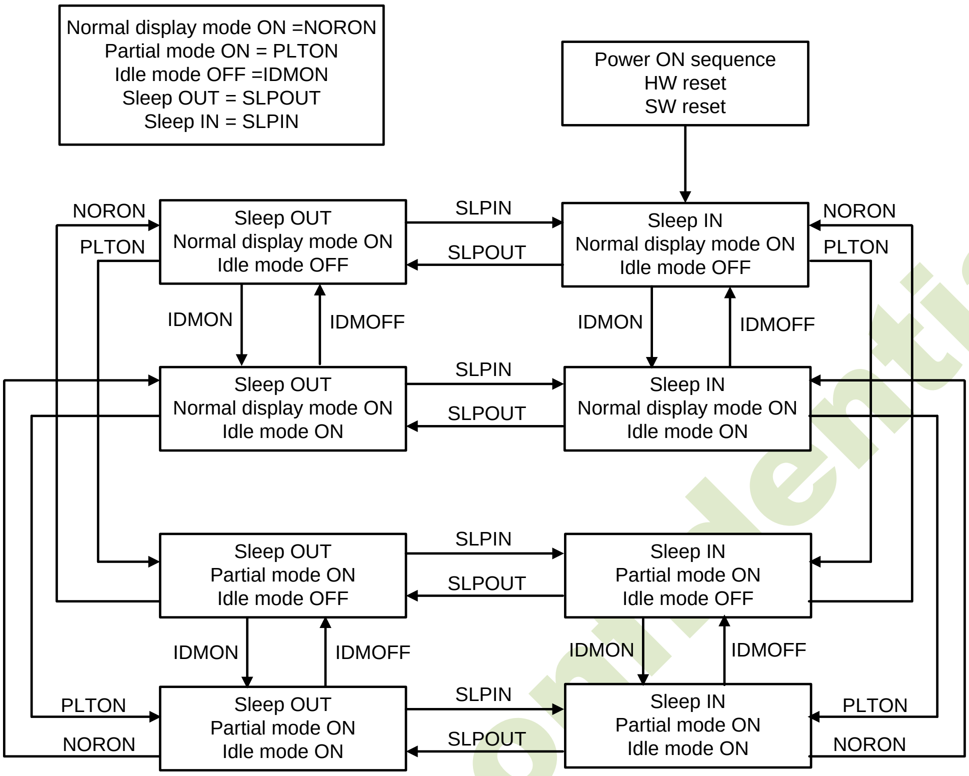
8.5.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

8.5.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

8.6. Power on/off sequence

8.6.1. General

IOVCC must be setup ready before analog power setup.
IOVCC must be power down after analog power down.

During power off, if the display module is in the SLPOUT mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if the display module is in the SLPIN mode, VCI and IOVCC can be powered down minimum 0msec after RESX has been released.

There will be no damage to the display module if the power sequences are not met.
There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

There will be no abnormal visible effects on the display panel between end of Power On Sequence and before receiving SLPOUT command. Also, between receiving SLPOUT command and Power Off Sequence.

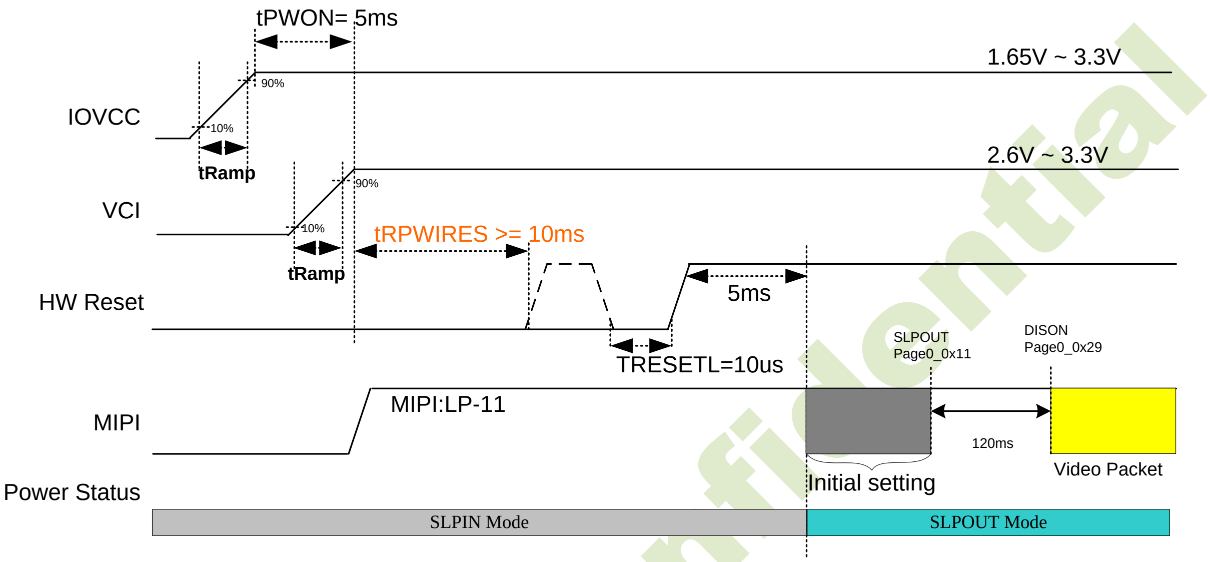
If RESX line is not held stable by host during Power On Sequence as defined in Sections 8.6.1, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

There is not a limit for Rise/Fall time on VCI, VCIP and IOVCC.

8.6.2. Power on/off sequence

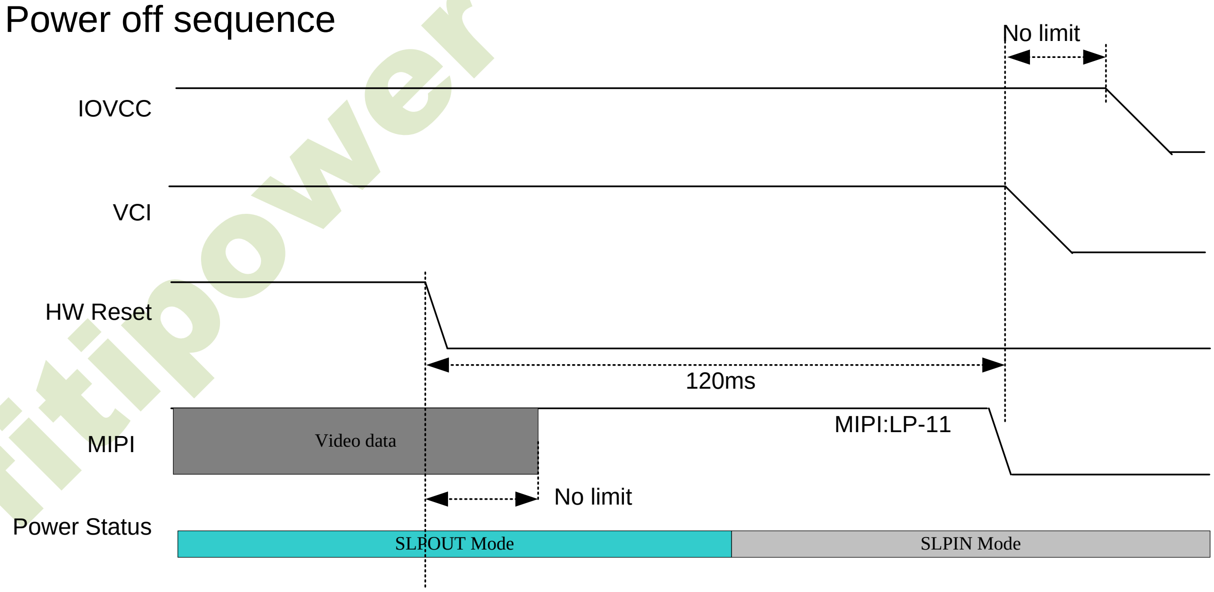
Internal DC/DC power mode IOVCC =1.65V ~ 3.3V, VCI=VCIP=2.6V ~ 3.3V.

Power on sequence



	Min	Typ	Max
Power up tRamp for VCI/IOVCC	0.2mS		20mS

Power off sequence



8.7. Content adaptive brightness control (CABC) function

8.7.1.Definition of the CABC

A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image.

This function and its four different modes can be controlled. See chapter "10.2.39 Write Content Adaptive Brightness Control (55h)" (bits: C1 and C0) for more information.
Definition of These Four Modes and Target Power Reduction Ration:

1. Off mode: Content Adaptive Brightness Control functionality is totally off.

2. UI [User interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less

3. Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%

4. Moving image mode: Optimized for moving image e.g. Video clip. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30% Limits of image degradation are needed to agree with Nokia and module supplier. Nokia provides test images to the module supplier.

Notes:
1. Partial area updating of the image data is supported by the CABC function.
2. Power consumption of the CABC processing is minimized.

8.7.2. Transition Time of the CABC

Content Adaptive Brightness Control (CABC) is a dimming function where two different dimming functions are implemented in the ABC system:

- Image content based dimming function
- Manual Setting based dimming function
-

Both functions have to combine without any abnormal visible effect, e.g. flicker problem.
The transition time for dimming function is illustrated below.

- Image content based dimming function

Display brightness is changed, according to the image contents. The following graph mentions the case of displaying three different images.

- Image A: -20% brightness reduction
- Image B: -30% brightness reduction
- Image C: -10% brightness reduction

Transition time from the previous image to the current displayed image is “Transition time A”. “Transition time A” is not specified in this specification because it is depending on CABC algorithm, which is defined by the display module supplier.

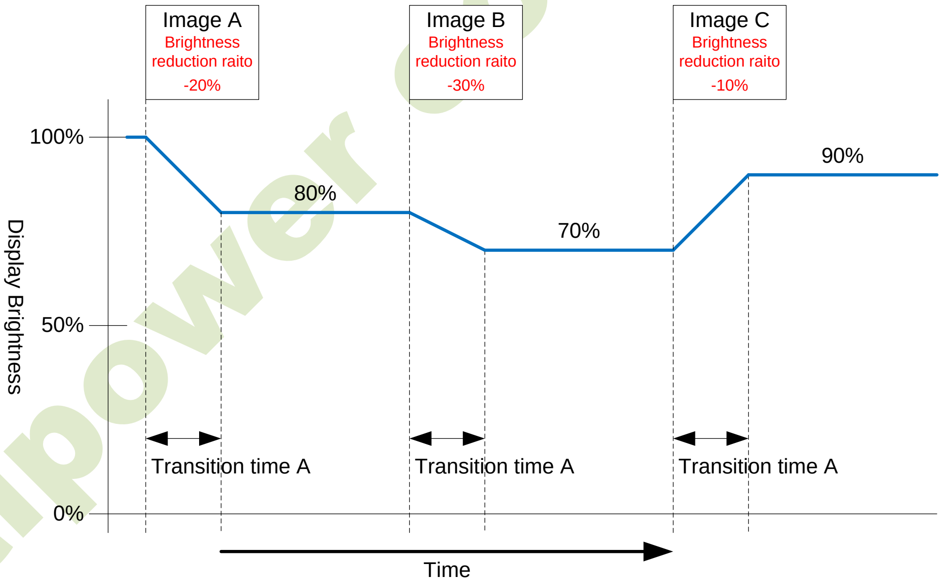


Figure. 8.7 Transition Time on Content Adaptive Brightness Control

- Manual Setting based dimming function

Transition time from the previous display brightness to the current display brightness is "Transition time B".

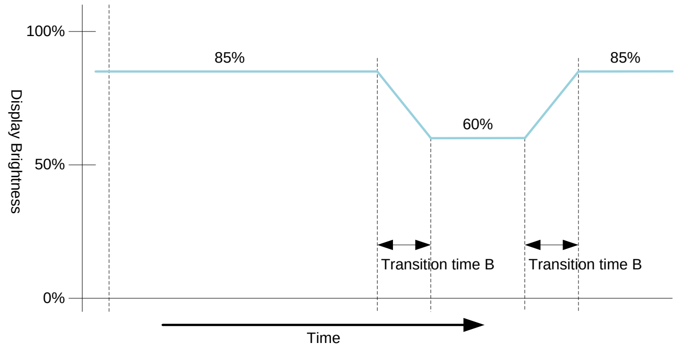


Figure. 8.8 Transition Time on Manual Setting

- Combined display brightness

Green line in the following graph is for the output brightness of display. It is combined with both display brightness, which are defined in the above graphs.

Maximum transition time is transition time A + B.

The brightness level of the display is calculated with the following formula.
Display Output Brightness = Manual Setting * CABC Brightness Ratio.

Case	Brightness	Brightness ratio	Display Output brightness
Case 1	85%	80%	68%
Case 2	60%	70%	42%
Case 3	85%	90%	76.5%

Table 8.2 Display Output Brightness Calculations

Notes:
1. "Transition Time A" is based on CABC algorithm.
2. "Transition Time B" is controlled by bit DD of "11.2.45 Write CTRL Display (53h)" command.
3. The worst case transition time (A+B) is from a current to target brightness

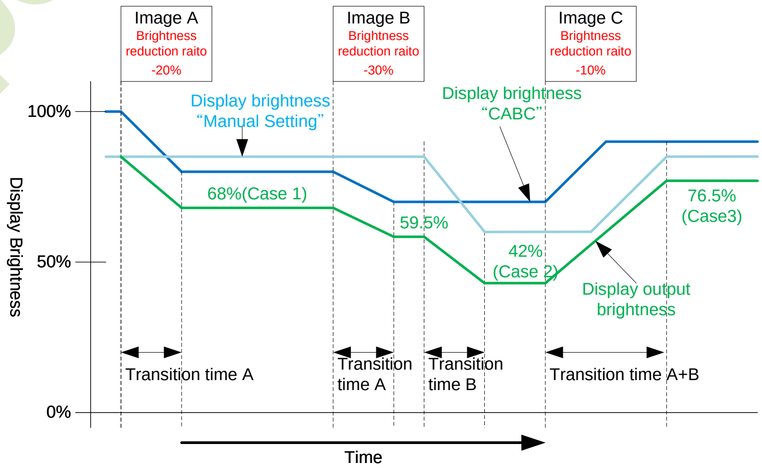


Figure. 8.9 Transition Time on Combined Display Brightness

8.7.3.Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting is to avoid too much brightness reduction. When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. If CABC algorithm works without any abnormal visual effect, image processing function can operate even when the brightness cannot be changed.

When display brightness is turned off (BCTRL=0 of “10.2.37 Write CTRL Display (53h)”), CABC minimum brightness setting is ignored. “10.2.42 Read CABC Minimum Brightness (5Fh)” always read the setting value of “10.2.41 Write CABC Minimum Brightness (5Eh)”.

Example:
CABC minimum brightness value = 51d (33h: 20% display brightness)

Case	A	B	C	Real Display Output Brightness
	Brightness (Manual Setting)	Brightness Ratio (CABC)	Calculation Result: Display Output Brightness Value	
Case 1	50%	70%	35%	35%
Case 2	20%	70%	14%	20%
Case 3	50%	70%	35%	35%

Table 8.3 Minimum Brightness Setting of the CABC Function - Example

9. Command

9.1. Command List

9.1.1. Standard command

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	00h	No Operation
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	01h	
RDDIDIF	0	↑	1	-	0	0	0	0	0	1	0	0	04h	Read display ID
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	ID1[7:0]									ID1 read
	1	1	↑	-	ID2[7:0]									ID2 read
	1	1	↑	-	ID3[7:0]									ID3 read
RDRED	0	↑	1	-									06h	Read Red Color
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	R[7:0]									
RDGREEN	0	↑	1	-									07h	Read Green Color
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	G[7:0]									
RDBLUE	0	↑	1	-									08h	Read Blue Color
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	B[7:0]									
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	09h	Read Display Status
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D[31:24]									
	1	1	↑	-	D[23:16]									
	1	1	↑	-	D[15:8]									
	1	1	↑	-	D[7:0]									
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	0Ah	Read display power mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0		
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	0Bh	Read display MADCTL
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0		

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	0Ch	Read display pixel format
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0		
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	0Dh	Read display image mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0		
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	0Eh	Read display signal mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0		
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	0Fh	Read display self-diagnostic result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D7	D6	D5	D4	0	0	0	0		
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	10h	Sleep In
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	11h	Sleep Out
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	12h	Partial Mode On
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	13h	Normal display mode on
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	20h	Display inversion off
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	21h	Display inversion on
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	26h	Gamma set
	1	↑	1	-	GC[7:0]									
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	28h	Display off
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	29h	Display on
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	2Ah	Column Address Set
	1	↑	1	-	SC[15:8]									Column address start
	1	↑	1	-	SC[7:0]									
	1	↑	1	-	EC[15:0]									Column address end
	1	↑	1	-	EC[7:0]									
PASET	0	↑	1	-	0	0	1	0	1	0	1	1	2Bh	Page address set
	1	↑	1	-	SP[15:0]									Page address start
	1	↑	1	-	SP[7:0]									
	1	↑	1	-	EP[15:0]									Page address end
	1	↑	1	-	EP[7:0]									
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	2Ch	Memory Write
	1	↑	1	D1[17:8]	D1[7:0]									Write data
	1	↑	1	Dx[17:8]	Dx[7:0]									
	1	↑	1	Dn[17:8]	Dn[7:0]									
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	2Eh	Memory read
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	D1[17:8]	D1[7:0]									
	1	1	↑	Dx[17:8]	Dx[7:0]									
	1	1	↑	Dn[17:8]	Dn[7:0]									

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PLTAR	0	↑	1	-	0	0	1	1	0	0	0	0	30h	Partial Area
	1	↑	1	-	SR[15:0]									Start row
	1	↑	1	-	SR[7:0]									
	1	↑	1	-	ER[15:0]									End row
	1	↑	1	-	ER[7:0]									
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	33h	Vertical scrolling definition
	1	↑	1	-	TFA[15:8]									Top Fixed Area
	1	↑	1	-	TFA[7:0]									
	1	↑	1	-	VSA[15:8]									Vertical Scrolling Area
	1	↑	1	-	VSA[7:0]									
	1	↑	1	-	BFA[15:8]									Bottom Fixed Area
	1	↑	1	-	BFA[7:0]									
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	34h	Tearing Effect Line OFF
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	35h	Tearing Effect Line ON
	1	↑	1	-	-	-	-	-	-	-	-	M		
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	36h	Memory Access Control
	1	↑	1	-	MY	MX	MV	ML	RGB	0	0	0		
VSCRSADD	0	↑	1	-	0	0	1	1	0	1	1	1	37h	Vertical scrolling start address
	1	↑	1	-	VSP[15:8]									
	1	↑	1	-	VSP[7:0]									
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	38h	Idle mode off
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	39h	Idle mode on
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	3Ah	Interface Pixel Format,
	1	↑	1	-	-	D6	D5	D4	-	D2	D1	D0		
RAMWRCON	0	↑	1		0	0	1	1	1	1	0	0	3Ch	Memory write contiune
	1	↑	1	D1[17:8]	D1[7:0]									Write data
	1	↑	1	Dx[17:8]	Dx[7:0]									
	1	↑	1	Dn[17:8]	Dn[7:0]									
RAMRDCON	0	↑	1	-	0	0	1	1	1	1	1	0	3Eh	Memory read contiune
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	D1[17:8]	D1[7:0]									Read Data
	1	1	↑	Dx[17:8]	Dx[7:0]									
	1	1	↑	Dn[17:8]	Dn[7:0]									
TESL	0	↑	1	-	0	1	0	0	0	1	0	0	44h	Set Tear Effect Scan Lines
	1	↑	1	-	TELINE[15:8]									
	1	↑	1	-	TELINE[7:0]									
GETSCAN	0	↑	1	-	0	1	0	0	0	1	0	1	45h	Return the current scan line
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	SLN[15:8]									
	1	1	↑	-	SLN[15:8]									

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	51h	Write Display Brightness
	1	↑	1	-	DBV[7:0]									
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	52h	Read Display Brightness Value
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	DBV[7:0]									
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	53h	Write CTRL Display
	1	↑	1	-	-	-	BCTRL	-	DD	BL	-	-		
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	54h	Read Control Display value
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0		
WRCABC	0	↑	1	-	0	1	0	1	0	1	0	1	55h	Write Adaptive Brightness Control
	1	↑	1	-	-	-	-	-	-	-	CABC[1:0]			
RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	56h	Read Adaptive Brightness Control
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	0	0	0	0	0	0	CABC[1:0]			
WRCABCMB	0	↑	1	-	0	1	0	1	1	1	1	0	5Eh	Write CABC minimum brightness
	1	↑	1	-	CMB[7:0]									
RDCABCMB	0	↑	1	-	0	1	0	1	1	1	1	1	5Fh	Read CABC minimum brightness
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	CMB[7:0]									
RDABCSDR	0	↑	1	-	0	1	1	0	1	0	0	0	68h	Read ABC Self-Diagnostic Result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	D[7:6]									
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	DAh	Read ID1
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	module's manufacturer[7:0]									
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	DBh	Read ID2
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	LCD module/driver version [7:0]									
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	DCh	Read ID3
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	LCD module/driver ID[7:0]									

9.1.2. User command

TBD.

9.2. Command Description

9.2.1. NOP (00h)

<table>
<tr><th>CMD/Pas</th><th>D/CX</th><th>WRX</th><th>RDX</th><th>D17-8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command does not have any effect on the display module.
The NOP command may be used to terminate a Frame Memory Read or Frame Memory Write.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>N/A</td></tr>
<tr><td>SW Reset</td><td>N/A</td></tr>
<tr><td>HW Reset</td><td>N/A</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>

9.2.2. SWRESET: Software Reset (01h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	0	0	1	01

Parameter	No Parameter
Description	The display module performs a software reset. Registers are written with their SW Reset default values. The Frame Memory contents are unaffected by this command
Restriction	The host processor must wait 5 milliseconds before sending any new commands to a display module following this command. The display module updates the registers during this time. If a SWRESET is sent when the display module is in SLPIN Mode, the host processor must wait 120 milliseconds before sending an SLPOUT command. SWRESET should not be sent when the display module is not in SLPIN mode

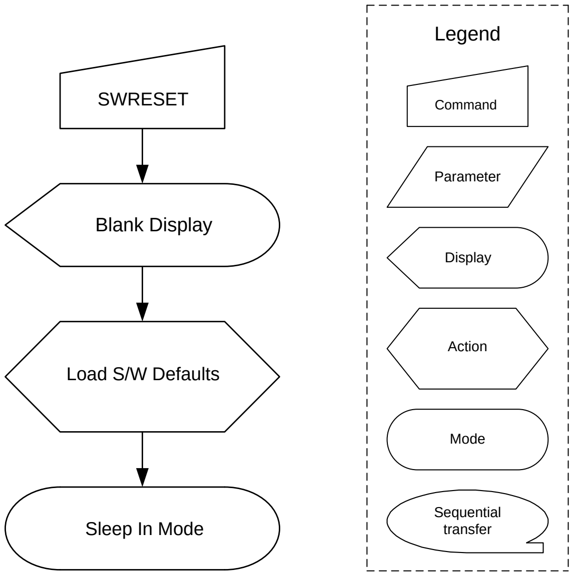
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart



9.2.3. RDDIDIF: Read display identification information (04h)

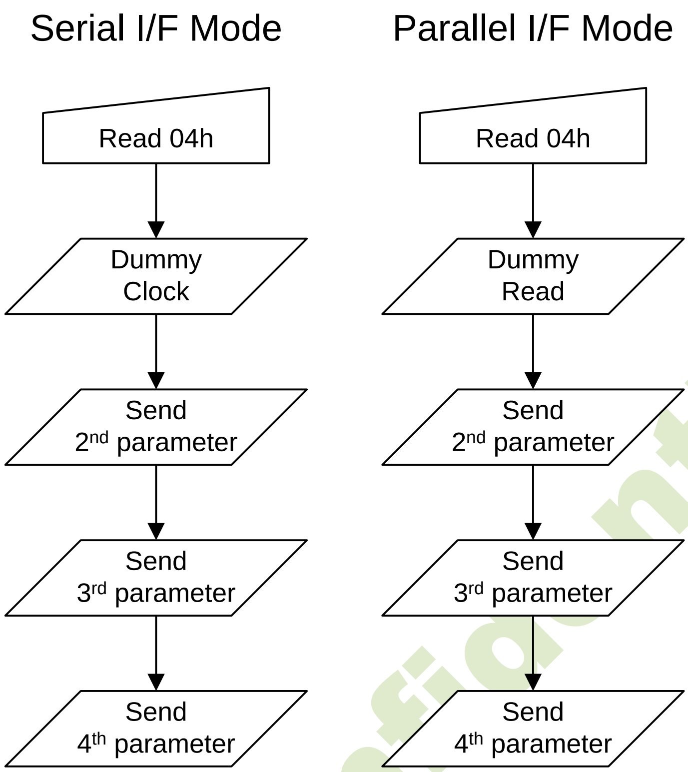
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	1	0	0	04
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	ID1[7:0]								
3rd Parameter	1	1	↑	-	ID2[7:0]								
4th Parameter	1	1	↑	-	ID3[7:0]								
Description	This read byte returns 24-bit display identification information. The 1st Parameter is dummy read. The 2nd parameter: LCD module's manufacturer ID. The 3rd parameter: LCD module/driver version ID The 4th parameter: LCD module/driver ID.												
Restriction	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

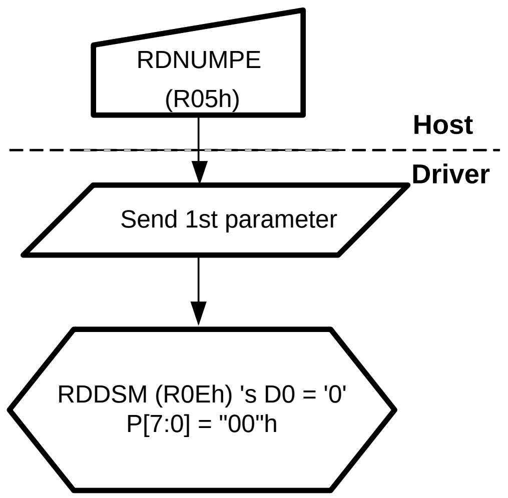
Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	98h	51h	01h
SW Reset	98h	51h	01h
HW Reset	98h	51h	01h

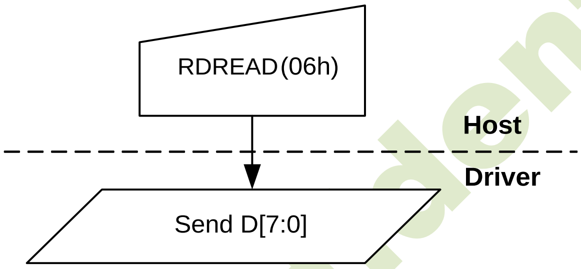
Flow Chart	

Serial I/F Mode
Parallel I/F Mode
Read 04h
Dummy Clock
Send 2nd parameter
Send 3rd parameter
Send 4th parameter
Read 04h
Dummy Read
Send 2nd parameter
Send 3rd parameter
Send 4th parameter

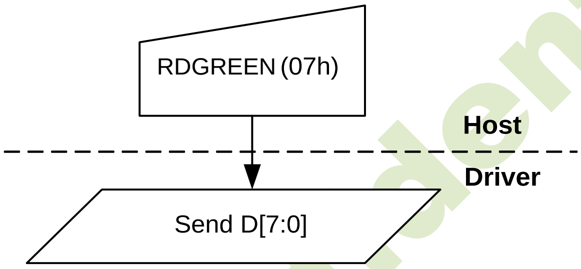
9.2.4. RDNUMPE: Read number of the parity errors (05h)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>05</td></tr>
<tr><td>Parameter 1</td><td>R</td><td>P7</td><td>P6</td><td>P5</td><td>P4</td><td>P3</td><td>P2</td><td>P1</td><td>P0</td><td></td></tr>
<tr><td>Description</td><td colspan="10">The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below.
P[6:0] bits are telling a number of the errors.
P[7] is set to ‘1’ if there is overflow with P[6..0] bits.
P[7:0] bits are set to ‘0’s (as well as RDDSM(0Eh)’s D0 is set ‘0’ at the same time) after there is sent the second parameter information (=The read function is completed).</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="10">DSI I/F Mode

</td></tr>
</table>

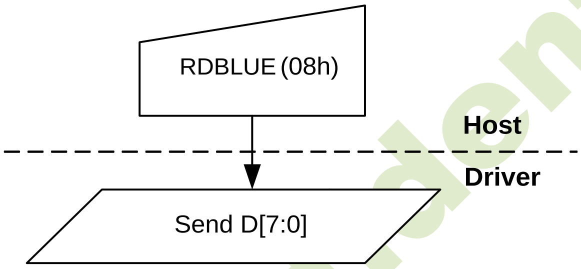
9.2.5. REDRD: Read Red Color (06h)

CMD/PAs	R/W	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	-	0	0	0	0	0	1	1	0	06
Parameter 1	**R**	-	R7	R6	R5	R4	R3	R2	R1	R0	
Description	The first parameter is telling red color value of the first pixel of the frame when there is used DPI I/F. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to ‘0’. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to ‘0’.										
Restriction	-										
Flow Chart											

9.2.6. REDGREEN: Read Green Color (07h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	0	1	1	1	07
Parameter 1	**R**	G7	G6	G5	G4	G3	G2	G1	G0	
Description	The first parameter is telling green color value of the first pixel of the frame when there is used DPI I/F. 16 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to ‘0’. 18 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to ‘0’.									
Restriction	-									
Flow Chart										

9.2.7. REDBLUE: Read Blue Color (08h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	1	0	0	0	08
Parameter 1	**R**	B7	B6	B5	B4	B3	B2	B1	B0	
Description	The first parameter is telling blue color value of the first pixel of the frame when there is used DPI I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to ‘0’. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to ‘0’.									
Restriction	-									
Flow Chart										

9.2.8. RDDST: Read Display Status (09h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	0	1	09
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	D[31:24]								
3rd Parameter	1	1	↑	-	D[23:16]								
4th Parameter	1	1	↑	-	D[15:8]								
5th Parameter	1	1	↑	-	D[7:0]								

Description

This command indicates the current status of the display as described in the table below

Bit	Description	Value
D31	Booster Voltage Status	'0' = Booster Off. '1' = Booster On.
D30	Page Address Order	'0' = Top to Bottom (MADCTL B7='0'). '1' = Bottom to Top (MADCTL B7='1').
D29	Column Address Order	'0' = Left to Right (MADCTL B6='0'). '1' = Right to Left (MADCTL B6='1')
D28	Page/Column Order	'0' = Normal Mode (When MADCTL B5='0'). '1' = Reverse Mode (When MADCTL B5='1').T
D27	Vertical Order	'0' = LCD Refresh Top to Bottom (When MADCTL B4='0'). '1' = LCD Refresh Bottom to Top (When MADCTL B4='1').
D26	RGB/BGR Order	'0' = RGB (MADCTL B3='0'). '1' = BGR (MADCTL B3='1').
D25	Horizontal Order	'0' = LCD Refresh Left to Right (When MADCTL B2='0'). '1' = LCD Refresh Right to Left (When MADCTL B2='1').
D24	For Future Use	This bit is not applicable for this project, set it to '0'
D23	For Future Use	This bit is not applicable for this project, set it to '0'
D22 D21 D20	Interface Color Pixel Format Definition	See interface format table below
D19	Idle Mode On/Off	'0' = Idle Mode Off. '1' = Idle Mode On.
D18	Partial Mode On/Off	'0' = Partial Mode Off, '1' = Partial Mode On.
D17	Sleep In/Out	'0' = Sleep In Mode. '1' = Sleep Out Mode.
D16	Display Normal Mode On/Off	'0' = Partial or Scrolling Mode. '1' = Normal Mode.
D15	Vertical Scrolling Status	'0' = Vertical Scrolling is Off. '1' = Vertical Scrolling is On.
D14	Horizontal Scrolling Status	This bit is not applicable for this project, set it to '0'
D13	Inversion Status	'0' = Inversion is Off. '1' = Inversion is On.
D12	All Pixels On	'0' = Normal mode. '1' = All Pixels On.

Interface Format	D22	D21	D20
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 Bit/Pixel	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	1	1	1

D11	All Pixels Off	'0' = Normal mode. '1' = All Pixels Off.
D10	Display On/Off	'0' = Display is Off. '1' = Display is On.
D9	Tearing Effect Line On/Off	'0' =Tearing Effect Line Off. '1' = Tearing Effect On.
D8	Gamma Curve Selection	(see Gamma Curve table below)
D7	Gamma Curve Selection	(see Gamma Curve table below)
D6	Gamma Curve Selection	(see Gamma Curve table below)
D5	Tearing Effect Output Line Mode	'0' = Mode 1, V-Blanking only. '1' = Mode 2, both H-Blanking and V-Blanking.
D4	Horizontal Sync. (HSYNC, DPI I/F)	'0' = Horizontal Sync. line is Off ("Low"). '1' = Horizontal Sync. line is On ("High").
D3	Vertical Sync. (VSYNC, DPI I/F)	'0' = Vertical Sync. line is Off ("Low"). '1' = Vertical Sync. line is On ("High").
D2	Pixel Clock (DCK, DPI I/F)	'0' = PCLK line is Off ("Low"). '1' = PCLK line is On ("High").
D1	Data Enable (ENABLE, DPI I/F)	'0' = DE line is Off ("Low"). '1' = DE line is On ("High").
D0	Parity Error on DSI	'0'=No Parity Error. '1'=Parity Error.

Gamma Curve Selected	B8	B7	B6
Gamma Curve 1	0	0	0
Gamma Curve 2	0	0	1
Gamma Curve 3	0	1	0
Gamma Curve 4	0	1	1
Not Defined	1	0	0
Not Defined	1	0	1
Not Defined	1	1	0
Not Defined	1	1	1

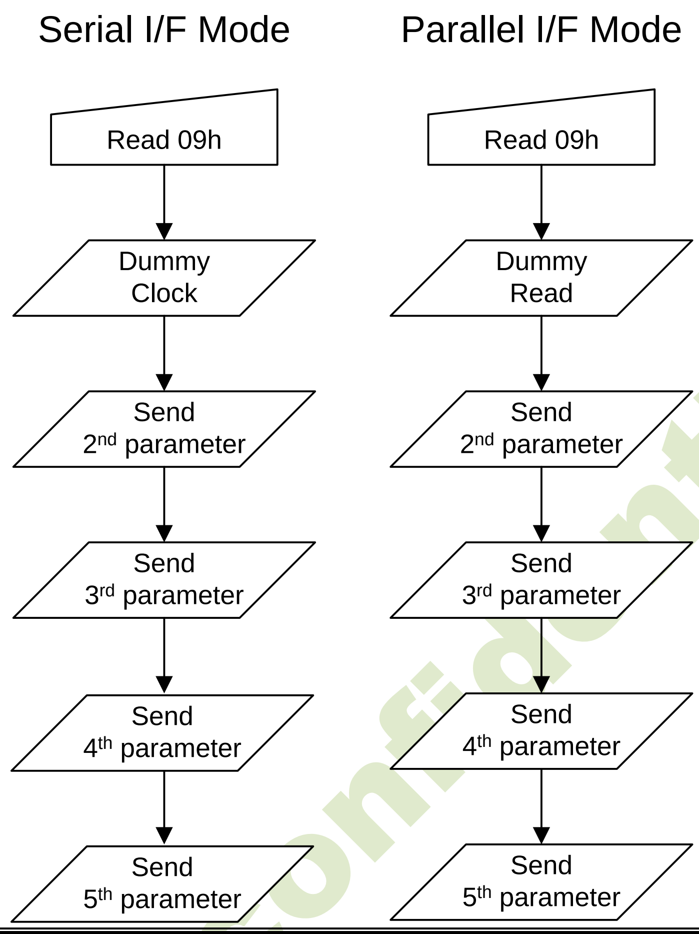
Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	98h	51h	01h
SW Reset	98h	51h	01h
HW Reset	98h	51h	01h

Flow Chart	

Serial I/F Mode
Parallel I/F Mode
Read 09h
Dummy Clock
Send 2nd parameter
Send 3rd parameter
Send 4th parameter
Send 5th parameter
Read 09h
Dummy Read
Send 2nd parameter
Send 3rd parameter
Send 4th parameter
Send 5th parameter

9.2.9. RDDPM: Read Display Power Mode (0Ah)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	1	0	0A
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	

Description

Bit	Description	Value
D7	Booster Voltage Status	‘0’ = Booster Off. ‘1’ = Booster On.
D6	Idle Mode On/Off	‘0’ = Idle Mode Off. ‘1’ = Idle Mode On.
D5	Partial Mode On/Off	‘0’ = Partial Mode Off. ‘1’ = Partial Mode On.
D4	Sleep In/Out	‘0’ = Sleep In Mode. ‘1’ = Sleep Out Mode.
D3	Display Normal Mode On/Off	‘0’ = Display Normal Mode Off. ‘1’ = Display Normal Mode On.
D2	Display On/Off	‘0’ = Display is Off. ‘1’ = Display is On.
D1	Not Defined	Set to ‘0’
D0	Not Defined	Set to ‘0’

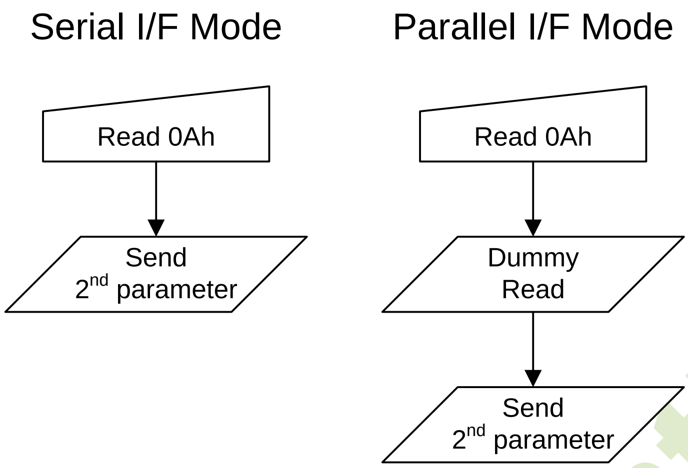
Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
SW Reset	08h
HW Reset	08h

Flow Chart	Serial I/F Mode Parallel I/F Mode Read 0Ah Send 2nd parameter Read 0Ah Dummy Read Send 2nd parameter

9.2.10. RDDMADCTL: Read Display MADCTL (0Bh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	1	1	0B
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Page Address Order (MY)	‘0’ = Top to Bottom (When MADCTL B7=’0’). ‘1’ = Bottom to Top (When MADCTL B7=’1’).
D6	Column Address Order (MX)	‘0’ = Left to Right (When MADCTL B6=’0’). ‘1’ = Right to Left (When MADCTL B6=’1’).
D5	Page/Column Order (MV)	‘0’ = Normal Mode (When MADCTL B5=’0’). ‘1’ = Reverse Mode (When MADCTL B5=’1’).
D4	Line Address Order	‘0’ = LCD Refresh Top to Bottom (When MADCTL B4=’0’). ‘1’ = LCD Refresh Bottom to Top (When MADCTL B4=’1’).
D3	RGB/BGR Order	‘0’ = RGB (When MADCTL B3=’0’). ‘1’ = BGR (When MADCTL B3=’1’).
D2	Display Data Latch Order	‘0’ = LCD Refresh Left to Right (When MADCTL B2=’0’). ‘1’ = LCD Refresh Right to Left (When MADCTL B2=’1’).
D1	Source scan sequence	‘0’ = Source output Left to Right (When MADCTL B1=’0’). ‘1’ = Source output Right to Left (When MADCTL B1=’1’).
D0	Gate scan sequence	‘0’ = Gate output Top to Bottom (When MADCTL B1=’0’). ‘1’ = Gate output Bottom to Top (When MADCTL B1=’1’)

Restriction

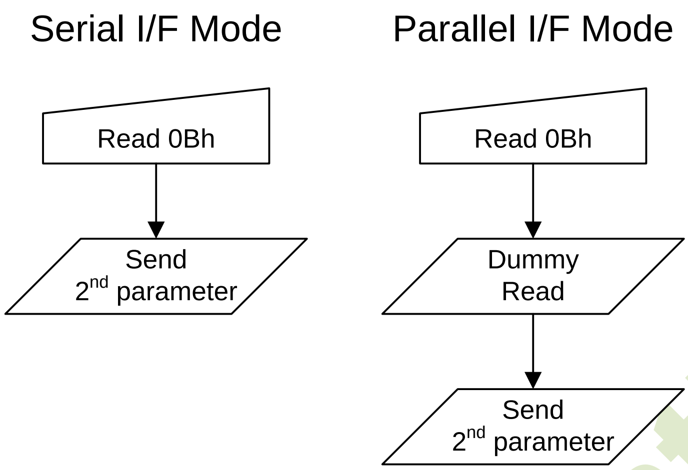
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	No Change
HW Reset	00h

Flow Chart	

Serial I/F Mode
Read 0Bh
Send
2nd parameter
Parallel I/F Mode
Read 0Bh
Dummy
Read
Send
2nd parameter

9.2.11. RDDCOLMOD: Read Display Pixel Format (0Ch)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	0	0	0C
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	-	Set to '0'
D6	DSI Interface Color Format	'011' = 12 bits/pixel
D5		'101' = 16 bits/pixel
D4		'110' = 18 bits/pixel
D3	-	Set to '0'
D2	Control Interface Color Format	'011' = 12 bits/pixel
D1		'101' = 16 bits/pixel
D0		'110' = 18 bits/pixel

Others are no define and invalid

"-" Don't care

Restriction

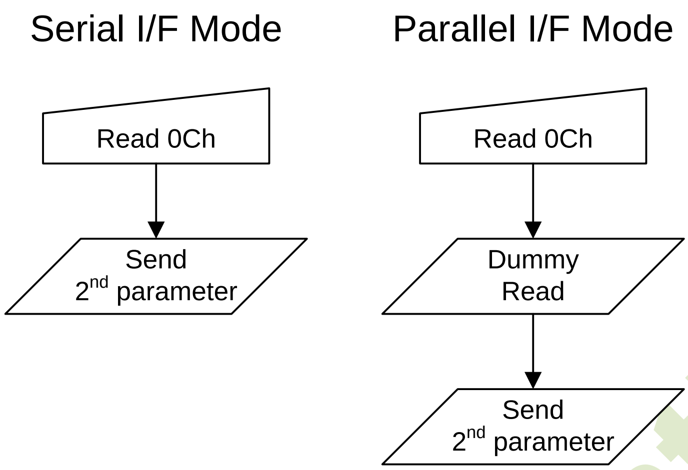
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	06h (18 bits/pixel)
SW Reset	No Change
HW Reset	06h (18 bits/pixel)

Flow Chart	

Serial I/F Mode
Parallel I/F Mode
Read 0Ch
Send 2nd parameter
Read 0Ch
Dummy Read
Send 2nd parameter

9.2.12. RDDIM: Read Display Image Mode (0Dh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	0	1	0D
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Vertical Scrolling On/Off	‘0’ = Vertical Scrolling is Off. ‘1’ = Vertical Scrolling is On.
D6	Horizontal Scrolling Status	This bit is not applicable for this project, set it to ‘0’
D5	Inversion On/Off	‘0’ = Inversion is Off. ‘1’ = Inversion is On.
D4	All Pixels On	‘0’ = Normal Display ‘1’ = White Display
D3	All Pixels Off	‘0’ = Normal Display ‘1’ = Black Display
D2 D1 D0	Gamma Curve Selection	(see table below)

Gamma Curve Selected	D2	D1	D0	Gamma Set (26h)
Gamma Curve 1	0	0	0	CG0
Gamma Curve 2	0	0	1	CG1
Gamma Curve 3	0	1	0	CG2
Gamma Curve 4	0	1	1	CG3
Not Defined	1	0	0	
Not Defined	1	0	1	
Not Defined	1	1	0	
Not Defined	1	1	1	

Restriction: -

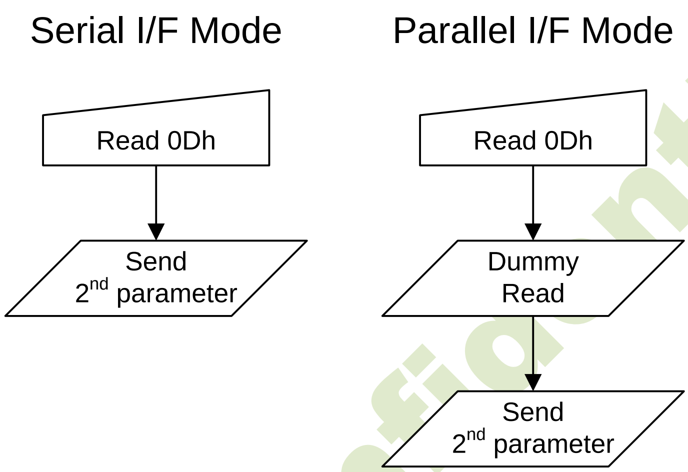
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



9.2.13. RDDSM: Read Display Signal Mode (0Eh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	1	0	0E
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	TEON	TEM	0	0	0	0	0	D0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Tearing Effect Line On/Off	'0' = Tearing Effect Line Off. '1' = Tearing Effect On.
D6	Tearing Effect Line Output Mode	'0' = Mode 1. '1' = Mode 2.
D5	Horizontal Sync. On/Off. (DSI I/F)	'0' = Horizontal Sync. Line is Off ("Low"). '1' = Horizontal Sync. Line is On ("High").
D4	Vertical Sync. On/Off. (DSI I/F)	'0' = Vertical Sync. Line is Off ("Low"). '1' = Vertical Sync. Line is On ("High").
D3	Pixel Clock(PCLK) On/Off. (DSI I/F)	'0' = PCLK line is Off ("Low"). '1' = PCLK line is On ("High").
D2	Data Enable(DE) On/Off. (DSI I/F))	'0' = DE line is Off ("Low"). '1' = DE line is On ("High").
D1	Not Defined	For future use and are set to '0'.
D0	Parity Error on DSI	'0'=No Parity Error. '1'=Parity Error.

Restriction

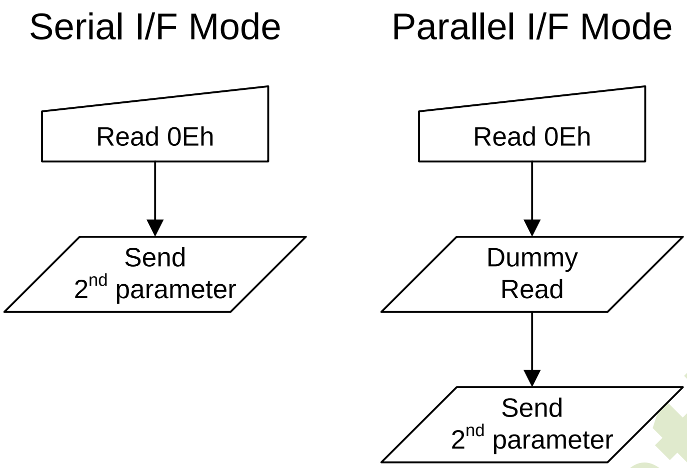
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	Serial I/F Mode Read 0Eh Send 2nd parameter Parallel I/F Mode Read 0Eh Dummy Read Send 2nd parameter

9.2.14. RDDSDR: Read Display Self-Diagnostic Result (0Fh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	1	1	0F
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	D7	D6	D5	D4	0	0	0	0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Register Loading Detection	See section "Sleep Out –command and self-diagnostic functions of the display module"
D6	Functionality Detection	
D5	Chip Attachment Detection	Set to '0' if feature unimplemented.
D4	Display Glass Break Detection	Set to '0' if feature unimplemented.
D3	Reserved	Set to '0'.
D2		Set to '0'.
D1		Set to '0'.
D0		Set to '0'.

Restriction

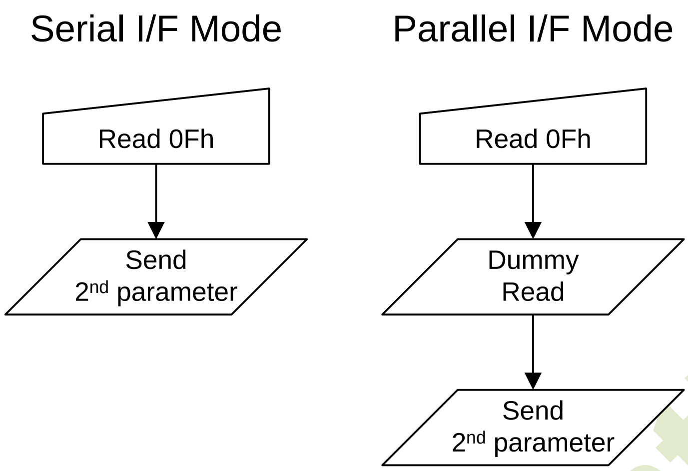
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	

Serial I/F Mode
Parallel I/F Mode
Read 0Fh
Send
2nd parameter
Read 0Fh
Dummy
Read
Send
2nd parameter

9.2.15. SLPIN: Sleep In (10h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	0	0	10
Parameter	No Parameter												

Description

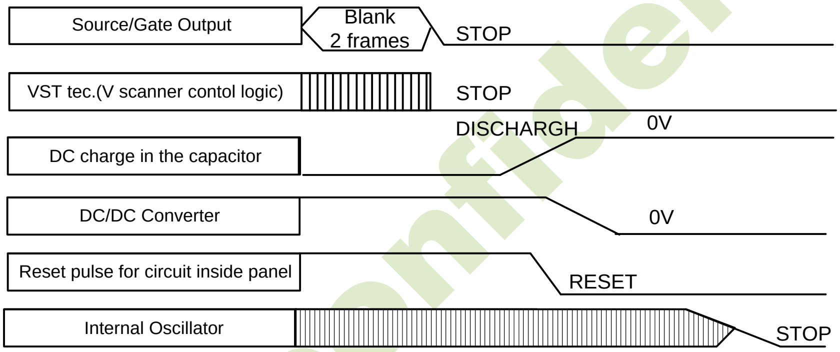
This command causes the LCD module to enter the minimum power consumption mode.

In this mode, all unnecessary blocks inside the display module are disabled except interface communication.

This is the lowest power mode the display module supports.

MCU interface and memory are still working and the memory keeps its contents.

In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.



Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).

It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.

It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

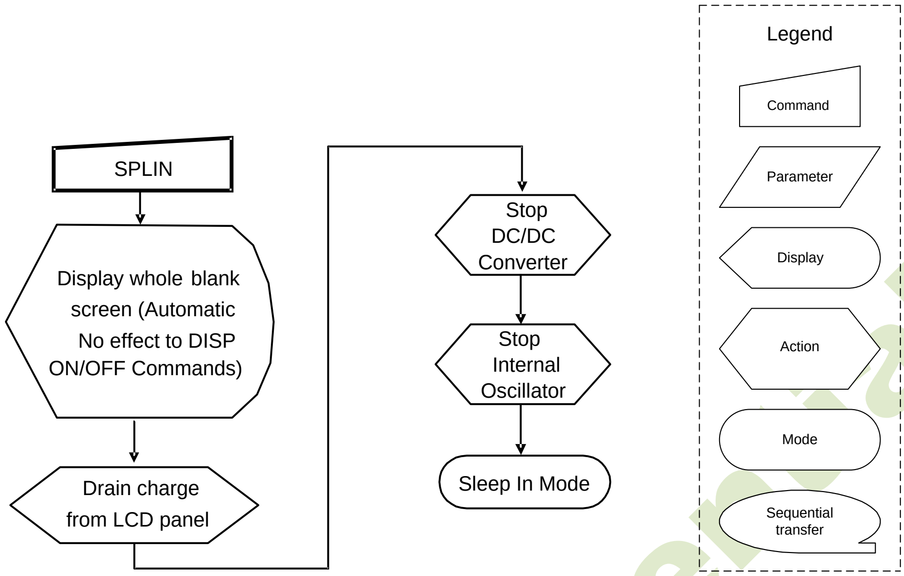
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

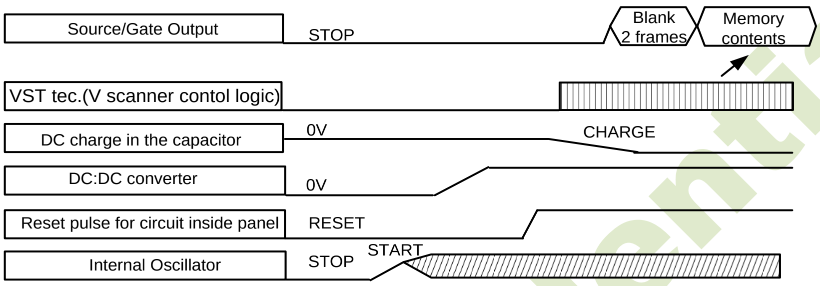
Status	Default Value
Power On Sequence	Sleep in mode
SW Reset	Sleep in mode
HW Reset	Sleep in mode

Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.

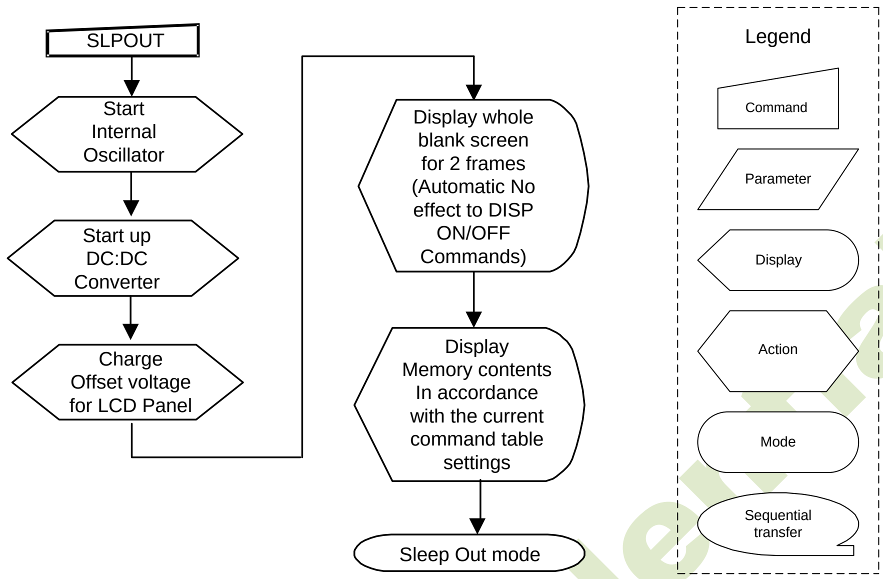


9.2.16. SLPOUT: Sleep Out (11h)

<table>
<tr><th>CMD/Pas</th><th>D/CX</th><th>WRX</th><th>RDX</th><th>D17-8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns off sleep mode.
In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.

</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h).
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
The display module loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.
The display module is doing self-diagnostic functions during this 5msec. It will be necessary to alit 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Sleep in mode</td></tr>
<tr><td>SW Reset</td><td>Sleep in mode</td></tr>
<tr><td>HW Reset</td><td>Sleep in mode</td></tr>
</table></td></tr>
</table>

Flow Chart

It takes 120msec to become Sleep Out mode after SLPOUT command issued.



9.2.17. PTLON: Partial Mode ON (12h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	1	0	12
Parameter	No Parameter												
Description	This command turns on partial mode. The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.												
Restriction	This command has no effect when Partial mode is active.												
Register Availability	(see table below)												
Default	(see table below)												
Flow Chart	See Partial Area (30h)												

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	Normal Mode On
SW Reset	Normal Mode On
HW Reset	Normal Mode On

9.2.18. NORON: Normal Display Mode ON (13h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	1	1	13
Parameter	No Parameter												
Description	This command returns the display to normal mode. Normal display mode is means Partial mode off, Scroll mode Off. There is no abnormal visual effect during mode change from Partial mode On to Normal mode On.												
Restriction	This command has no effect when Normal Display mode is active.												
Register Availability	(see table below)												
Default	(see table below)												
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.												

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	Normal Mode On
SW Reset	Normal Mode On
HW Reset	Normal Mode On

9.2.19. INVOFF: Display Inversion OFF (20h)

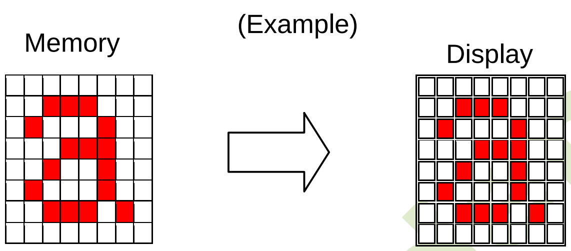
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	0	0	0	0	20
Parameter	No Parameter												

Description

This command is used to recover from display inversion mode.

This command makes no change of contents of frame memory.

This command does not change any other status.



Restriction

This command has no effect when module is already in inversion off mode.

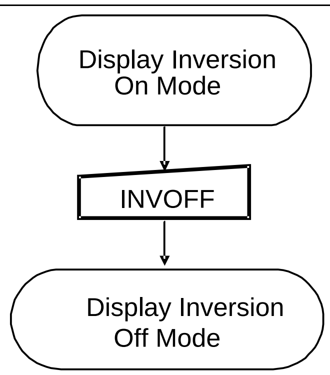
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
SW Reset	Display Inversion off
HW Reset	Display Inversion off

Flow Chart



9.2.20. INVON: Display Inversion ON (21h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	0	0	0	1	21
Parameter	No Parameter												

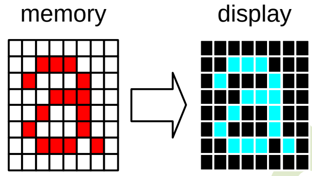
Description

This command is used to enter into display inversion mode.

This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.

This command does not change any other status.

(Example)



Restriction

This command has no effect when module is already in inversion on mode.

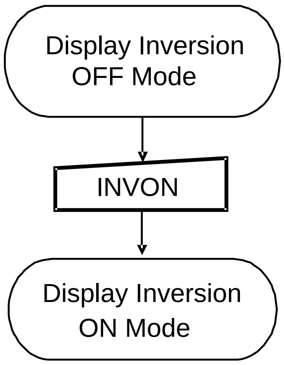
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
SW Reset	Display Inversion off
HW Reset	Display Inversion off

Flow Chart



9.2.21. GAMSET: Gamma Set (26h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	0	1	1	0	26
1st Parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:

GC[7..0]	Parameter	Curve selected
01h	GC0	Gamma Curve 1
02h	GC1	Gamma Curve 2
04h	GC2	Gamma Curve 3
08h	GC3	Gamma Curve 4

Note: All other values are undefined.

Restriction

Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

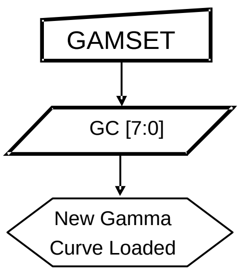
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
SW Reset	01h
HW Reset	01h

Flow Chart



9.2.22. DISPOFF: Display Off (28h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	0	0	28

Parameter

No Parameter

Description

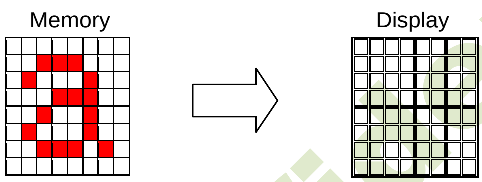
This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.

This command makes no change of contents of frame memory.

This command does not change any other status.

There will be no abnormal visible effect on the display.

Example



Restriction

This command has no effect when module is already in display off mode.

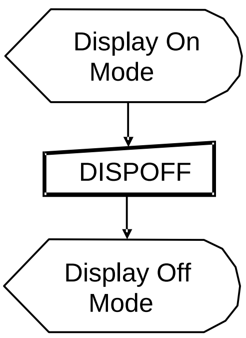
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
SW Reset	Display off
HW Reset	Display off

Flow Chart



9.2.23. DISPON: Display On (29h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	0	1	29
Parameter	No Parameter												

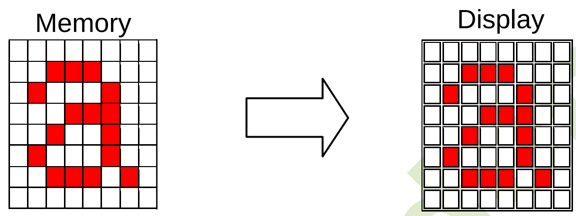
Description

This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.

This command makes no change of contents of frame memory.

This command does not change any other status.

(Example)



Restriction

This command has no effect when module is already in display on mode.

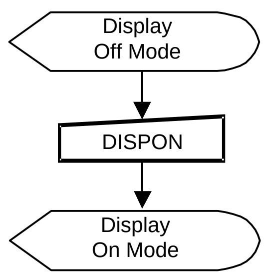
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
SW Reset	Display off
HW Reset	Display off

Flow Chart



9.2.24. CASET: Column Address Set (2Ah)

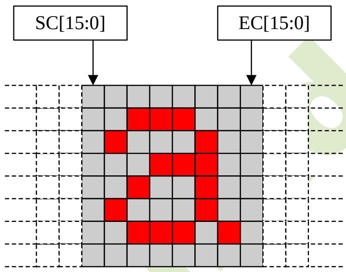
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	1	0	2A
1st Parameter	1	↑	1	-	SC[15:8]								
2nd Parameter	1	↑	1	-	SC[7:0]								
3rd Parameter	1	↑	1	-	EC[15:0]								
4th Parameter	1	↑	1	-	EC[7:0]								

Description

This command is used to define area of frame memory where MCU can access.

This command makes no change on the other driver status.

The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



Restriction

SC[15:0] always must be equal to or less than EC[15:0]

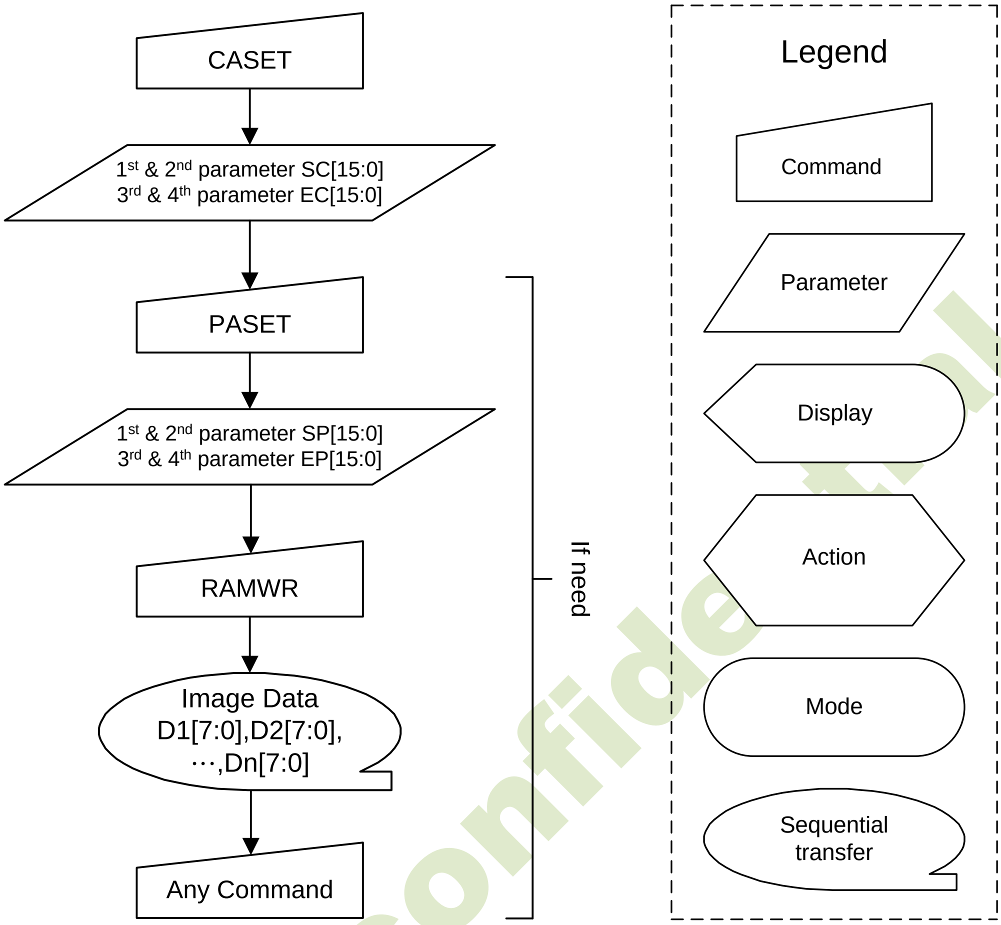
Note 1: When SC[15:0] or EC[15:0] is greater than 7Fh (when MADCTL's B5=0) or 9Fh (when MADCTL's B5=1), data of out of range will be ignored

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SC[15:0] = 0000h	EC[15:0] = 00EFh
SW Reset	SC[15:0] = 0000h	When MV=0: EC[15:0] = 00EFh When MV=1: EC[15:0] = 013Fh
HW Reset	SC[15:0] = 0000h	EC[15:0] = 00EFh

Flow Chart	

CASET
1st & 2nd parameter SC[15:0]
3rd & 4th parameter EC[15:0]
PASET
1st & 2nd parameter SP[15:0]
3rd & 4th parameter EP[15:0]
RAMWR
Image Data
D1[7:0],D2[7:0],
…,Dn[7:0]
Any Command
If need
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

9.2.25. PASET: Page Address Set (2Bh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	1	1	2B
1st Parameter	1	↑	1	-	SP[15:8]								
2nd Parameter	1	↑	1	-	SP[7:0]								
3rd Parameter	1	↑	1	-	EP[15:0]								
4th Parameter	1	↑	1	-	EP[7:0]								

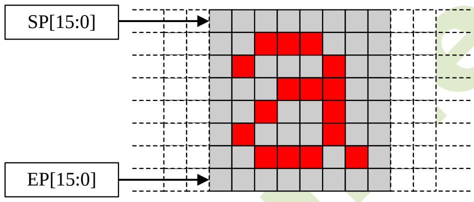
Description

This command is used to define area of frame memory where MCU can access.

This command makes no change on the other driver status.

The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.

Each value represents one Page line in the Frame Memory.



Restriction

SP[15:0] always must be equal to or less than EP[15:0]

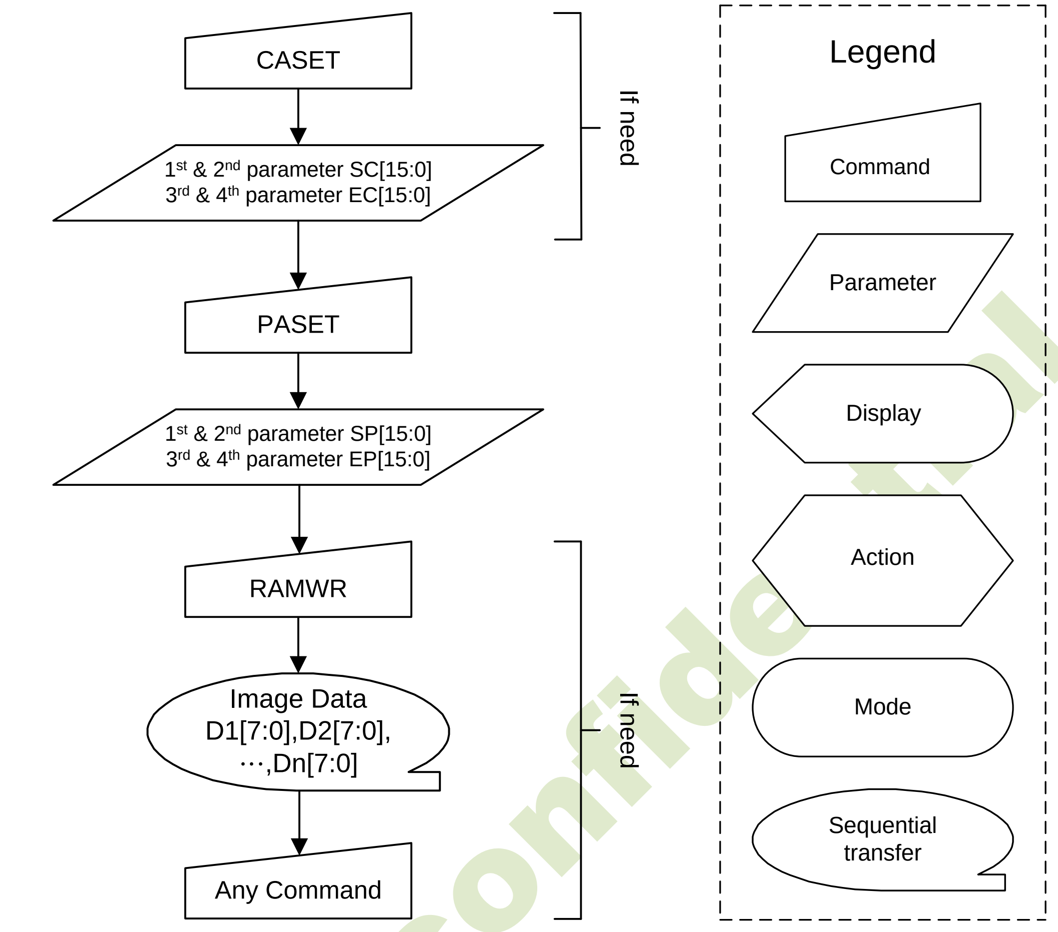
Note 1: When SP[15:0] or EP[15:0] is greater than 9Fh (When MADCTL's B5=0) or 7Fh (When MADCTL's B5=1), data of out of range will be ignored.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP[15:0] = 0000h	EC[15:0] = 013Fh
SW Reset	SP[15:0] = 0000h	When MV=0: EC[15:0] = 013Fh When MV=1: EC[15:0] = 00EFh
HW Reset	SP[15:0] = 0000h	EC[15:0] = 013Fh

Flow Chart	

CASET
1st & 2nd parameter SC[15:0]
3rd & 4th parameter EC[15:0]
PASET
1st & 2nd parameter SP[15:0]
3rd & 4th parameter EP[15:0]
RAMWR
Image Data D1[7:0],D2[7:0], …,Dn[7:0]
Any Command
If need
If need
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

9.2.26. RAMWR: Memory Write (2Ch)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	1	0	0	2C
1st Parameter	1	↑	1	D1[17:8]	D1[7:0]								
…	1	↑	1	Dx[17:8]	Dx[7:0]								
Nth Parameter	1	↑	1	Dn[17:8]	Dn[7:0]								

Description

This command is used to transfer data from MCU to frame memory.

This command makes no change to the other driver status.

When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.

The Start Column/Start Page positions are different in accordance with MADCTL setting.

Then D[17:0] is stored in frame memory and the column register and the page register Incremented.

Sending any other command can stop frame Write.

Restriction

In all color modes, there is no restriction on length of parameters..

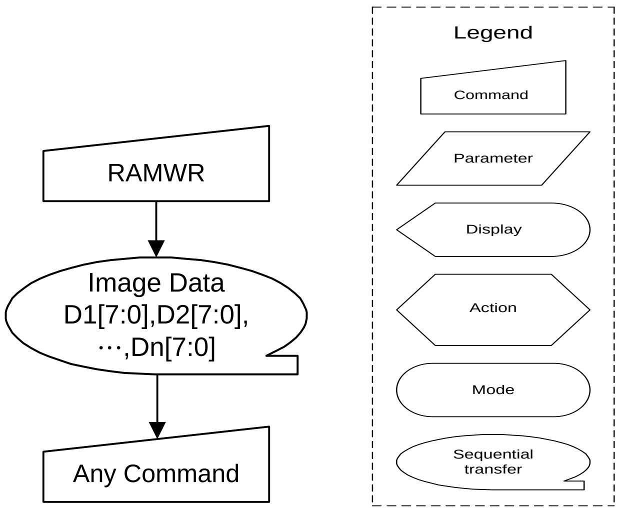
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart



9.2.27. RAMRD: Memory Read (2Eh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	1	1	0	2E
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	D1[17:8]	D1[7:0]								
…	1	1	↑	Dx[17:8]	Dx[7:0]								
Nth Parameter	1	1	↑	Dn[17:8]	Dn[7:0]								

Description

This command is used to transfer data from frame memory to MCU.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.
The Start Column/Start Page positions are different in accordance with MADCTL setting.
Then D[17:0] is read back from the frame memory and the column register and the pageregister incremented.
Frame Read can be stopped by sending any other command.

Restriction

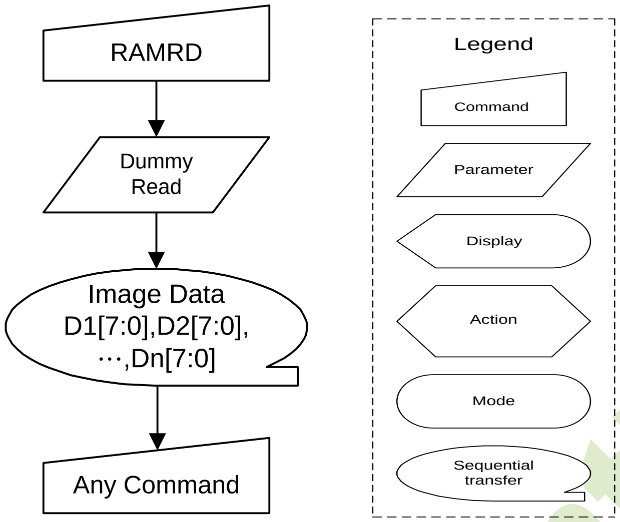
In all color modes, there is no restriction on length of parameters..

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

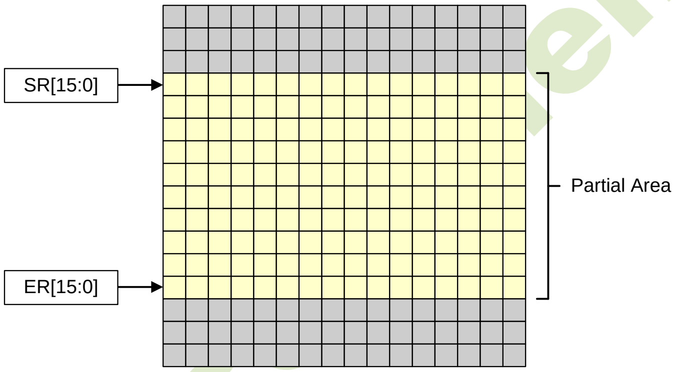
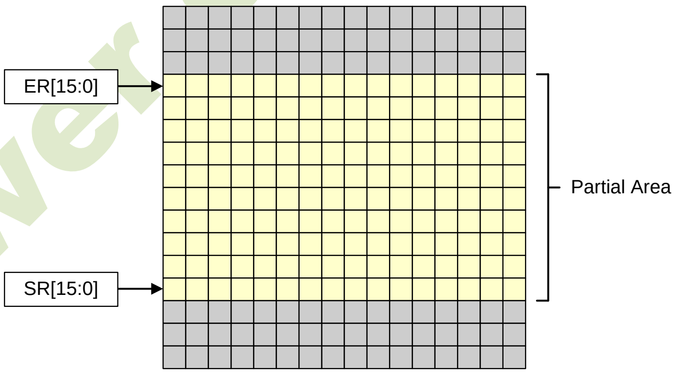
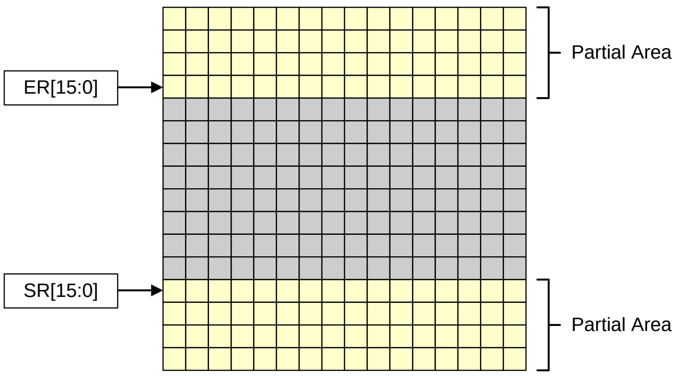
Default

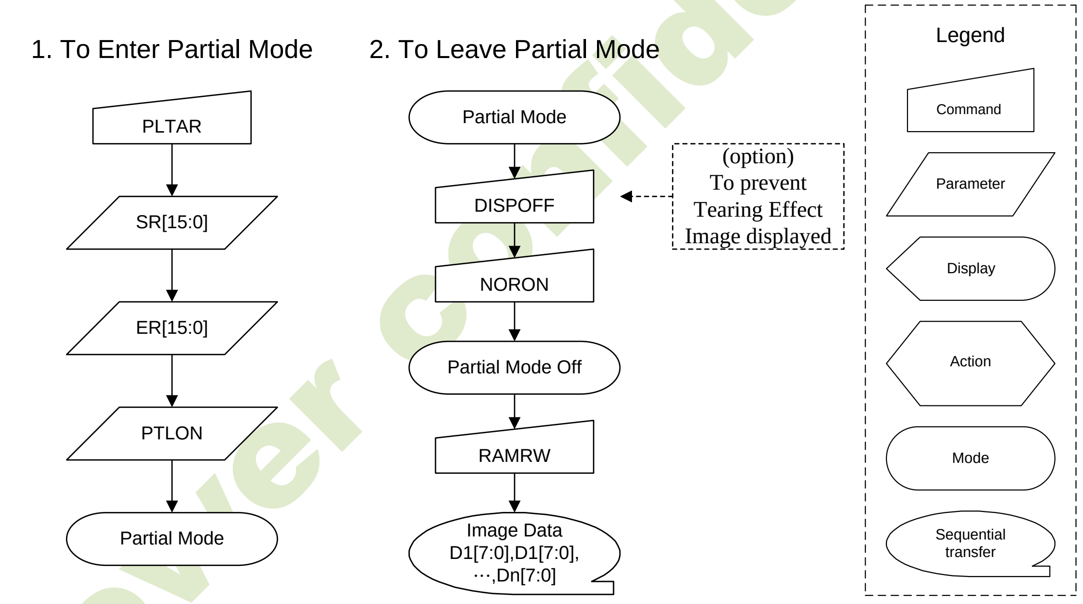
Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart	

RAMRD
Dummy Read
Image Data D1[7:0],D2[7:0], ···,Dn[7:0]
Any Command
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

9.2.28. PTLAR: Partial Area (30h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	0	0	0	30
1st Parameter	1	↑	1	-	SR[15:8]								
2nd Parameter	1	↑	1	-	SR[7:0]								
3rd Parameter	1	↑	1	-	ER[15:0]								
4th Parameter	1	↑	1	-	ER[7:0]								
Description	This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL B4 (ML) = 0:  If End Row>Start Row when MADCTL B4 (ML) = 1:  If End Row<Start Row when MADCTL B4=0:  If End Row = Start Row then the Partial Area will be one row deep.													

<table>
<tr><td>Restriction</td><td>SR[15..0] and ER[15..0] cannot be greater than 13Fh.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>SR[15:0] = 0000h</td><td>ER[15:0] = 013Fh</td></tr>
<tr><td>SW Reset</td><td>SR[15:0] = 0000h</td><td>ER[15:0] = 013Fh</td></tr>
<tr><td>HW Reset</td><td>SR[15:0] = 0000h</td><td>EC[15:0] = 013Fh</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

9.2.29. VSCRDEF: Vertical Scrolling Definition (33h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	0	1	1	33
1st Parameter	1	↑	1	-	TFA[15:8]								
2nd Parameter	1	↑	1	-	TFA [7:0]								
3rd Parameter	1	↑	1	-	VSA[15:0]								
4th Parameter	1	↑	1	-	VSA [7:0]								
5th Parameter	1	↑	1	-	BFA[15:8]								
6th Parameter	1	↑	1	-	BFA[7:0]								

Description

This command defines the Vertical Scrolling Area of the display.

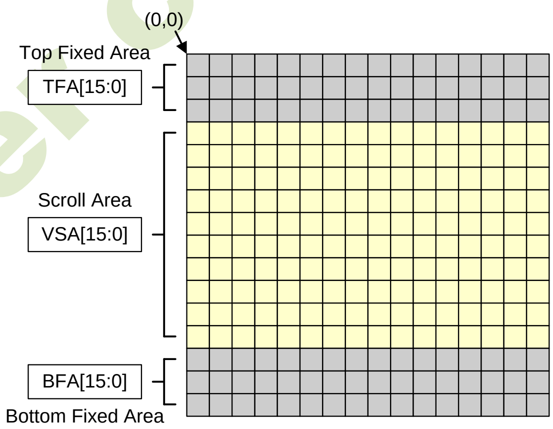
When MADCTL B4 (ML) = 0

The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.

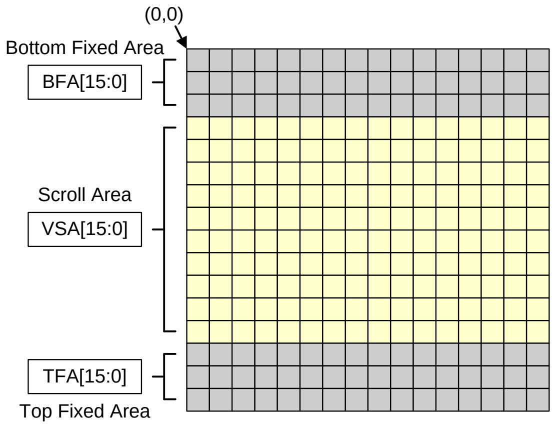


When MADCTL B4 (ML) = 1

The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



Restriction	The condition is (TFA+VSA+BFA)=320, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTL B5 (MV) should be set to '0' – this only affects the Frame Memory Write.

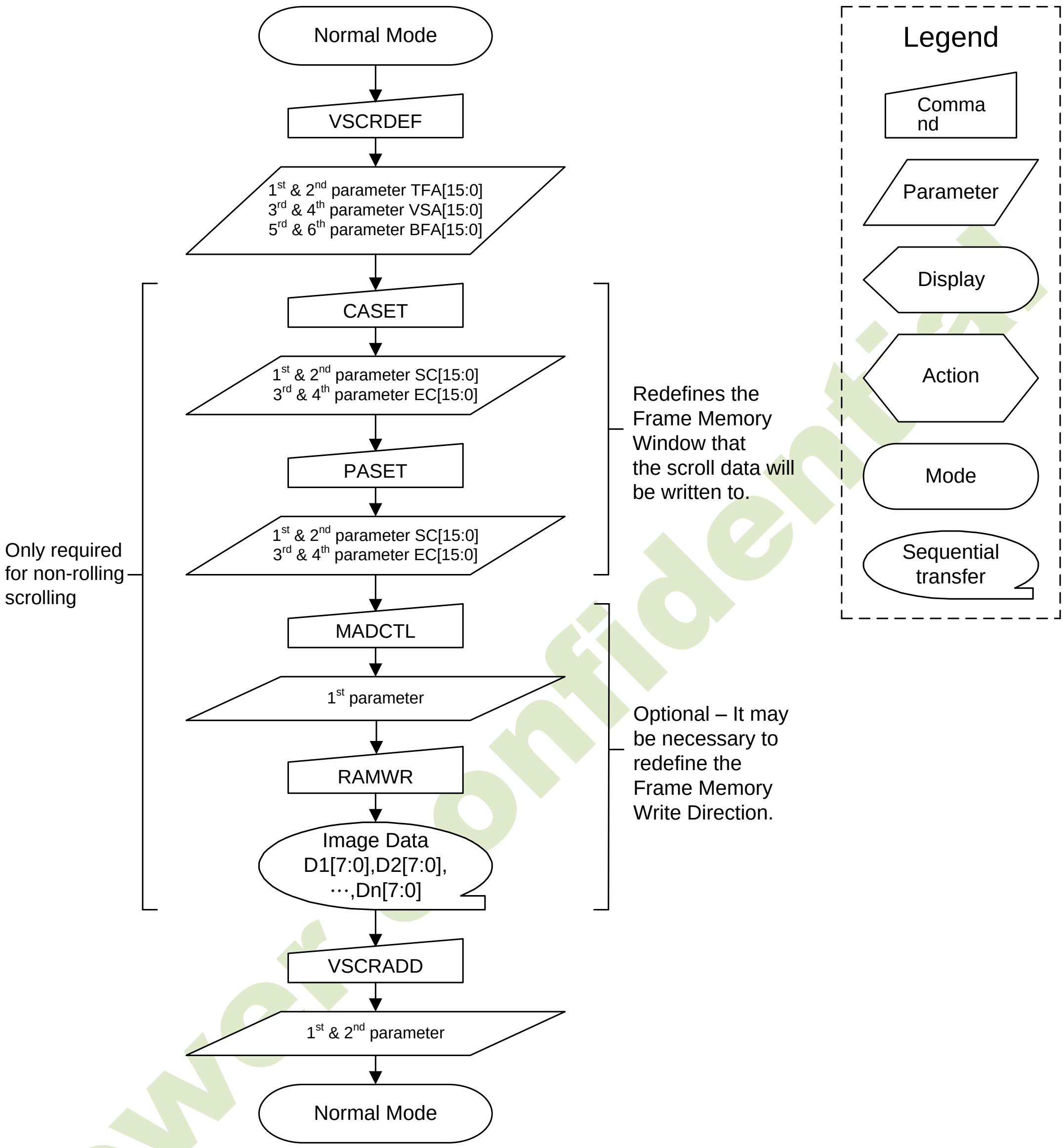
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

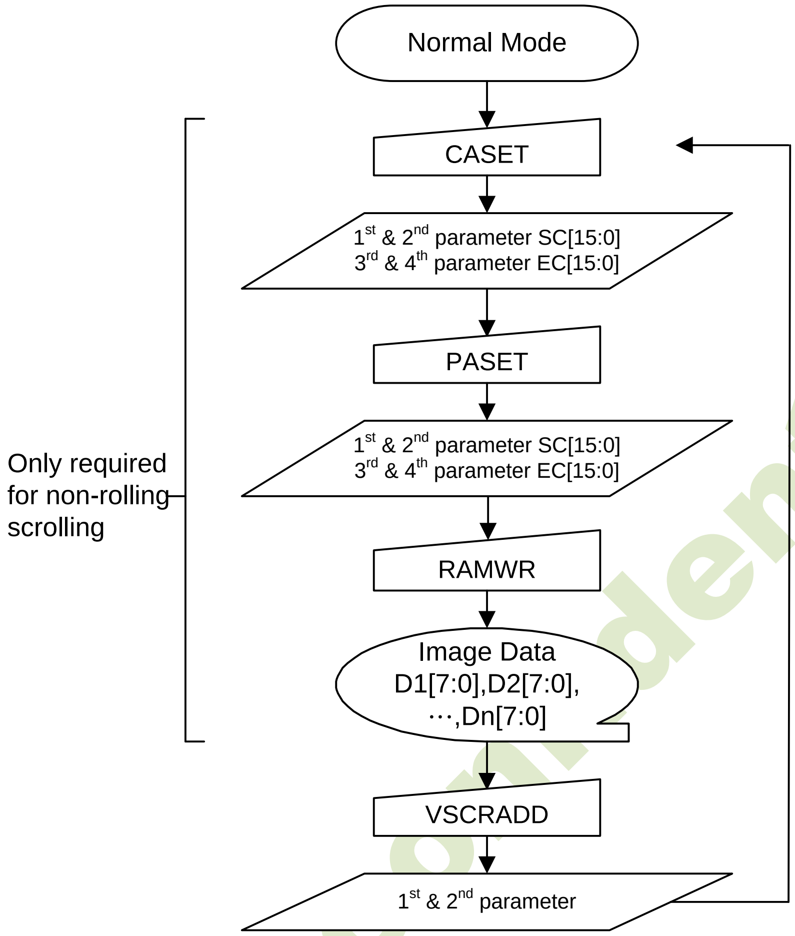
Status	Default Value		
Power On Sequence	TFA[15:0] = 0000h	VSA[15:0] = 0140h	BFA[15:0] = 0000h
SW Reset	TFA[15:0] = 0000h	VSA[15:0] = 0140h	BFA[15:0] = 0000h
HW Reset	TFA[15:0] = 0000h	VSA[15:0] = 0140h	BFA[15:0] = 0000h

Flow Chart	1. To enter Vertical Scroll Mode:

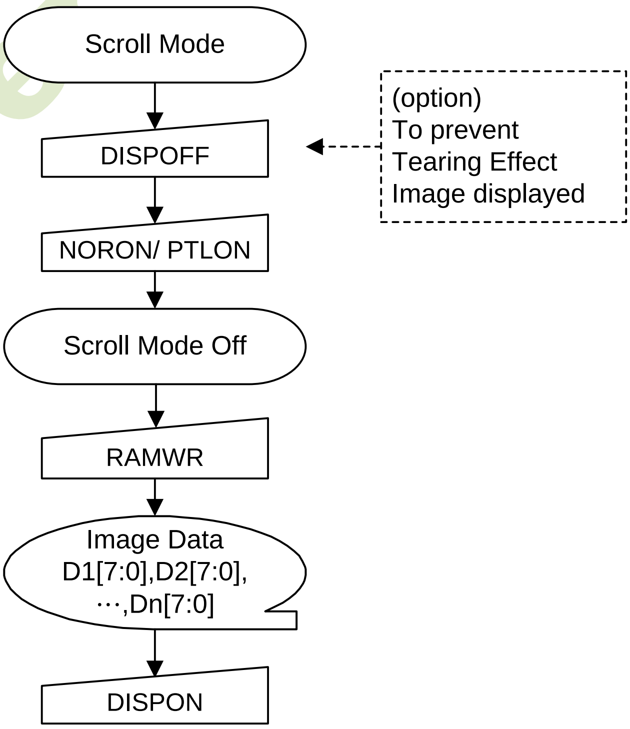


Note The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll:



3. To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

9.2.30. TEOFF: Tearing Effect Line OFF (34h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	0	0	34
Parameter	No Parameter												
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.												
Restriction	This command has no effect when Tearing Effect output is already OFF.												

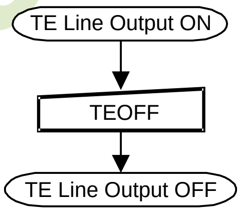
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
SW Reset	Off
HW Reset	Off

Flow Chart



9.2.31. TEON: Tearing Effect Line ON (35h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	0	1	35
1st Parameter	1	↑	1	-	X	X	X	X	X	X	X	M	

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4.

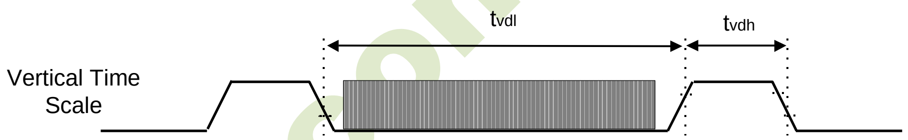
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).

When M=0:

The Tearing Effect Output line consists of V-Blanking information only:

When M=1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

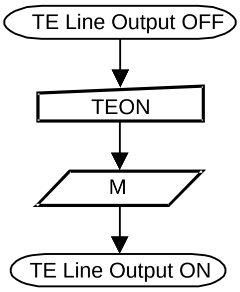
This command has no effect when Tearing Effect output is already ON.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
SW Reset	Off
HW Reset	Off

Flow Chart	

9.2.32. MADCTL: Memory Access Control(36h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	1	0	36
1st Parameter	1	↑	1	-	B7	B6	B5	B4	B3	B2	B1	B0	

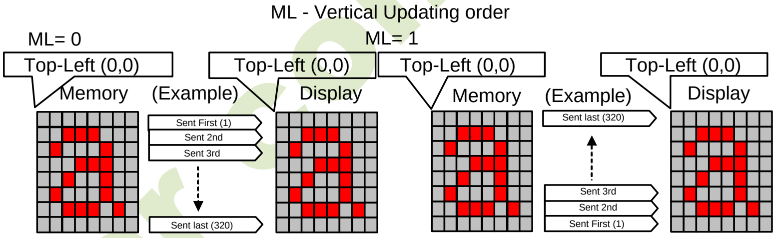
Description

This command defines read/ write scanning direction of frame memory.

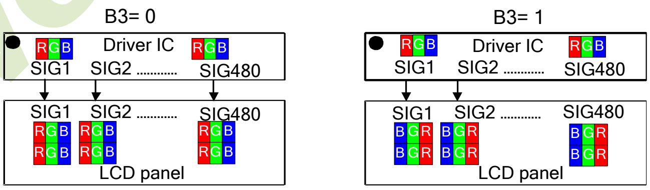
This command makes no change on the other driver status.

Bit	NAME	DESCRIPTION
B7	PAGE ADDRESS ORDER (MY)	These 3 bits controls MCU to memory write/read direction.
B6	COLUMN ADDRESS ORDER (MX)	
B5	PAGE/COLUMN SELECTION (MV)	
B4	Vertical ORDER (ML)	LCD vertical refresh direction control
B3	RGB-BGR ORDER (BGR)	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel
B2	Horizontal ORDER (MH)	LCD horizontal refresh direction control
B1	Flip Horizontal (SS)	Select the Source driver scan direction on panel module
B0	Flip Vertical (GS)	Select the Gate driver scan direction on panel module

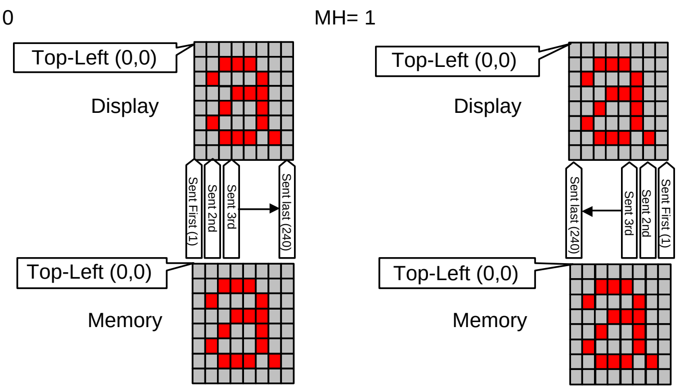
ML - Vertical Updating order



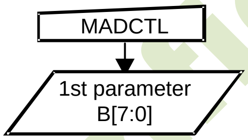
RGB-BGR Order



MH - Horizontal Updating order



Note: Top-Left (0,0) means a physical memory location

<table>
<tr><td>Restriction</td><td>D1 and D0 are set to ‘00’ internally. D2 is implemented if the LCD is updating pixel-bypixel.
D2 is set to ‘0’ internally if the LCD is updating line-by-line.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

9.2.33. VSCRSADD: Vertical Scrolling Start Address (37h)

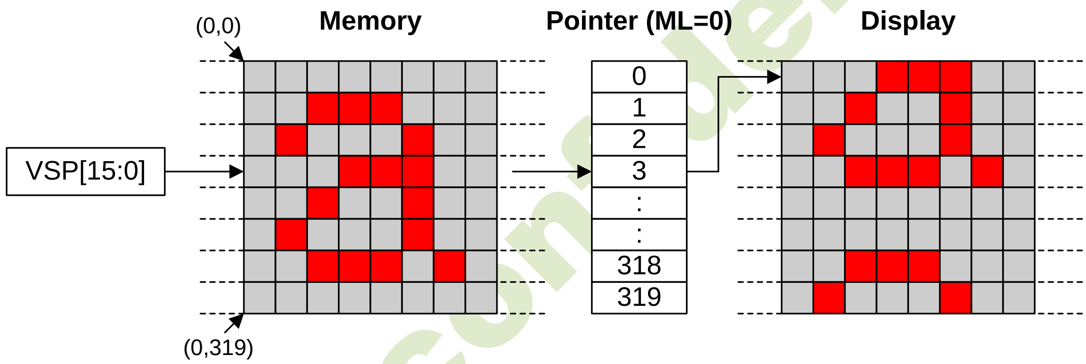
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	1	1	37
1st Parameter	1	↑	1	-	VSP[15:8]								
2nd Parameter	1	↑	1	-	VSP[7:0]								

Description

This command is used together with 錯誤! 找不到參照來源。. These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

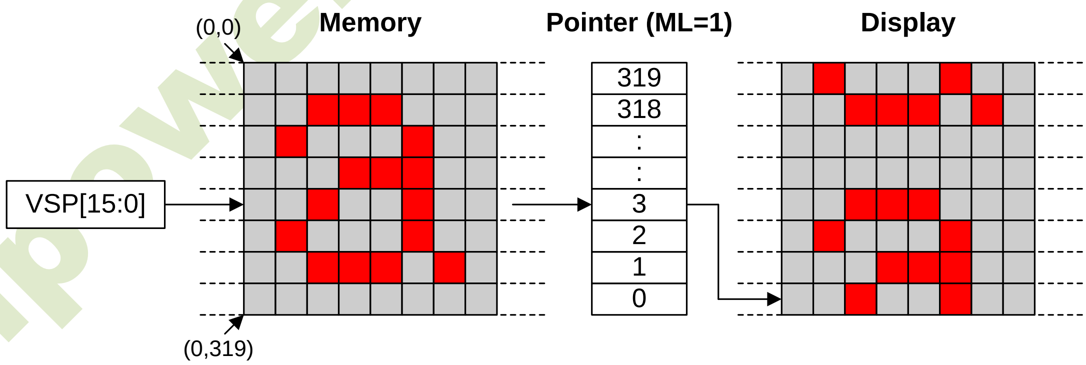
When MADCTL B4 (ML) = 0

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP = '3'.



When MADCTL B4 (ML) = 1

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP = '3'.



Note1: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

Note3: VSP refers to the Frame Memory line Pointer.

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by 錯誤! 找不到參照來源。 – otherwise undesirable image will be displayed on the Panel.

<table>
<tr><td>Register
Availability</td><td>

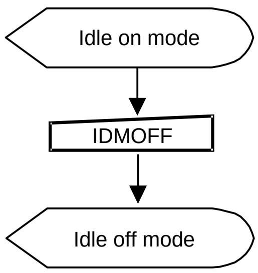
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No
Sleep In	Yes

</td></tr>
<tr><td>Default</td><td>

Status	Default Value
Power On Sequence	0000h
SW Reset	0000h
HW Reset	0000h

</td></tr>
<tr><td>Flow Chart</td><td>See 錯誤! 找不到參照來源。 description</td></tr>
</table>

9.2.34. IDMOFF: Idle Mode OFF (38h)

<table>
<tr><th>CMD/Pas</th><th>D/CX</th><th>WRX</th><th>RDX</th><th>D17-8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 262144 colors.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Idle mode off</td></tr>
<tr><td>SW Reset</td><td>Idle mode off</td></tr>
<tr><td>HW Reset</td><td>Idle mode off</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">
</td></tr>
</table>

9.2.35. IDMON: Idle Mode ON (39h)

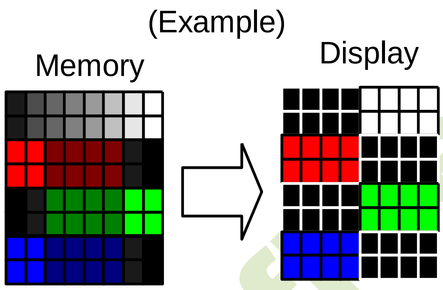
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	0	1	39
Parameter	No Parameter												

Description

This command is used to enter into Idle mode on.

In the idle on mode, color expression is reduced.

The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



Color	$R_5R_4R_3R_2R_1R_0$	$G_5G_4G_3G_2G_1G_0$	$B_5B_4B_3B_2B_1B_0$
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

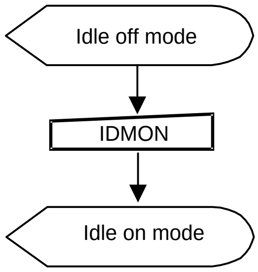
This command has no effect when module is already in idle on mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode off
SW Reset	Idle mode off
HW Reset	Idle mode off

Flow Chart	

9.2.36. COLMOD: Pixel Format Set (3Ah)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	1	0	3A
1st Parameter	1	↑	1	-	0	D6	D5	D4	0	D2	D1	D0	

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface.

The formats are shown in the table:

Bit	Description	Value
D7	-	Set to '0'
D6	DSI Interface Color Format	'011' = 12 bits/pixel
D5		'101' = 16 bits/pixel
D4		'110' = 18 bits/pixel
D3	-	Set to '0'
D2	Control Interface Color Format	'011' = 12 bits/pixel
D1		'101' = 16 bits/pixel
D0		'110' = 18 bits/pixel

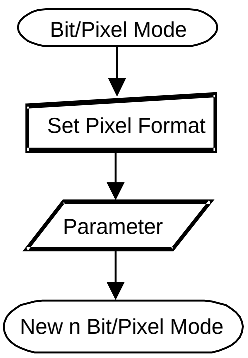
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	18bits/pixel
SW Reset	No change
HW Reset	18bits/pixel

Flow Chart	Bit/Pixel Mode Set Pixel Format Parameter New n Bit/Pixel Mode

9.2.37. WRMEMC: Write Memory Continue (3Ch)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	1	0	0	3C
1st Parameter	1	↑	1	D1[17:8]	D1[7:0]								
…	1	↑	1	Dx[17:8]	Dx[7:0]								
Nth Parameter	1	↑	1	Dn[17:8]	Dn[7:0]								

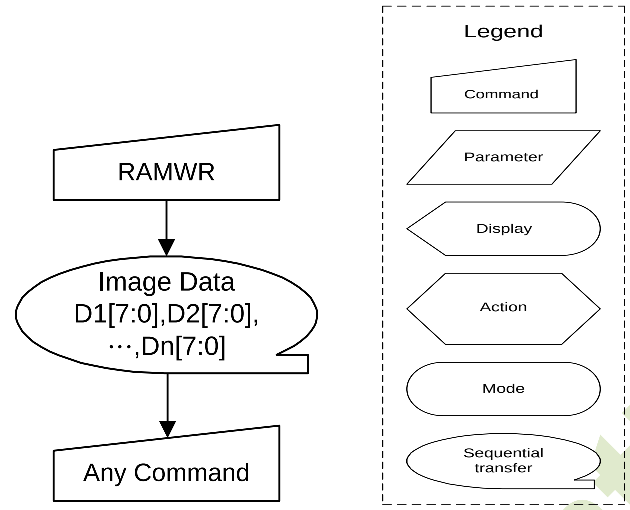
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous Write Memory Continue (3Ch) or Memory Write Start (2Ch) command. Sending any other command can stop frame Write. If MATCDL MV = 0: Data is written continuing from the pixel location after the write range of the previous Memory Write Start (2Ch) or Write Memory Continue (3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. If MATCDL MV = 1: Data is written continuing from the pixel location after the write range of the previous Memory Write Start (2Ch) or Write Memory Continue (3Ch). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.
Restriction	A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart	

RAMWR
Image Data D1[7:0],D2[7:0], …,Dn[7:0]
Any Command
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

9.2.38. RDMEMC: Read Memory Continue (3Eh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	1	1	0	2E
1st Parameter	1	1	↑		-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	D1[17:8]	D1[7:0]								
…	1	1	↑	Dx[17:8]	Dx[7:0]								
Nth Parameter	1	1	↑	Dn[17:8]	Dn[7:0]								

Description

This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous Read Memory Continue (3Eh) or Memory Read Start (2Eh) command.

If MATCDL MV=0:

Pixels are read continuing from the pixel location after the read range of the previous Memory Read Start (2Eh) or Read Memory Continue (3Eh). The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If MATCDL MV=1:

Pixels are read continuing from the pixel location after the read range of the previous Memory Read Start (2Eh) or Read Memory Continue (3Eh). The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

Regardless of the color mode set in Interface Pixel Format (3Ah), the pixel format returned by Read Memory Continue (3Eh) is always 18-bit so there is no restriction on the length of data.

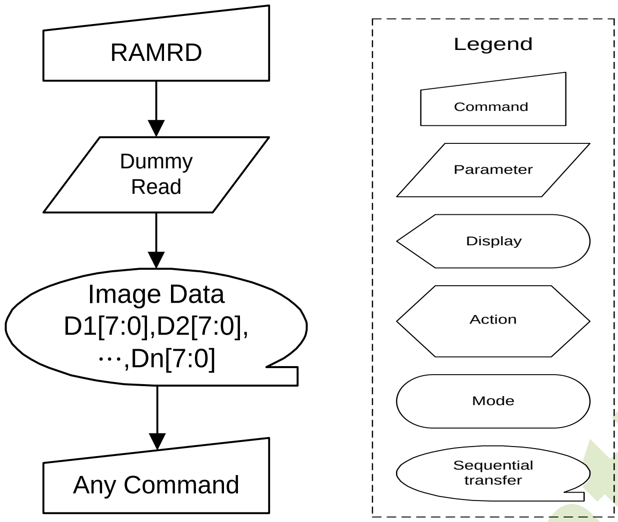
A Memory Read Start (2Eh) should follow a Column Address Set (2Ah), Page Address Set (2Bh) or Memory Access Control (36h) to define the read location. Otherwise, data read with Read Memory Continue (3Eh) is undefined..

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart	

RAMRD
Dummy Read
Image Data D1[7:0],D2[7:0], …,Dn[7:0]
Any Command
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

9.2.39. STE: Set Tear Scanline (44h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	0	0	1	0	0	44
1st Parameter	1	↑	1	-	TELINE[15:8]								
2th Parameter	1	↑	1	-	TELINE[7:0]								

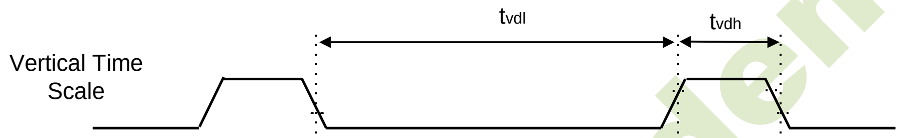
Description

This command is turns on the display module's Tearing Effect output signal on the TE signal

Line when the display module reaches line TELINE. The TE signal is not affected by changing MADCTL bit B4.

The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

The Tearing Effect Output line consists of V-Blanking information only:



Note: That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.

Restriction

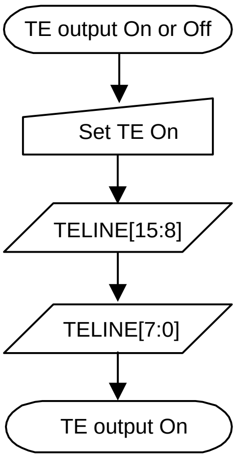
A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
SW Reset	0000h
HW Reset	0000h

Flow Chart	TE output On or Off Set TE On TELINE[15:8] TELINE[7:0] TE output On

9.2.40. GSCAN: Get Scanline (45h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	0	0	1	0	1	45
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	SLN[15:0]								
3rd Parameter	1	1	↑	-	SLN [7:0]								

Description

The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.

When in Sleep Mode, the value returned by get scanline is undefined.

Restriction

-

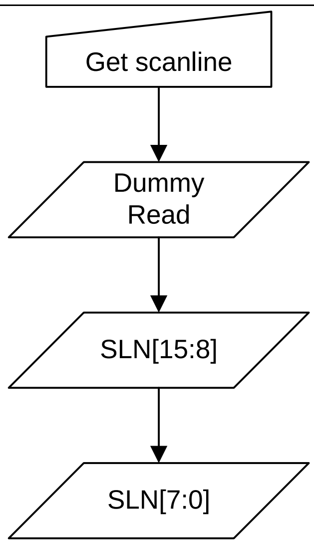
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
SW Reset	0000h
HW Reset	0000h

Flow Chart



9.2.41. WRDISBV: Write Display Brightness (51h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	0	0	1	51
1st Parameter	1	↑	1	-	DBV[7:0]								

Description

This command is used to adjust the brightness value of the display.

It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification.

In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

See chapter "Content adaptive brightness control (CABC) function"

Restriction

-

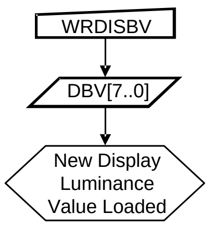
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



9.2.42. RDDISBV: Read Display Brightness Value (52h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	0	1	0	52
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	DBV:0]								

Description

This command returns the brightness value of the display.

It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

DBV[7:0] is reset when display is in sleep-in mode.

DBV[7:0] is '0' when bit BCTRL of Write CTRL Display (53h)" command is '0'.

DBV[7:0] is manual set brightness specified with Write CTRL Display (53h)" command when bit BCTRL is '1'.

Restriction

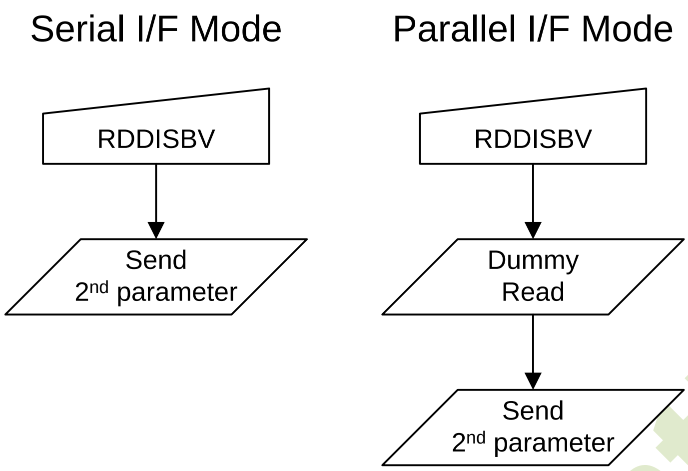
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	

Serial I/F Mode
Parallel I/F Mode
RDDISBV
Send 2nd parameter
RDDISBV
Dummy Read
Send 2nd parameter

9.2.43. WRCTRLD: Write CTRL Display (53h)

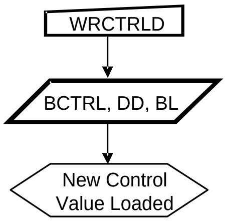
CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	0	1	1	53
1st Parameter	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0	
Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (DD): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.												
Restriction	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	

9.2.44. RDCTRLD: Read CTRL Value Display (54h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	1	0	0	54
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0	
Description	This command returns ambient light and brightness control values. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit) 1 = On												
Restriction	-												

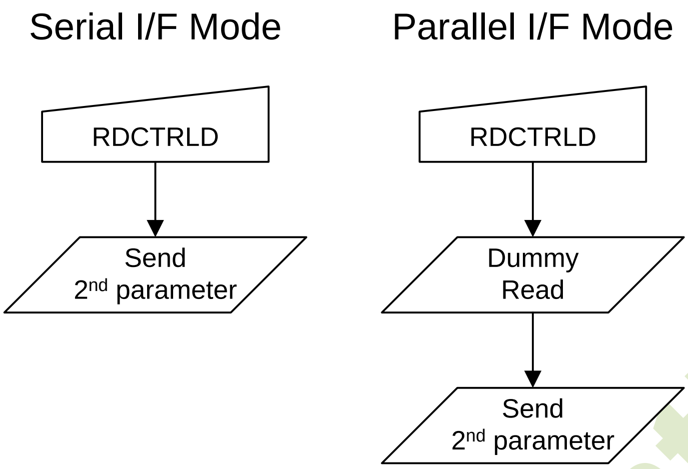
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	


Serial I/F Mode
RDCTRLD
Send
2nd parameter
Parallel I/F Mode
RDCTRLD
Dummy
Read
Send
2nd parameter

9.2.45. WRCABC: Write Content Adaptive Brightness Control (55h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	1	0	1	55
1st Parameter	1	↑	1	-	0	0	0	0	0	0	CABC[1:0]		

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "10.7 Content Adaptive Brightness Control (CABC)".

CABC[1:0]		Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

Restriction

-

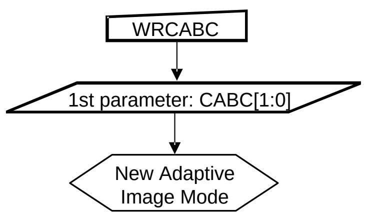
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



9.2.46. RDCABC: Read Content Adaptive Brightness Control (56h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	0	1	1	0	56
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	0	0	0	0	0	0	CABC[1:0]		

Description

This command is used to set parameters for image content based adaptive brightness control functionality.
There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "10.7 Content Adaptive Brightness Control (CABC)".

CABC[1:0]		Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

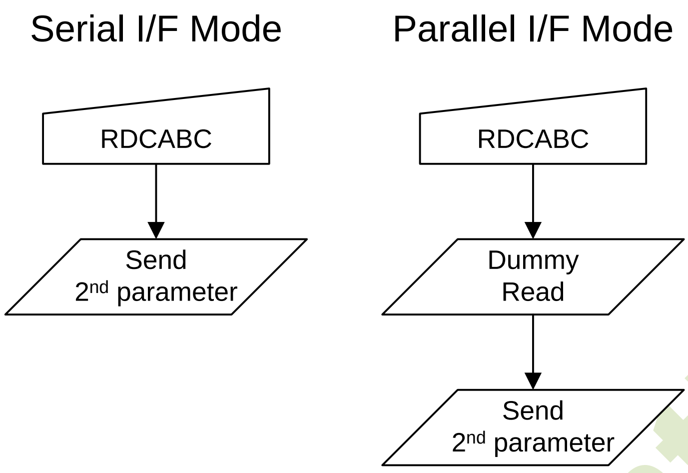
Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	Serial I/F Mode RDCABC Send 2nd parameter Parallel I/F Mode RDCABC Dummy Read Send 2nd parameter

9.2.47. WRCABCMB: Write CABC Minimum Brightness (5Eh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	1	1	1	0	5E
1st Parameter	1	↑	1	-	CMB[7:0]								

Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.
Restriction	-

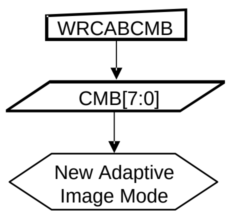
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



9.2.48. RDCABCMB: Read CABC Minimum Brightness (5Fh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	0	1	1	1	1	1	5F
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	CMB[7:0]								

Description

This command returns the minimum brightness value of CABC function.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

Restriction

-

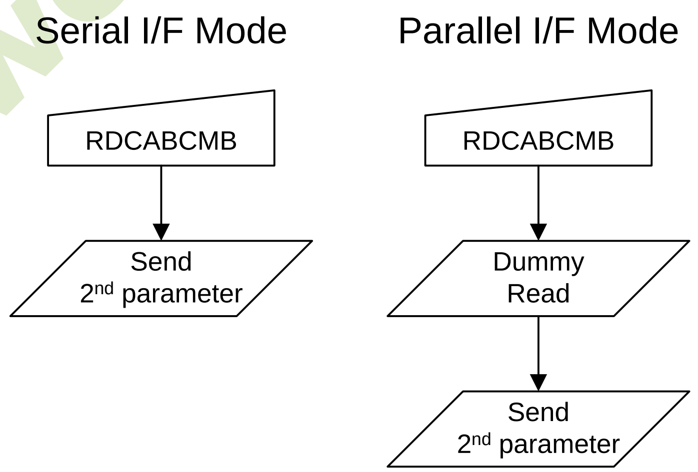
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



9.2.49. RDABCSD: Read Automatic Brightness Control Self-Diagnostic Result (68h)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	1	1	0	1	0	0	0	68
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	D7	D6	0	0	0	0	0	0	

Description

This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out -command as described in the table below:

D7 – Register Loading Detection

D6 – Functionality Detection

D5, D4, D3, D2, D1 and D0 are for future use and are set to '0'.

Restriction

-

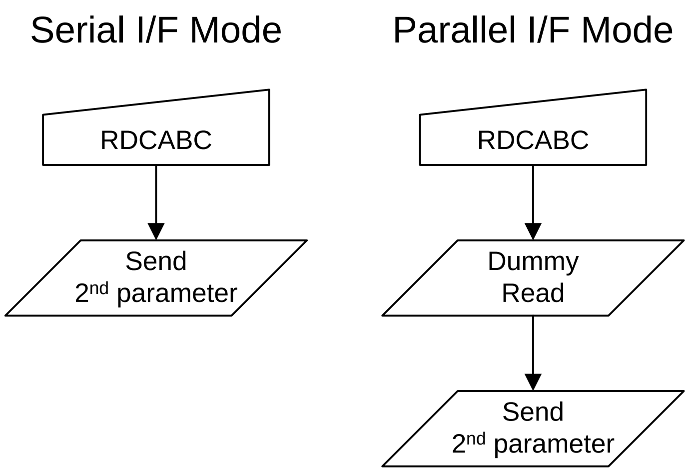
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



9.2.50. RDID1: Read ID1 (DAh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	0	1	0	DA
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	module's manufacture[7:0]								
Description	This read byte identifies the LCD module's manufacturer.												
Restriction	-												

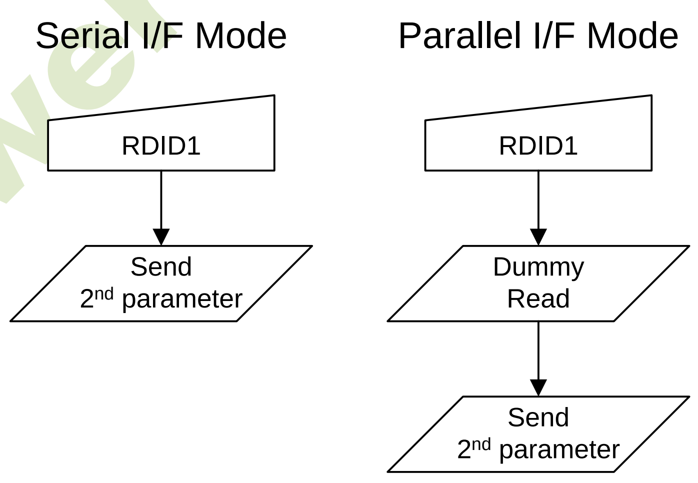
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	98h
SW Reset	98h
HW Reset	98h

Flow Chart



9.2.51. RDID2: Read ID2 (DBh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	0	1	1	DB
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	LCD module/driver version[7:0]								
Description	This read byte is used to track the LCD module/driver version.												
Restriction	-												

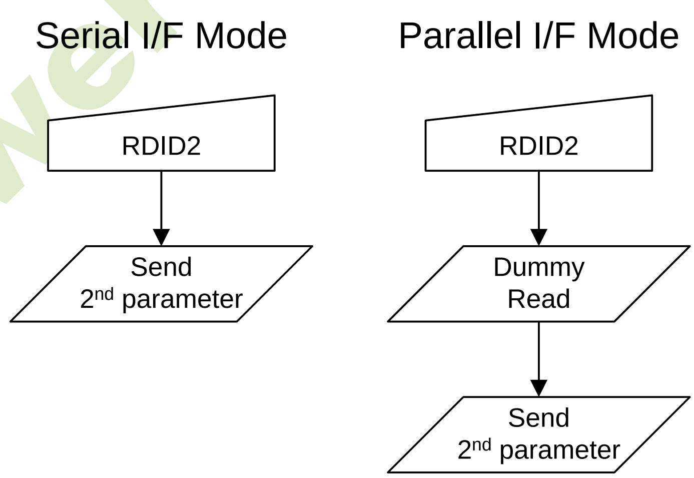
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	51h
SW Reset	51h
HW Reset	51h

Flow Chart



9.2.52. RDID3: Read ID3 (DCh)

CMD/Pas	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	1	0	0	DC
1st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	LCD module/driver ID[7:0]								
Description	This read byte identifies the LCD module/driver.												
Restriction	-												

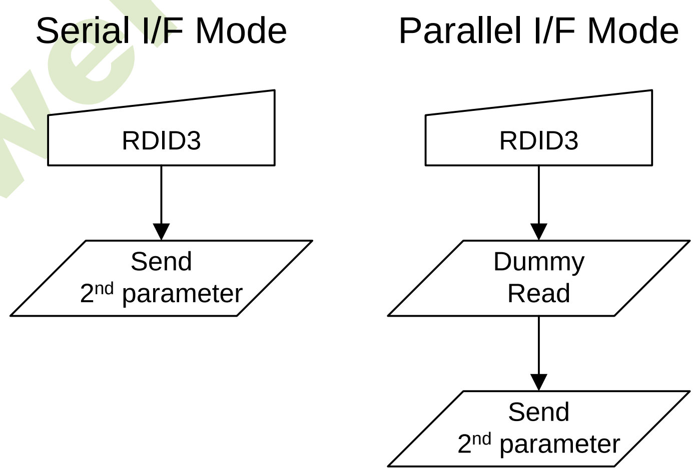
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



9.3. Uesr Command

TBD

10. Electrical Characteristics

10.1. Absolute maximum ratings

Symbol	Parameter	Unit	Value	Note
IOVCC	Interface Supply Voltage	V	-0.3 to +3.3	Note(3),(4)
VCI	Logic Supply Voltage	V	-0.3 to +3.3	Note(3),(5)
AVDD	Positive Voltage input	V	-0.3 to +6.5	Note(6)
AVEE	Negative Voltage input	V	0 to -5.2	Note(7)
VGH	Power Supply Voltage	V	-0.3 to +16	Note(8)
VGL	Power Supply Voltage	V	0 to -12	Note(9)
Top	Operating Temperature	°C	-40 to +85	Note(10)
Tstg	Storage Temperature	°C	-55 to +110	Note(11)

Table 10.1 Absolute maximum ratings

Note: (1) Permanent device damage may occur if absolute maximum conditions are exceeded.
(2) Functional operation should be restricted to the conditions described under DC Characteristics.
(3) IOVCC, VSSD must be maintained.
(4) To make sure IOVCC ≥ VSSD.
(5) To make sure VCI≥ AVSS.
(6) To make sure AVDD ≥ AVSS
(7) To make sure AVSS ≥ VSN
(8). To make sure VGH ≥ AVSS
(9) To make sure AVSS ≥ VGL (VGH +|VGL| < 30V)
(10) For die and wafer products, specified up to +85℃
(11) This temperature specifications apply to the TCP package.

10.2. DC Characteristics

(T_A=-40 ~ 85 °C, VCI=2.6 ~ 3.3V, IOVCC=1.65~3.3V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
IOVCC	V_{IN}	Interface Supply Voltage	1.65	-	3.3	V
VCI	V_{IN}	Analog Supply Voltage	2.6	-	3.3	V
Input high voltage	V_{IH}	IOVCC= 1.65 ~ 3.3V VCI= 2.6 ~ 3.3V	0.7 $_{IOVCC}$	-	IOVCC	V
Input low voltage	V_{IL}		0	-	0.3 $_{IOVCC}$	V
VPP	V_{IH} V_{IL}	VPP	8.0V	8.25V	8.5V	V
Output high voltage (SDO, LEDPWM)	V_{OH1}	I_{OH} = -1.0 mA	0.8 $_{IOVCC}$	-	IOVCC	V
Output low voltage (SDO, LEDPWM)	V_{OL1}	IOVCC= 1.65 ~ 2.4V I_{OL} = 1.0 mA	0	-	0.2 $_{IOVCC}$	V
Logic High level input current	I_{IH}	VSYNC, HSYNC	-	-	1	µA
		RESX, DCX_SCL, CSX, RDX, WRX_SCL	-	-	1	µA
	I_{IHD}	DB[17…0], SDI, DCX	-	-	1	µA
		DB[17…0]	-	-	1	µA
Logic Low level input current	I_{IL}	VSYNC, HSYNC	-1	-		µA
		RESX, DCX, CSX, RDX, WRX_SCL	-1	-		µA
	I_{ILD}	DB[17…0], SDI, DCX	-1	-		µA
		DB[17…0]	-1	-		µA
Current consumption Sleep In mode	I_{IOVCC}	VCI=2.8V, IOVCC=1.8V T_A =25°C	-	TBD	-	µA
	I_{VCI}		-	TBD	-	µA

10.3. AC Characteristics

10.3.1. 8080 Series Parallel 18/16/9/8-bit Interface Characteristics

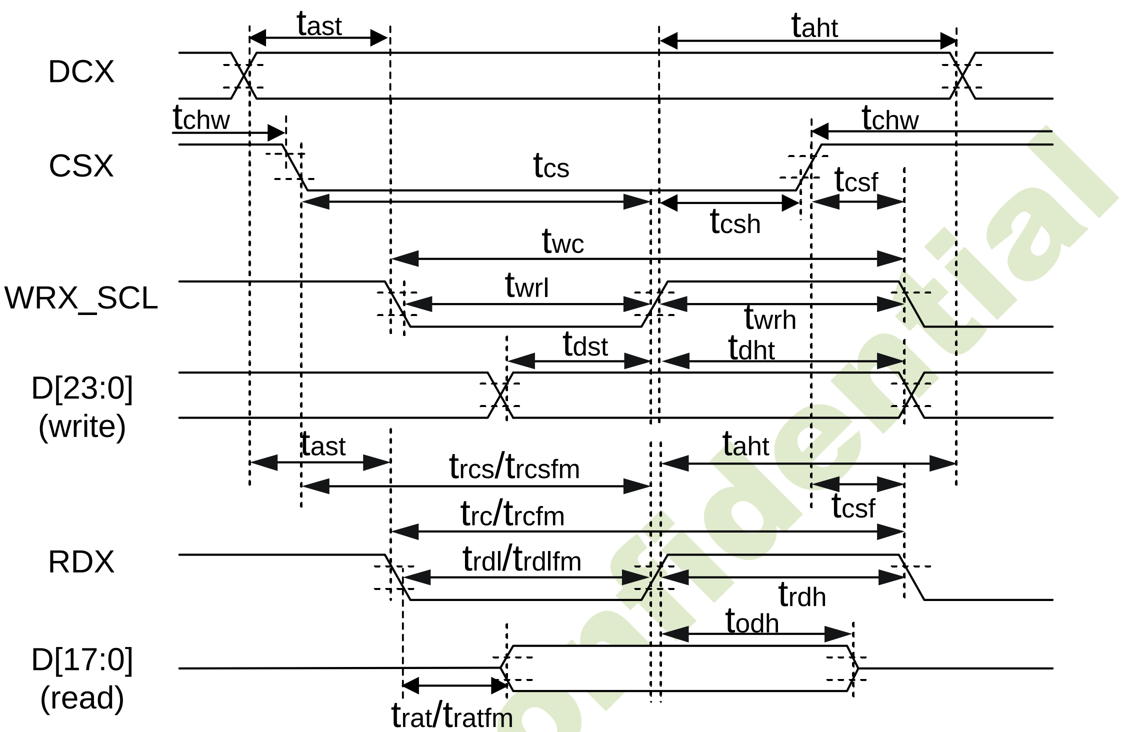


Figure. 10.1 8080 Series Parallel interface Timing Characteristics

(T_A=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (write/read)	10	-	ns	
CSX	tchw	CSX “H” Pulse Width	0		ns	
	tcs	Chip select setup time (write)	15		ns	
	trcs	Chip select setup time (read ID)	45		ns	
	trcsfm	Chip Select setup time (read FM)	355		ns	
	tcsf	Chip select wait time (write/read)	10		ns	
	tcsh	Chip select hold time	10		ns	
WRX	twc	Write cycle	66		ns	
	twrh	Control pulse “H” duration	15		ns	
	twrl	Control pulse “L” duration	15		ns	
RDX(ID)	trc	Read cycle (ID)	160		ns	
	trdh	Control pulse “H” duration (ID)	90		ns	
	trdl	Control pulse “L” duration (ID)	45		ns	
RDX(FM)	trcfm	Read cycle (FM)	450		ns	
	trdhfm	Control pulse “H” duration (FM)	90		ns	
	trdlfm	Control pulse “L” duration (FM)	355		ns	
D[17:0]	Tdst	Data setup time	10		ns	
	tdht	Data hold time	10		ns	
	trat	Read access time (ID)		42	ns	
	tratfm	Read access time (FM)		340	ns	
	todh	Output disable time	20	80	ns	

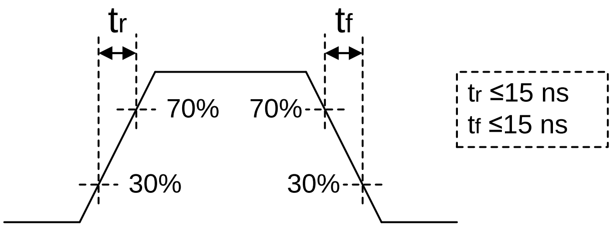


Figure. 10.2 Input rise and fall times

10.3.2. Serial Interface Timing Characteristics (3-line SPI)

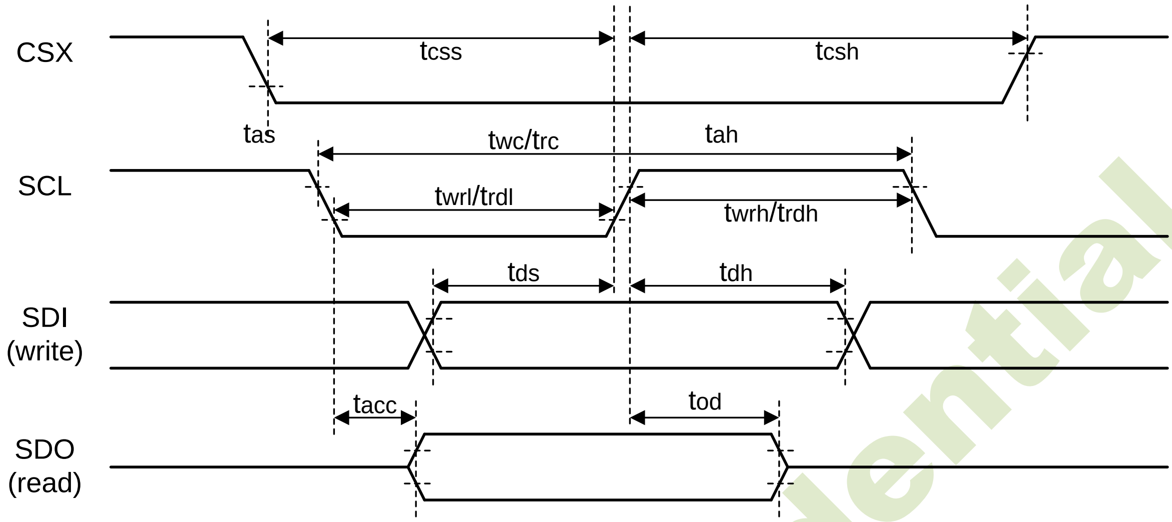


Figure. 10.3 3-line Serial Interface Timing Characteristics

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	tcss	Chip select setup time (Write)	15		ns	
	tcsh	Chip select setup time (Read)	60		ns	
SCL (write)	twc	Write cycle	16		ns	
	twrh	Control pulse "H" duration	7		ns	
	twrl	Control pulse "L" duration	7		ns	
SCL (read)	trc	Read cycle	150		ns	
	trdh	Control pulse "H" duration	60		ns	
	trdl	Control pulse "L" duration	60		ns	
SDI/SDO (write)	tds	Data setup time	7		ns	
	tdt	Data hold time	7		ns	
SDI/SDO (read)	tracc	Read access time	10	50	ns	
	tod	Output disable time	15	50	ns	

10.3.3. Serial Interface Timing Characteristics (4-line SPI)

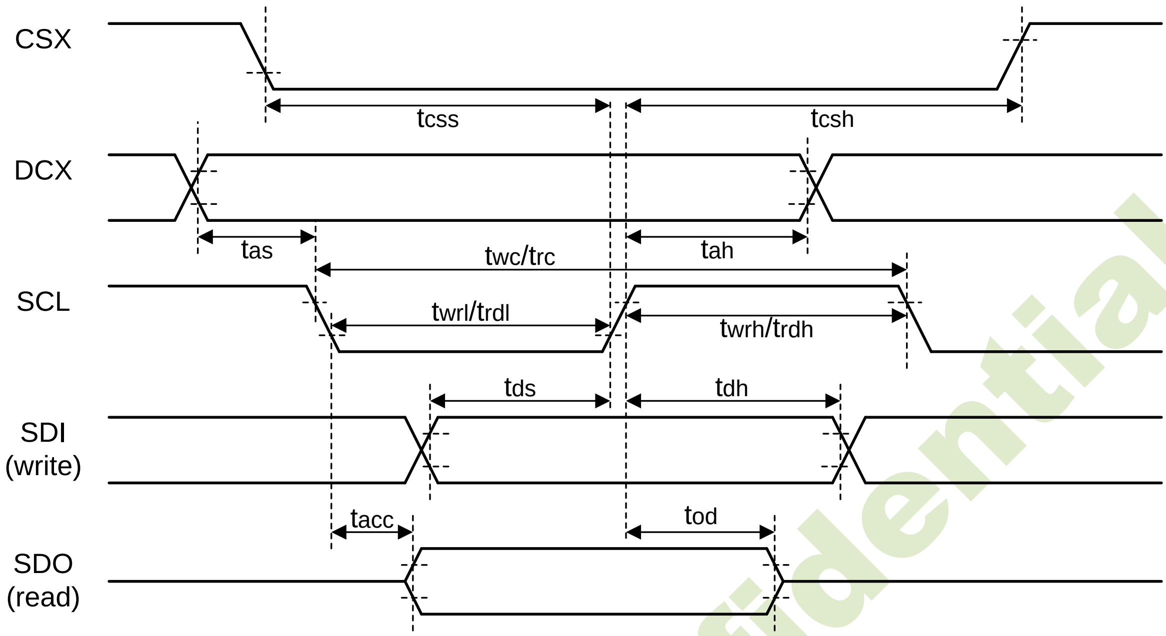


Figure. 10.4 4-line Serial Interface Timing Characteristics

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	tcss	Chip select setup time (Write)	15		ns	
	tcsh	Chip select setup time (Read)	60		ns	
DCX	tas	Address setup time	10		ns	
	tah	Address hold time (Write/Read)	10		ns	
WRX (write)	twc	Write cycle	16		ns	
	twrh	Control pulse "H" duration	7		ns	
	twrl	Control pulse "L" duration	7		ns	
WRX (read)	trc	Read cycle	150		ns	
	trdh	Control pulse "H" duration	60		ns	
	trdl	Control pulse "L" duration	60		ns	
SDI/SDO (write)	tds	Data setup time	7		ns	
	tdt	Data hold time	7		ns	
SDI/SDO (read)	tracc	Read access time	-	50	ns	
	tod	Output disable time	15	50	ns	

10.3.4. Reset Input Timing

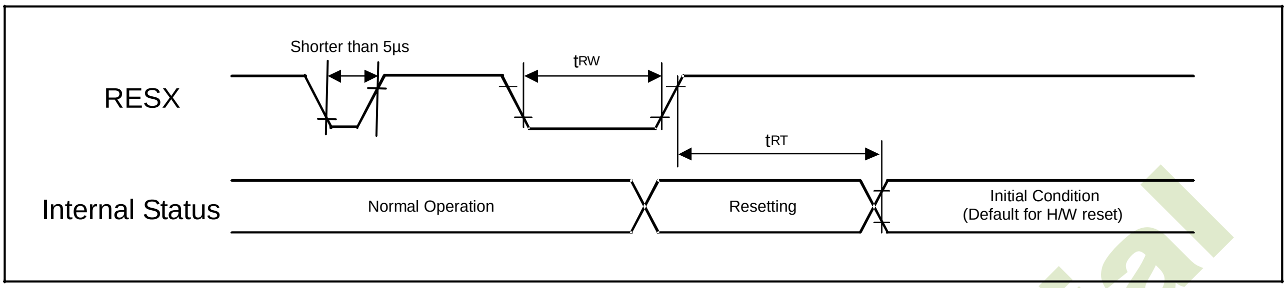


Figure. 10.5 Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	10	-	µs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

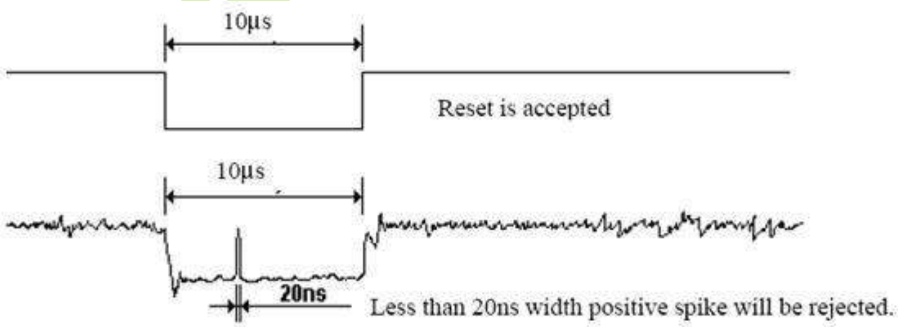
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

10.3.5. DSI D-PHY electronic characteristics

The Description of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: Low-Power Receiver (LP-RX), High-Speed Receiver (HS-RX), the Low-Power Contention Detector (LP-CD), and Low Power Transmitter (LP-TX). Figure 10.6 shows the complete set of electronic functions required for a fully featured PHY transceiver.

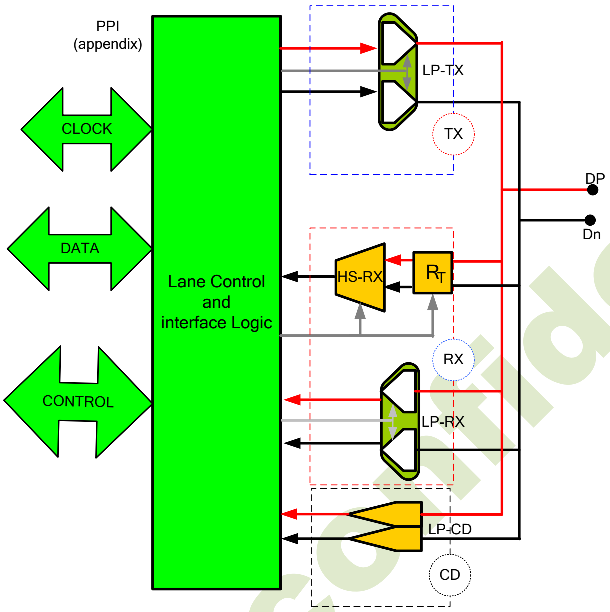


Figure. 10.6 Electronic functions of a D-PHY transceiver

Figure 10.7 shows both the HS and LP signal levels of electronic characteristics, respectively. Where, the HS receiver utilizes low-voltage swing differential signaling. The LP transmitter and LP receiver utilize low-voltage swing single signaling. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

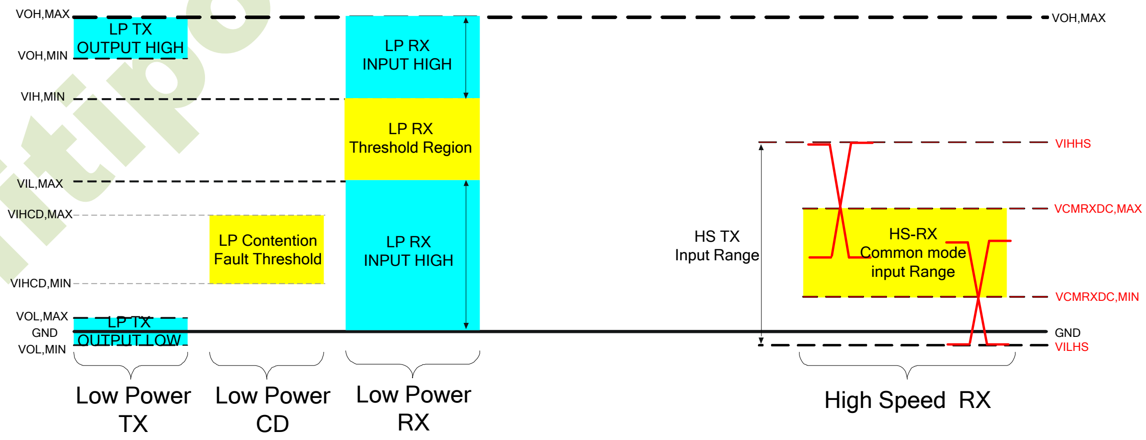


Figure. 10.7 HS and LP signal levels

The Electronic Characteristics of Low-Power Transmitter (TX)

The Low-Power TX shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power modes. Hence, it is important to keep static power consumption of a LP TX be as low as possible. Under tables list DC and AC characteristic for Low power transmitter.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
V_{OL}	Thevenin output low level	-50	-	50	mV	
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1)Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 10.2 LP-TX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
$T_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock	90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST- 700)	-	-	mV/ns	(1),(8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
C_{LOAD}	Load capacitance	-	-	70	pF	-

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

(2) When the output voltage is between 400 mV and 930 mV.

(3) Measured as average across any 50 mV segment of the output signal transition.

(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.

(5) This value represents a corner point in a piecewise linear curve.

(6) When the output voltage is in the range specified by VPIN(absmax).

(7) When the output voltage is between 400 mV and 700 mV.

(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.

(9) When the output voltage is between 700 mV and 930 mV.

Table 10.3 LP-TX AC Specifications

The Electronic Characteristics of Receiver (RX)

This part includes two parts which Low-Power RX and High-Speed RX. Because they have differential DC and AC characteristic, first to describe LP-RX then describe HS-RX.

Low-Power Receiver (RX)

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The Figure 11.8 shows Input Glitch Rejection of Low-Power RX. In addition, under tables list DC and AC characteristic for LP-RX

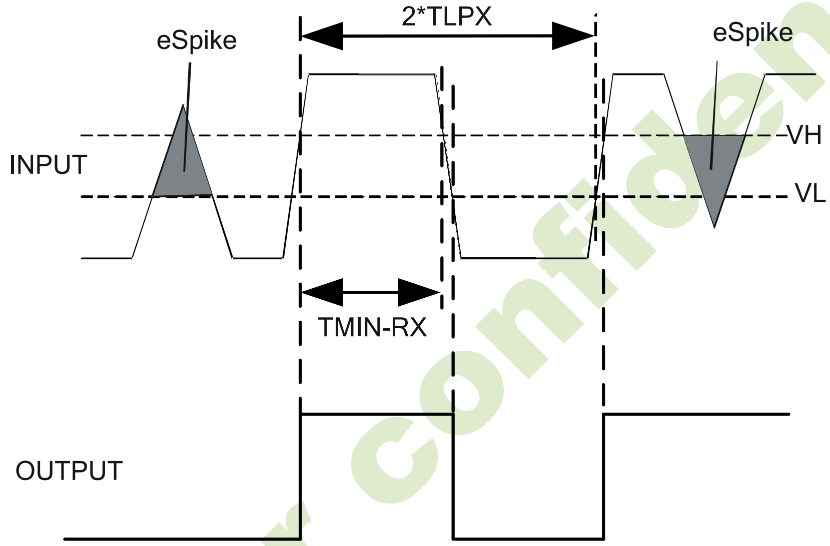


Figure. 10.8 Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IH}	Logic 1 input threshold	880	-	-	mV	-
V_{IL}	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

Table 10.4 LP-RX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state

(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

(4) An input pulse greater than this shall toggle the output.

Table 10.5 LP-RX AC Specifications

Line Contention Detection

Contention can be inferred by following conditions:

1. Detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than VIL.
2. Detect an LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VIHCD.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

Table 10.6 Contention Detector DC Specifications

High-Speed Receiver (RX)

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 10.7 HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV_{PP}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 10.8 HS Receiver AC Specifications

High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 11.9.

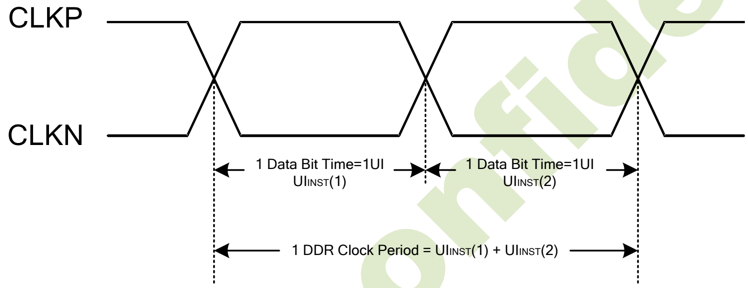


Figure. 10.9 DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications f
or the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	1.82	-	-	ns	(1), (2)

Note: (1) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

(2) Maximum total bit rate is 550Mbps/per lane @ 2 data lane 24-bit data format.

Table 10.9 Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 11.6 Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget. Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

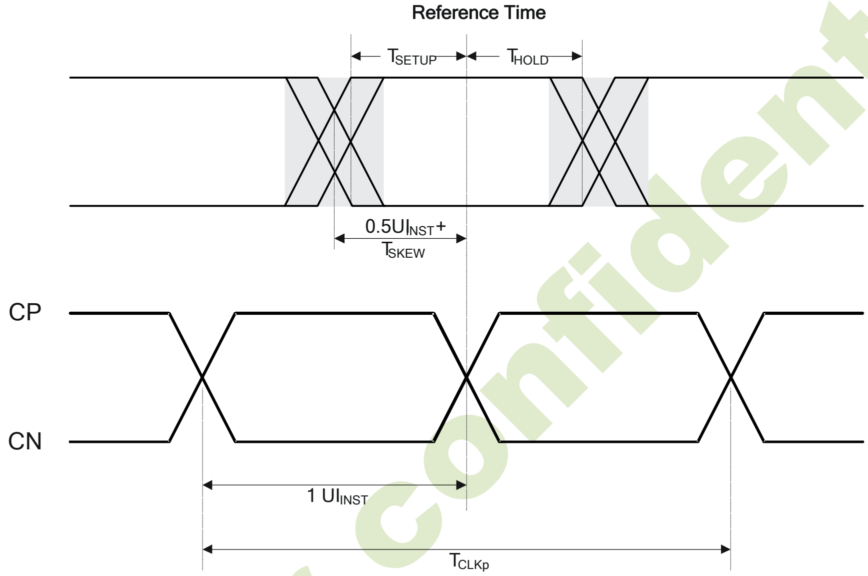


Figure. 10.10 Data to Clock Timing Definitions

Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 11.16. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 11.12 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave 0.4*UI_{INST}, i.e. ±0.2*UI_{INST} for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST

Table 10.10 Data to Clock Timing Specifications

10.3.6. Timings for DSI Video mode

Vertical Timings

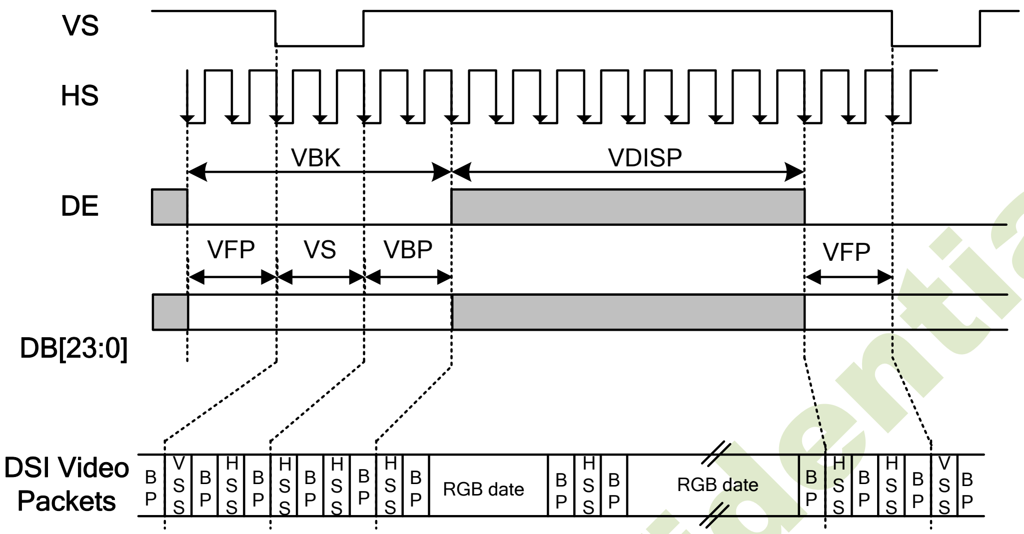


Figure. 10.11 Vertical Timings for DSI Video mode I/F

Resolution=240x320 (TA=25°C, IOVCC=1.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	320	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Figure. 10.12 Vertical Timings for DSI Video mode I/F

Horizontal Timings

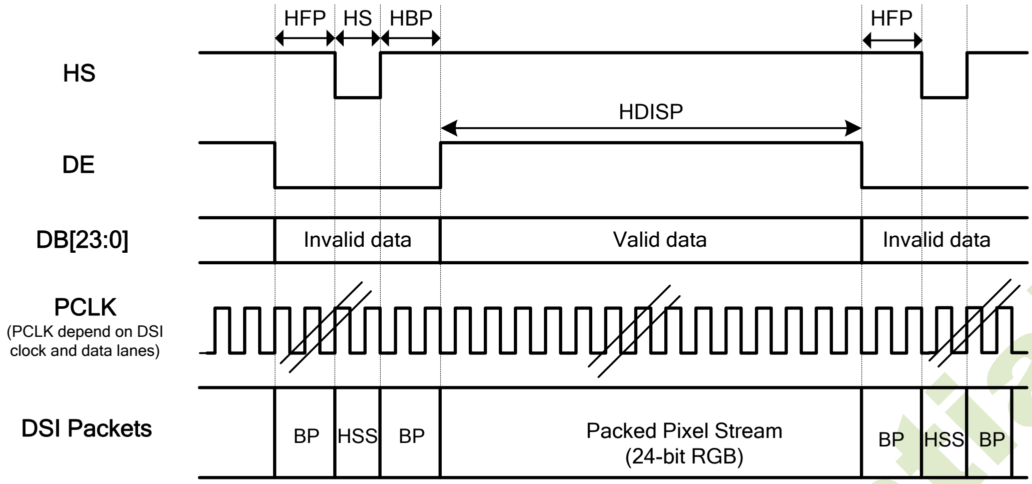


Figure. 10.13 Horizontal Timing for DSI Video mode I/F

Resolution=240x320 (TA=25°C, IOVCC=1.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	-	88	DCK
Horizontal active area	HDISP	-	-	240	-	DCK

Note: (1) HS+HBP>0.5uS.

(2) HFP>0.5uS.

Table 10.11 Horizontal Timings for DSI Video mode I/F