DATA SHEET

SBN0064G

Dot-matrix STN LCD 64-SEGMENT Driver with 64-row x 64-column Display Data Memory

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1 GENERAL

1.1 Description

The SBN0064G is a 64-SEGMENT driver with 64-row x64 column (4096-bit) on-chip Display Data Memory. It is designed to be paired with the SBN6400G 64-COMMON driver to drive a STN LCD panel.

The on-chip Display Data Memory is for storing display data. Dot-matrix mapping method is used. A “0” stored in the Display Data Memory bit corresponds to an OFF-pixel on the LCD panel; a “1” stored in the Display Data Memory bit corresponds to an ON-pixel on the LCD panel.

Display on the LCD panel is controlled by a host microcontroller. The interface between the host microcontroller and the SBN0064G is composed of 8-bit, bi-directional data bus (DB0~DB7) and control signals R/$\overline{W}$, E, and $\overline{C}$/D.

The SBN0064G does not have oscillator circuit. It depends on the SBN6400G to supply clocks (CLK1, CLK2) and display control signals (CL, M, FRM).

1.2 Features

- 64-SEGMENT STN LCD driver.
- To be paired with the SBN6400G 64-COMMON Driver.
- On-chip Display Data Memory: 64-row x 64-column (totally 4096 bits).
- Dot-Matrix Mapping between the Display Data Memory bit and LCD pixel.
- External LCD bias.
- Display duty cycle: 1/32 ~1/64.
- Normal mapping or Inverted mapping between SEGMENT outputs and Display Data Memory column outputs.
- Easy interface with a 8-bit host microcontroller.
- 8-bit parallel data bus; READ/WRITE, Enable, and Command/Data control bus.
- Programmable internal registers: Display ON/OFF, Display Start Line, Page Address, Column Address, and Status.
- Display Data WRITE and display data READ.
- Operating voltage range (V_{DD}): 2.7 ~ 5.5 volts.
- LCD bias voltage (V_{LCD}=V_{DD} - V5): 13 volts (max).
- Negative power supply (V_{NEG}=V_{DD}-V_{EE}): 16 volts (max).
- Operating temperature range: -20 to +75 °C.
- Storage temperature range: -55 to +125 °C.

1.3 Ordering information

Table 1 Ordering information

PRODUCT TYPE	DESCRIPTION
SBN0064G-LQFPG	LQFP100 Pb-free package.
SBN0064G-QFPG	QFP100 Pb-free package.
SBN0064G-LQFP	LQFP100 general package.
SBN0064G-QFP	QFP100 general package.
SBN0064G-D	tested die.

2 FUNCTIONAL BLOCK DIAGRAM AND DESCRIPTION

2.1 Functional block diagram

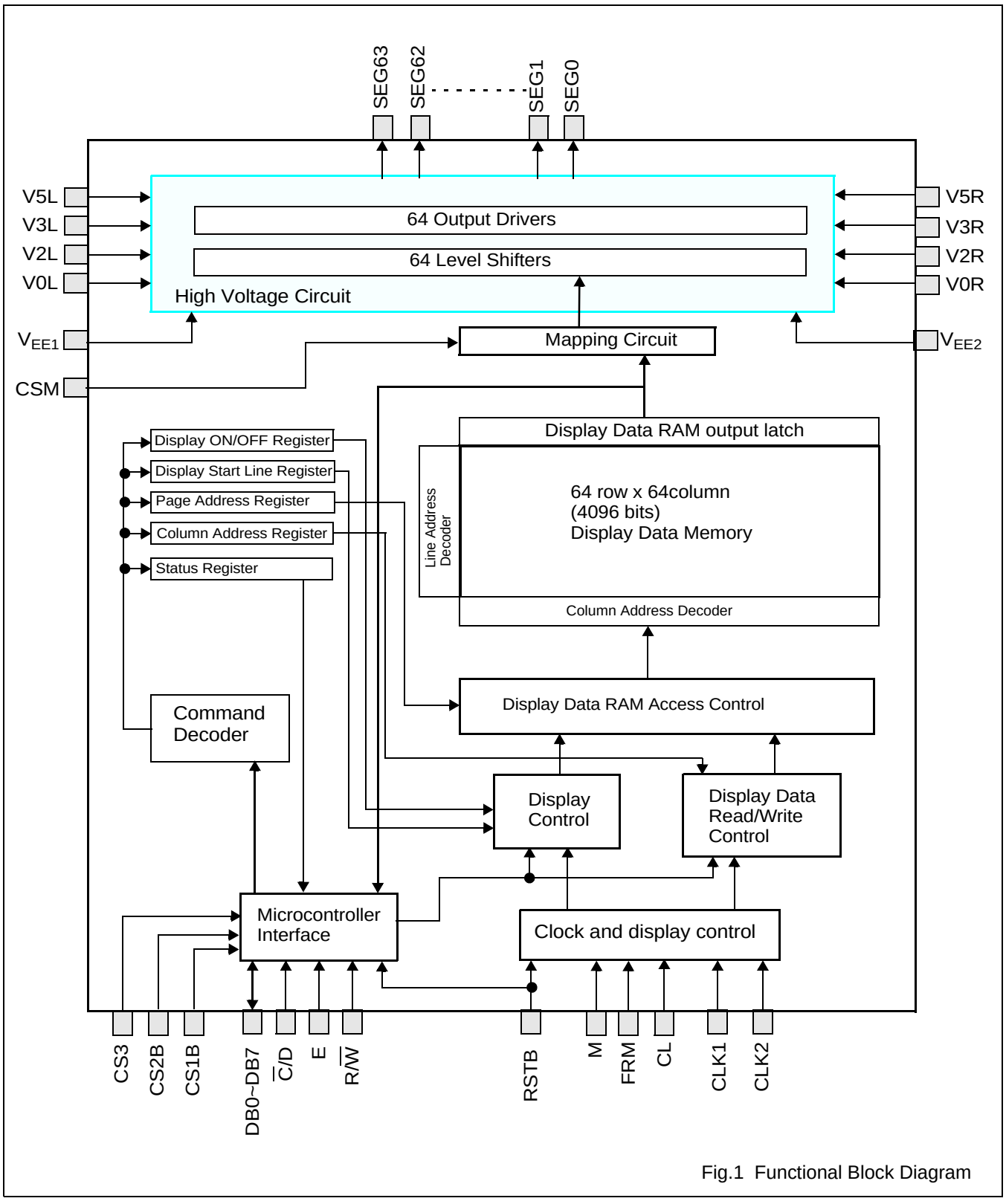


Fig.1 Functional Block Diagram

3 PIN(PAD) ASSIGNMENT, PAD COORDINATES, SIGNAL DESCRIPTION

3.1 The SBN0064G pinning diagram (LQFP100)

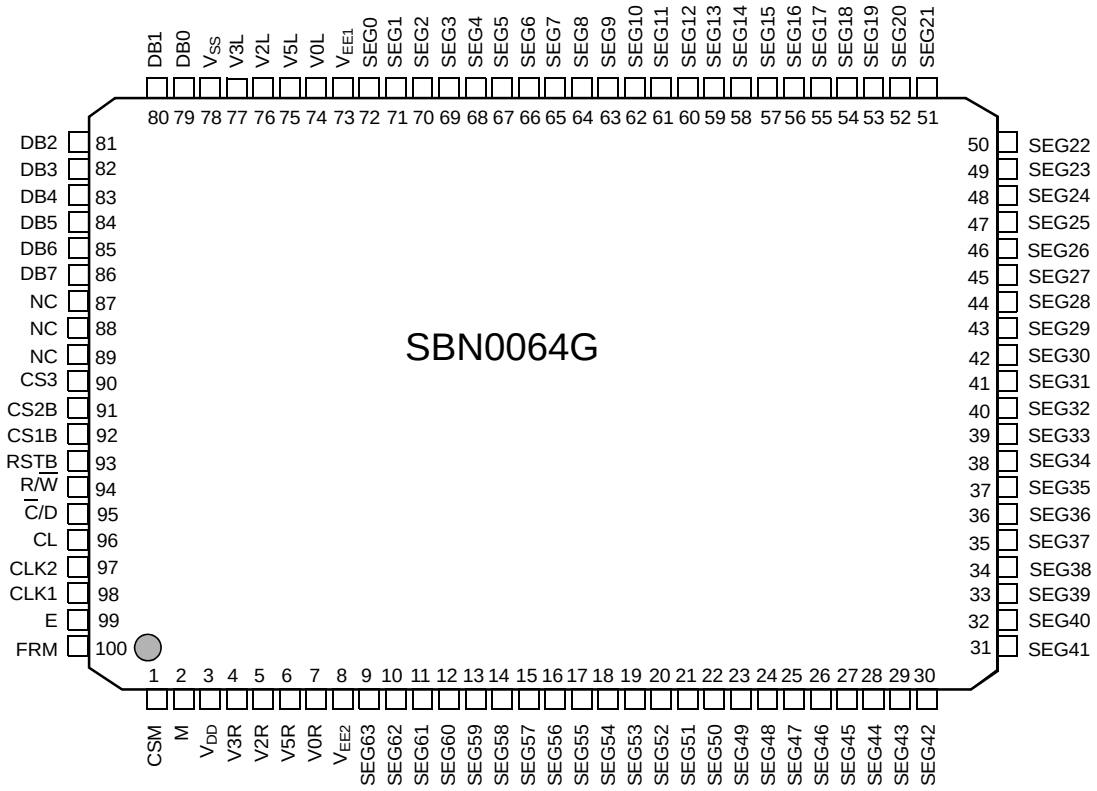
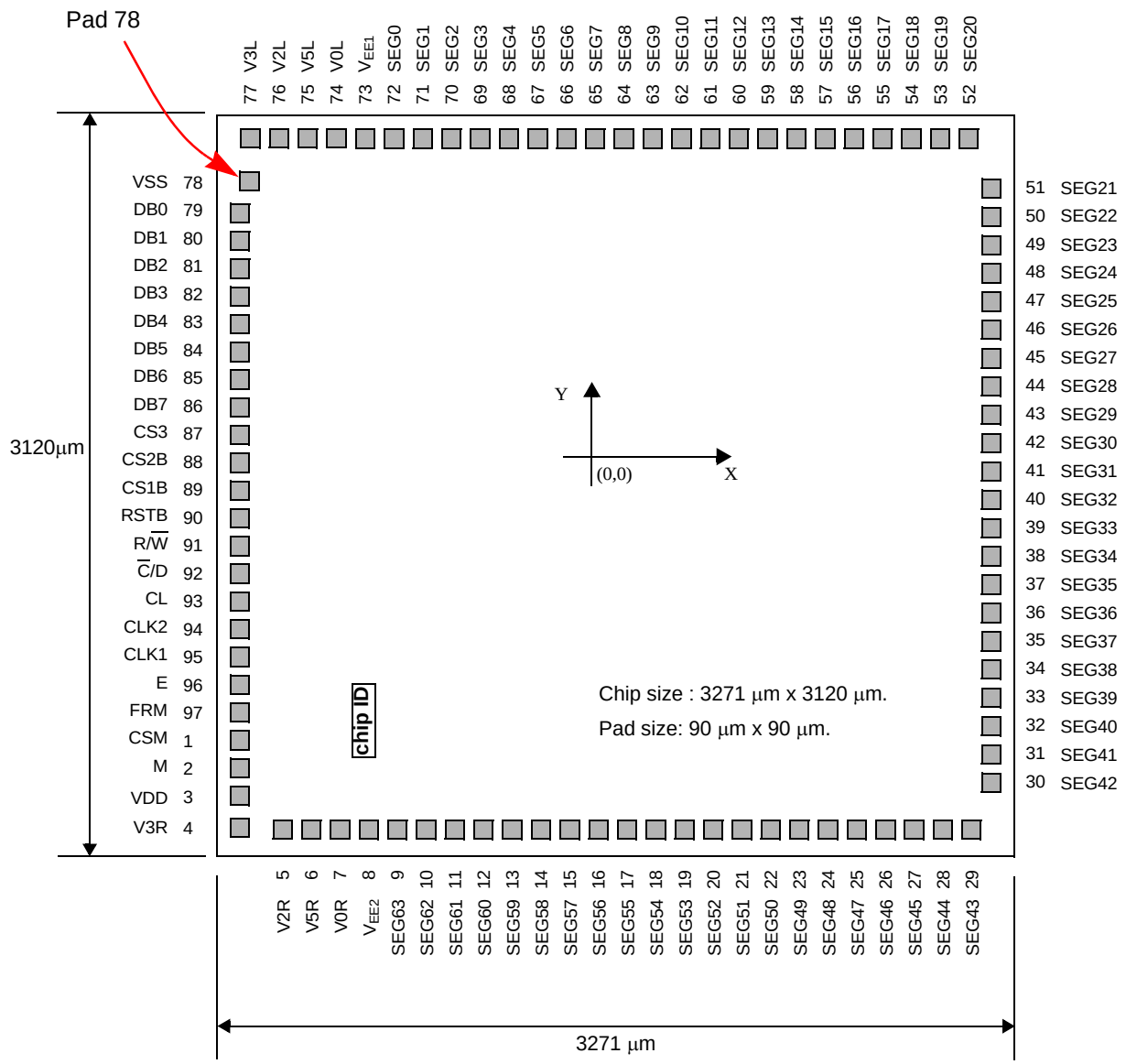


Fig.2 Pin assignment of LQFP100 package.

3.2 The SBN0064G pad placement



Note:

(1) The total pad number is 97.

(2) The chip ID is located at the lower left part of the chip.

(3) The chip ID of is 18005.

(4) The die origin is at the center of the chip.

(5) For chip_on_board bonding, **chip carrier** should be connected to VDD or left open. **Chip carrier** is the metal pad to which the die is attached.

Fig.3 The pad placement

3.3 Pad coordinates

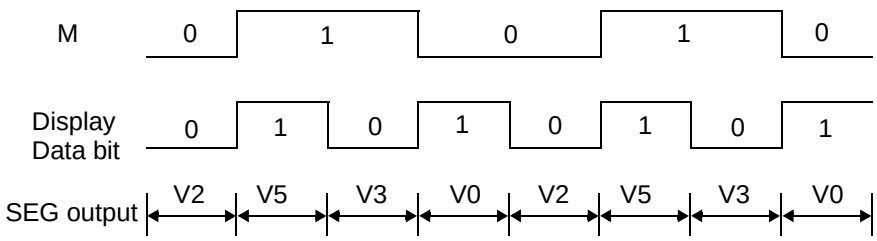
Table 2 The pad coordinates (unit: μm)

PAD NO.	PAD NAME	X	Y
1	CSM	-1506	-1066
2	M	-1506	-1181
3	VDD	-1512	-1300
4	V3R	-1512	-1430
5	V2R	-1338	-1434
6	V5R	-1223	-1434
7	V0R	-1108	-1434
8	VEE2	-993	-1434
9	SEG63	-878	-1434
10	SEG62	-763	-1434
11	SEG61	-648	-1434
12	SEG60	-533	-1434
13	SEG59	-418	-1434
14	SEG58	-303	-1434
15	SEG57	-188	-1434
16	SEG56	-73	-1434
17	SEG55	42	-1434
18	SEG54	157	-1434
19	SEG53	272	-1434
20	SEG52	387	-1434
21	SEG51	502	-1434
22	SEG50	617	-1434
23	SEG49	732	-1434
24	SEG48	847	-1434
25	SEG47	962	-1434
26	SEG46	1077	-1434
27	SEG45	1192	-1434
28	SEG44	1307	-1434
29	SEG43	1422	-1434
30	SEG42	1512	-1194
31	SEG41	1512	-1079
32	SEG40	1512	-964
33	SEG39	1512	-849
34	SEG38	1512	-734
35	SEG37	1512	-619
36	SEG36	1512	-504
37	SEG35	1512	-389
38	SEG34	1512	-274
39	SEG33	1512	-159
40	SEG32	1512	-44
41	SEG31	1512	71
42	SEG30	1512	186
43	SEG29	1512	301
44	SEG28	1512	416
45	SEG27	1512	531
46	SEG26	1512	646
47	SEG25	1512	761
48	SEG24	1512	876
49	SEG23	1512	991
50	SEG22	1512	1106
51	SEG21	1512	1221
52	SEG20	1407	1434
53	SEG19	1292	1434
54	SEG18	1177	1434
55	SEG17	1062	1434
56	SEG16	947	1434
57	SEG15	832	1434
58	SEG14	716	1434
59	SEG13	602	1434
60	SEG12	486	1434
61	SEG11	372	1434
62	SEG10	257	1434
63	SEG9	142	1434
64	SEG8	27	1434
65	SEG7	-88	1434
66	SEG6	-203	1434
67	SEG5	-318	1434
68	SEG4	-433	1434
69	SEG3	-548	1434
70	SEG2	-663	1434
71	SEG1	-778	1434
72	SEG0	-893	1434
73	VEE1	-1008	1434
74	V0L	-1124	1434
75	V5L	-1239	1434
76	V2L	-1355	1434
77	V3L	-1471	1434
78	VSS	-1471	1248
79	DB0	-1506	1119
80	DB1	-1506	1004
81	DB2	-1506	889
82	DB3	-1506	774
83	DB4	-1506	659
84	DB5	-1506	544
85	DB6	-1506	429
86	DB7	-1506	314
87	CS3	-1506	199
88	CS2B	-1506	84
89	CS1B	-1506	-31
90	RSTB	-1506	-146
91	R/$\overline{W}$	-1506	-261
92	$\overline{C}$/D	-1506	-376
93	CL	-1506	-491
94	CLK2	-1506	-606
95	CLK1	-1506	-721
96	E	-1506	-836
97	FRM	-1506	-951

3.4 Signal description

Table 3 Pad signal description

To avoid a latch-up effect at power-on: V_{SS} – 0.5 V < voltage at any pin at any time < V_{DD} + 0.5 V .

Pad number	SYMBOL	I/O	DESCRIPTION
1	CSM	I	Column/Segment Mapping. This signal controls the mapping relation between the column output of the Display Data Memory and the SBN0064G's segment output. If CMS=1, the mapping is called *Normal Mapping*. The mapping relation is that Columns 0, 1, 2,...,62,63 of the Display Data Memory are mapped to Segments 0, 1, 2,..., 62, 63 of segment driver outputs. If CMS=0, the mapping is called *Inverted Mapping*. The mapping relation is that Columns 0, 1, 2,...,62,63 of the Display Data Memory are mapped to Segments 63, 62, 61,..., 2, 1, 0 of segment driver outputs.
2	M	Input	AC frame input. The AC frame signal is the AC signal for generating alternating bias voltage of reverse polarities for LCD cells. This signal is supplied by the SBN6400G.
3	V_{DD}	Input	Power supply for logic part of the chip. The V_{DD} should be in the range from 2.7 volts to 5.5 volts.
4, 5, 6, 7	V3R, V2R, V5R, V0R	Input	External LCD Bias voltage. Note that V0R, V2R, V3R, and V5R must be connected to external bias voltages V_{DD}, V2, V3, and V5, respectively, and the condition $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must always be met. In addition, V_{LCD} (V_{DD} - V5) should not exceed 13 volts.
8	V_{EE2}	Input	Negative power supply for LCD bias. This pad should be connected to the V_{EE} of the external bias circuit.
9~72	SEG63~0	Output	SEGNENT driver outputs. The output voltage level of SEGMENT outputs are decided by the combination of the alternating frame signal (M) and display data. Depending on the value of the AC frame signal and the display data, a single voltage level is selected from V0, V2, V3, or V5 for SEGMENT driver, as shown in Fig. 4.  Fig.4 SEGMENT driver output voltage level
73	V_{EE1}	Input	Negative power supply for LCD bias. This pad should be connected to the V_{EE} of the external bias circuit.

Pad number	SYMBOL	I/O	DESCRIPTION
74, 75, 76, 77	V3L, V2L, V5L, V0L	Input	External LCD Bias voltage. Note that V0L, V2L, V3L, and V5L must be connected to external bias voltages V_{DD}, V2, V3, and V5, respectively, and the condition VDD≥V1≥V2≥V3≥V4≥V5 must always be met. In addition, V_{LCD} (V_{DD} - V5) should not exceed 13 volts.
78	V_{SS}		Ground.
79~86	DB0~DB7	I/O	Bi-direction, tri-state 8-bit parallel data bus for interface with a host microcontroller. This data bus is for data transfer between the host microcontroller and the SBN0064G.
87, 88, 89	CS3, CS2B, CS1B	Input	Chip Selection To enable selecting the SBN0064G as a peripheral device of the microcontroller, the condition CS3=1, CS2B=0, and CS1B=0 must be met.
90	RSTB	Input	Hardware reset input. A LOW pulse added to this input resets the internal circuit of the SBN0064G. The duration of the low pulse must be longer than 1 μS.
91	R/$\overline{W}$	Input	Read/Write (R/$\overline{W}$) control signal from the host microcontroller. This pin should be connected to the R/$\overline{W}$ output of the host microcontroller. A HIGH level on this pin indicates that the microcontroller intends to do a READ operation. A LOW level on this pin indicates that the microcontroller intends to do a WRITE operation.
92	$\overline{C}$/D	Input	COMMAND/DATA selection from the host microcontroller. When $\overline{C}$/D=0, the data on the 8-bit data bus (DB0~DB7) are either code data to be written to an internal register, or status from the internal Status Register. When $\overline{C}$/D=1, the data on the 8-bit data bus (DB0~DB7) are data to be written to or read from the Display Data Memory.
93	CL	Input	COMMON scan clock supplied by the SBN6400G. The time duration of a COMMON output is equal to one clock period of CL.
94, 95	CLK1, CLK2	Inputs	Two-phase clocks for the control logic. These two clocks are generated by the timing circuit of the SBN6400G COMMON Driver.
96	E	Input	Enable signal (E) from the host microcontroller.
97	FRM	Input	Frame signal from the SBN6400G, indicating the start of a new frame.

4 A SBN6400G AND SBN0064G-BASED DISPLAY SYSTEM

A SBN6400G and SBN0064G-based display system is shown in Fig. 5.

The SBN6400G contains timing generation circuit and 64 COMMON drivers. The timing generation circuit generates operating clocks and display control signals (frame signal FRM , COMMON scan signal CL, and AC frame signal M), for itself and the SBN0064G.

The SBN0064G contains 64 SEGMENT drivers, Display Data Memory, and interface circuit with a host microcontroller.

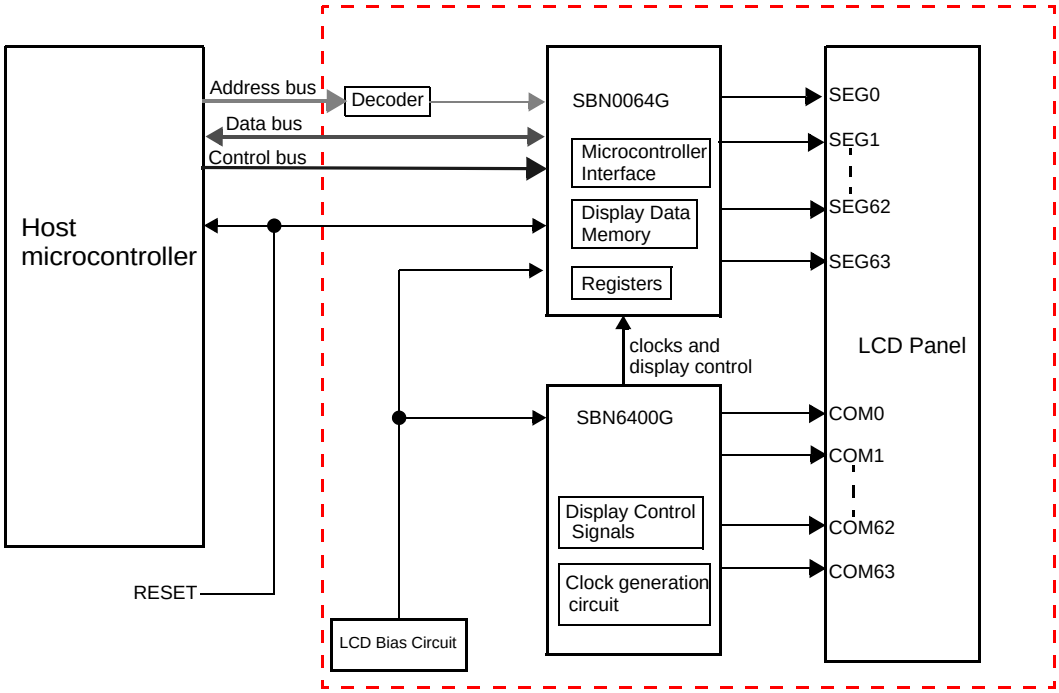


Fig.5 A SBN6400G and SBN0064G-based display system

5 INTERFACE WITH A HOST MICROCONTROLLER

5.1 Interface signals and operation

The interface signals between the host microcontroller and the SBN0064G are data bus and control bus. The data bus is an 8-bit (DB0~DB7) bi-directional bus. The control bus is composed of the following signals: $\overline{C}$/D, E, and R/$\overline{W}$.

By means of data bus and control bus, the host microcontroller can write data to or read data from the Display Data Memory, can program the internal registers, and can read status of the SBN0064G. It is the host microcontroller's responsibility to put proper data and timing on the data bus and control bus to ensure correct data transfer.

Fig. 6 gives an example for interface with an 8-bit microcontroller:

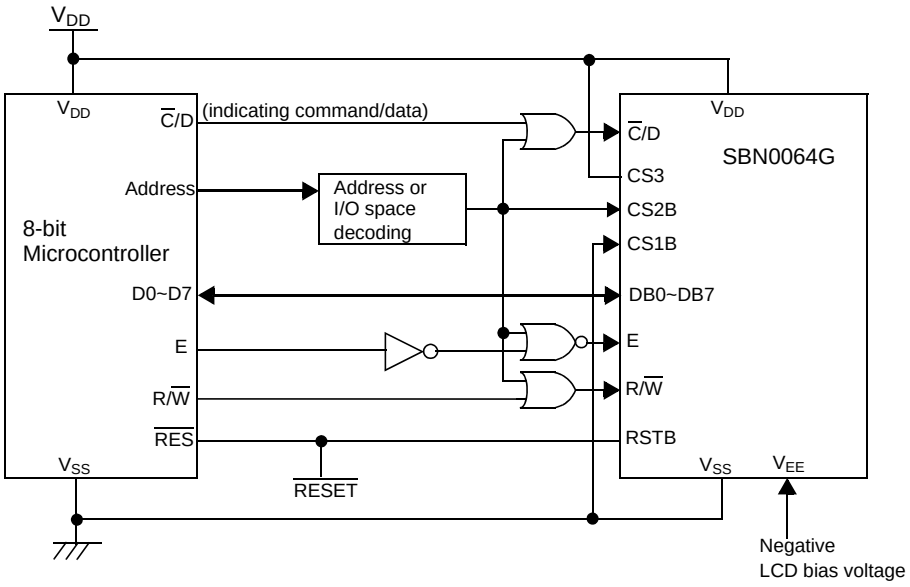


Fig.6 Interface example with an 8-bit microcontroller

Fig. 7 gives an example for interface with a 68-family microcontroller

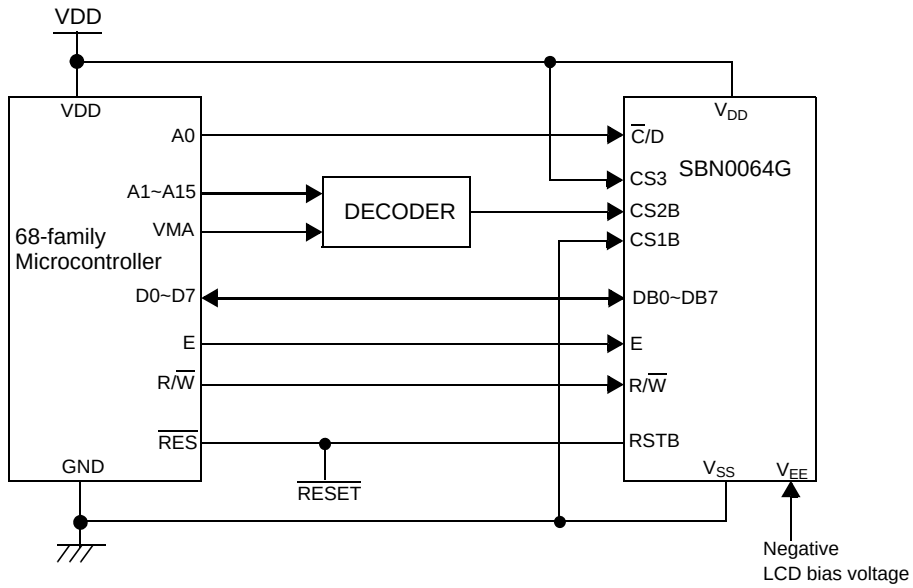


Fig.7 Interface with a 68-family microcontroller

Table 4 lists the setting for control bus and the types of data transfer.

Table 4 Interface signals and types of data transfer

$\overline{C}$/D	R/$\overline{W}$	Types of data transfer
1	1	The host microcontroller reads data from the Display Data Memory.
1	0	The host microcontroller writes data to the Display Data Memory
0	1	The host microcontroller reads the Status Register.
0	0	The host microcontroller programs an internal register.

5.2 Interface Timing (Writing to or reading from the SBN0064G)

Please refer to Fig. 16 and Fig. 17 for interface timing diagram and Table 25 and Table 26 for AC characteristics of interface timing.

6 DISPLAY DATA MEMORY AND LCD DISPLAY

The Display Data Memory is a static memory bit(cell) array of 64-row x 64-column. So, the total bit number is 64 x 64 = 4096 bits (512 bytes). Each bit of the memory is mapped to a single pixel (dot) on the LCD panel. A “1” stored in the Display Data Memory bit corresponds to an ON pixel (black dot in normal display). A “0” stored in the Display Data Memory bit corresponds to an OFF pixel (background dot in normal display).

Column outputs (Column 0~63) of the Display Data Memory is mapped to SEG 0~63 outputs of the SBN0064G. The mapping can be Normal Mapping or Inverse Mapping. Normal Mapping means that Column 0 is mapped to SEG0, Column 1 to SEG1, Column 2 to SEG2, and so on. Inverse Mapping means that Column 0 is mapped to SEG 63, Column 1 to SEG 62, Column 2 to SEG 61, and so on. The mapping relation is decided by the CSM input (Column/Segment Mapping). CSM=1 selects Normal Mapping and CSM=0 selects Inverse Mapping.

Any row (64 bits) of the Display Data Memory can be selected to map to the first row (COM0) of the LCD panel. This is decided by the Display Start Line Register. The Display Start Line Register points at a row of the Display Data Memory, which will be mapped to COM0 of LCD Display.

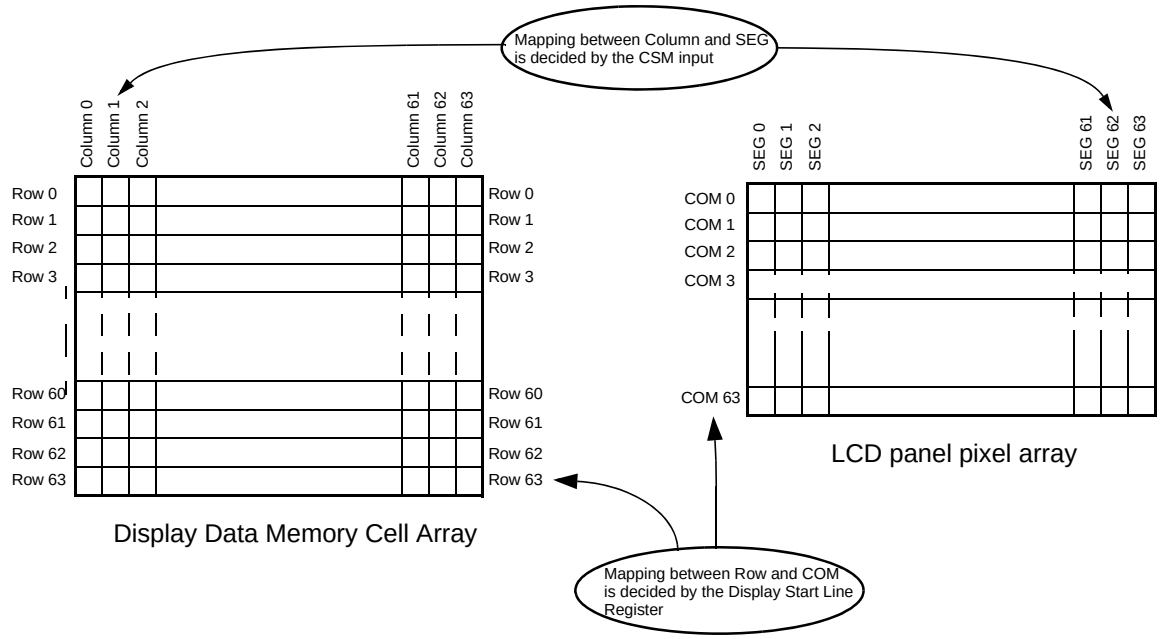


Fig.8 Memory cell array and LCD pixel array

7 REGISTERS

7.1 Registers and their states after hardware RESET

The SBN0064G has 5 registers. Four of them must be programmed by the host microcontroller after hardware reset. The Status Register can be read by the host microcontroller to check the current status of the SBN0064G.

The registers and their states after RESET is given in Table 5.

Table 5 Registers and their states after RESET

Register Name	Description	States after RESET
Display ON/OFF Register	The Display ON/OFF Register is a 1-bit register. After RESET, its value is LOW and, therefore, the LCD display is turned OFF.	0
Display Start Line Register	The Display Start Line Register is a 6-bit register. After RESET, its value is 00 0000 and, therefore, Row 0 of the Display Data Memory is mapped to COM0 of LCD panel.	00 0000
Page Address Register	The Page Address Register is a 3-bit register. It point to a page of the Display Data Memory.	xxx
Column Address Register	The Column Address Register is a 6-bit register.	xx xxxx
Status Register	The Status Register shows the current state of the SBN0064G. It is a 3-bit register, with each bit showing the status of a programmed function.	0010 0000

7.2 Display ON/OFF and the Display ON/OFF Register

The Display ON/OFF Register is a 1-bit Register. When this bit is programmed to HIGH, the display is turned ON. When this bit is programmed to LOW, the display is turned OFF and SEG0 ~ SEG63 outputs are set to V_{DD}.

To program this register, the setting of control bus is given in Table 6 and the setting of the data bus is given in Table 7.

Table 6 Setting of the control bus for programming the Display ON/OFF Register

$\overline{C}$/D	R/$\overline{W}$
0	0

Table 7 Setting of the data bus for programming the Display ON/OFF Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
0	0	1	1	1	1	1	D0

When D0=1, the code is 3F(Hex) and the display is turned ON. When D0=0, the code is 3E(Hex) and the display is turned OFF.

7.3 Display Start Line and the Display Start Line Register

The Display Start Line Register is a 6-bit register. It points at the first row of a block of the Display Data Memory, which will be mapped to COM0. The length of the block of the memory is decided by the display duty, which is decided by the SBN6400G. For example, if the Display Start Line Register is programmed with 00010 (decimal 2) and display duty is 1/64, then Row2 of the Display Data Memory will be mapped to COM0 of LCD panel, Row3 to COM1, Row4 to COM2, ...Row62 to COM60, Row63 to COM61, ...Row0 to COM62, and finally Row1 to COM63, as illustrated in Fig. 9.

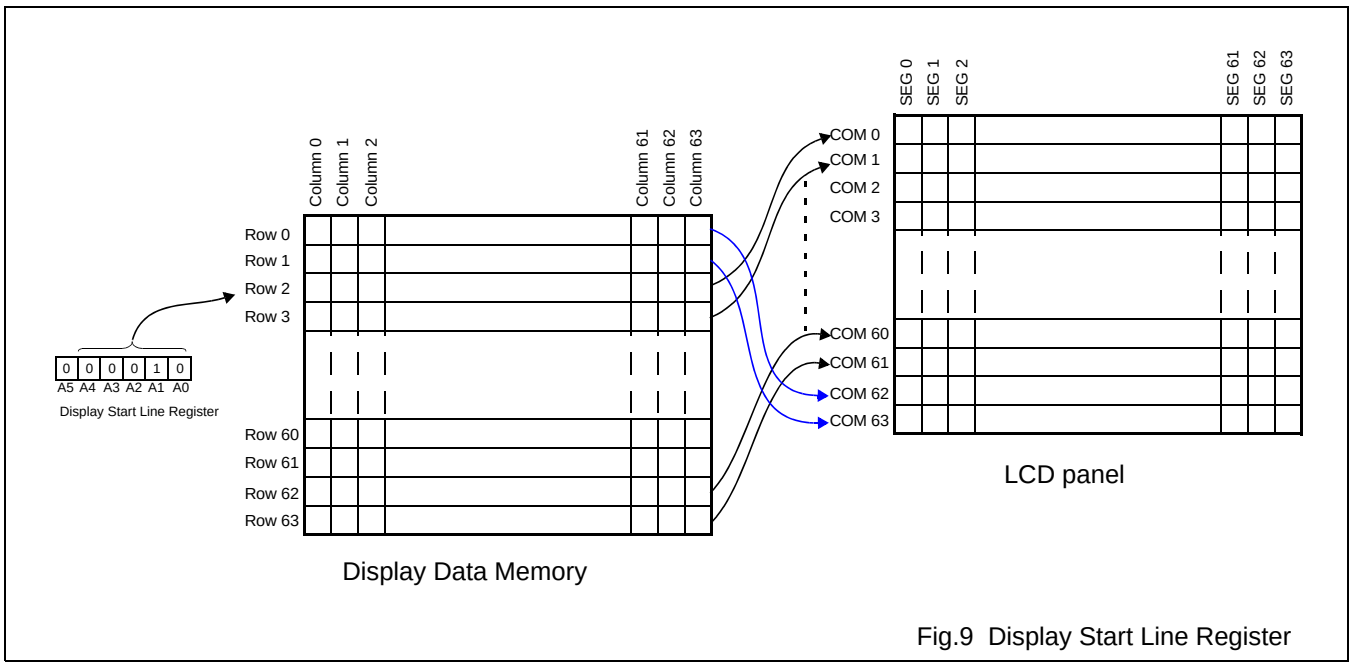


Fig.9 Display Start Line Register

To program this register, the setting of the control bus is given in Table 8 and the setting of the data bus is given in Table 9.

Table 8 The setting of the control bus for programming the Display Start Line Register

$\overline{C}$/D	R/$\overline{W}$
0	0

Table 9 The setting of the data bus for programming the Display Start Line Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	1	A5	A4	A3	A2	A1	A0

A5 ~ A0 are Display Start Line address bits and can be programmed with a value in the range from 0 to 63. Therefore, the code can be from 1100 0000 (C0 Hex) to 1111 1111 (FF Hex).

7.4 Mapping between Memory Columns and Segments

The mapping relation between the column outputs of the Display Data Memory and the Segment outputs SEG0~SEG63 is decided by the CSM (Column/Segment Mapping) input.

If CSM input is connected to HIGH, then data from column 0 of the Display Data Memory is output from SEG0. This type of mapping is called *normal mapping*.

If CSM input is connected to LOW, then the data from column 63 of the Display Data Memory is output from SEG0. This type of mapping is called *inverted mapping*.

By use of this input, the flexibility of component placement and routing on a PCB can be increased.

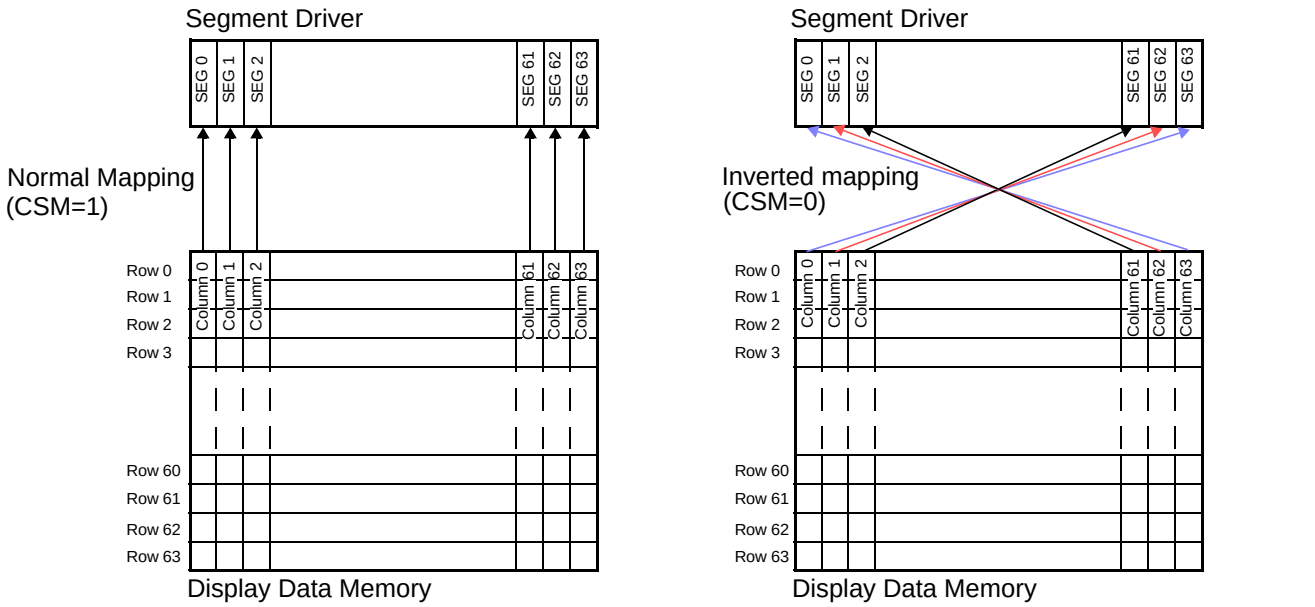


Fig.10 Column/Segment Mapping.

7.5 Display Data Memory Page and the Page Address Register

The Display Data Memory is divided into 8 pages: Page 0 ~ Page 7, with each page having 64 bytes in horizontal direction. Page 0 is from Row 0 to Row 7, Page 1 from Row 8 to Row 15, Page 2 from Row 16 to Row 23, and Page 3 from Row 24 to Row 31,...etc, as shown in Fig 11. When the host microcontroller intends to perform a READ/WRITE operation to the Display Data Memory, it has to program the Page Address Register to indicate which page it intends to access.

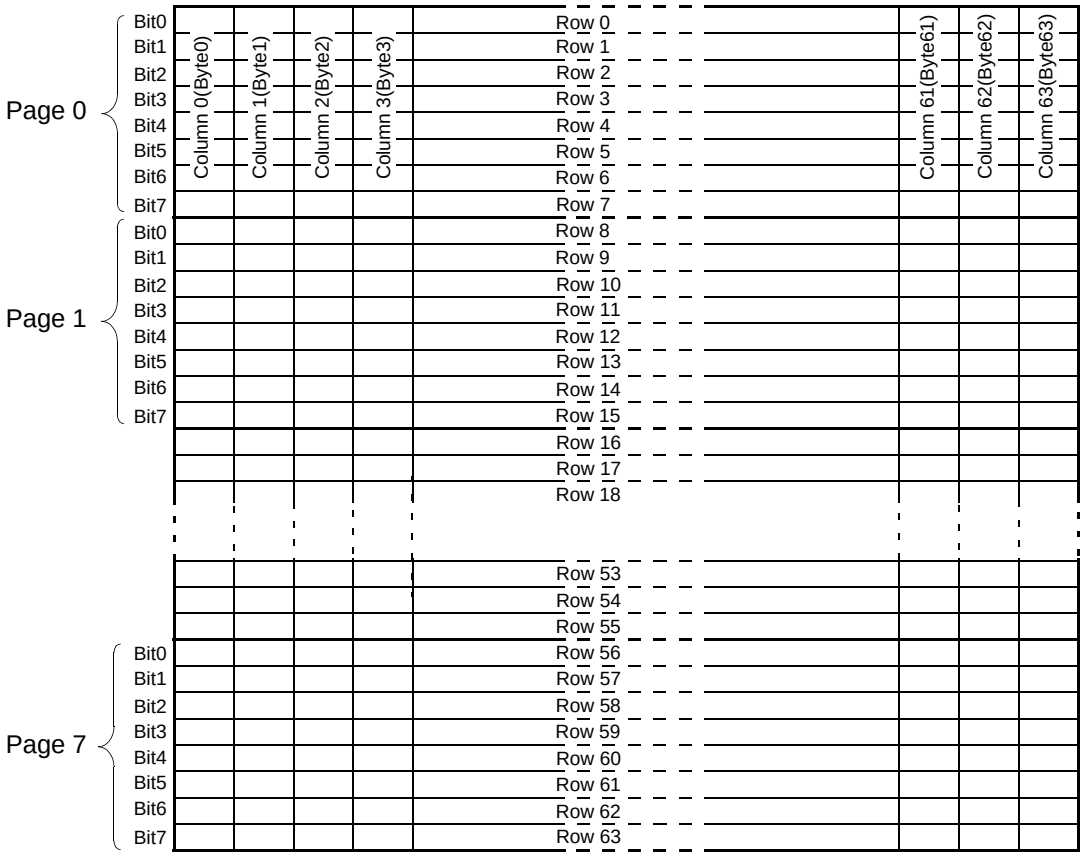


Fig.11 Page/Column address of the Display Data Memory

To program this register, the setting of the control bus is given in Table 10 and the setting of the data bus is given in Table 11.

Table 10 The setting of the control bus for programming the Page Address Register

$\overline{C}$/D	R/$\overline{W}$
0	0

Table 11 The setting of the data bus for programming the Page Address Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	0	1	1	1	A2	A1	A0

A2, A1and A0 are page address bits and can be programmed with a value in the range from 0 to 7. A2 A1 A0=000 selects Page 0; A2 A1 A0=001 selects Page 1; A2 A1 A0=010 selects Page 2, and A2 A1 A0=011 selects Page 3...etc. Therefore, the code can be from 1011 1000 (B8 Hex) to 1011 1111 (BF Hex).

7.6 Column address and the Column Address Register

The Column Address Register points at a column of the Display Data Memory which the host microcontroller intends to perform a READ/WRITE operation. To read or write a byte of the Display Data Memory, both its Page Address and Column Address must be specified.

The Column Address Register automatically increments by 1 after a READ or WRITE operation is finished. When the Column Address Register reaches 63, it overflows to 0. Please refer to Fig.11 for the column address sequence in a page of the Display Data Memory.

To program this register, the setting of the control bus is given in Table 12 and the setting of the data bus is given in Table 13.

Table 12 The setting of the control bus for programming the Column Address Register

$\overline{C}$/D	R/$\overline{W}$
0	0

Table 13 The setting of the data bus for programming the Column Address Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
0	1	A5	A4	A3	A2	A1	A0

A5~A0 are column address bits and can be programmed with a value in the range from 0 to 63. Therefore, the code can be from 0100 0000 (40 Hex) to 0111 1111 (7F Hex).

7.7 Status Read and Status Register

The Status Register shows the current state of the SBN0064G. It can be read by the host microcontroller. Bits 4, 5, 7 shows the current status and Bits 0~3, and 6 are always fixed at 0.

To read the Status Register, the setting of the control bus is given in Table 14; the bit allocation is given in Table 15; the description for each bit is given in Table 16.

Table 14 The setting of the control bus for reading the Status Register

$\overline{C}$/D	R/$\overline{W}$
0	1

Table 15 The Status Register bit allocation

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
BUSY	0	ON/OFF	RESET	0	0	0	0

Table 16 The Status Register bit description

Bit	Description
BUSY	BUSY=1 indicates that the SBN0064G is currently busy and can not accept new code or data. The SBN0064G is executing an internal operation. BUSY=0 indicates that the SBN0064G is not busy and is ready to accept new code or data.
ON/OFF	The ON/OFF bit indicates the current of status of display. If ON/OFF=0, the display has been turned ON. If ON/OFF=1, the display has been turned OFF. Note that the polarity of this bit is inverse to that of the Display ON/OFF Register.
RESET	RESET=1 indicates that the SBN0064G is currently in the process of being reset. RESET=0 indicates that the SBN0064G is currently in normal operation.

8 READ OR WRITE OPERATION TO THE DISPLAY DATA MEMORY

READ or WRITE operation to the Display Data Memory is shown in Table 17. When performing a READ or WRITE operation, the host microcontroller should give the control bus $\overline{C}$/D, E, and R/$\overline{W}$ proper value and timing.

Table 17 READ/WRITE operation

Operation	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
Write Display Data	Data to be written into the Display Data Memory.								Write a byte of data to the Display Data Memory. The data to be written is put on the data bus by the host microcontroller.
Read Display Data	Data read from the Display Data Memory output latch.								Read a byte of data from the Display Data Memory. The data read from the internal 8-bit output latch (refer to Fig. 12) appears on the data bus. A dummy read is needed to get correct value.

8.1 Write Display Data

The Write Display Data operation writes a byte (8 bits) of data to the Display Data Memory. Data is put on the data bus by the host microcontroller. The location which accepts this byte of data is pointed to by the Page Address Register and the Column Address Register. At the end of the operation, the content of the Column Address Register is automatically incremented by 1.

For page address and column address of the Display Data Memory, please refer to Fig. 11.

Table 18 gives the control bus setting for this command.

Table 18 The setting of the control bus for Write Display Data operation

$\overline{C}$/D	R/$\overline{W}$
1	0

8.2 Read Display Data

The Read Display Data operation is a 3-step operation.

1. First, the current data of the internal 8-bit output latch of the Display Data Memory is read by the microcontroller, via the 8-bit data bus DB0~DB7.
2. Then, a byte of data of the Display Data Memory is transferred to the 8-bit output latch from a location specified by the Page Address Register and the Column Address Register,
3. Finally, the content of the Column Address Register is automatically incremented by one.

Fig. 12 shows the internal 8-bit output latch located between the 8-bit I/O data bus and the Display Data Memory cell array. Because of this internal 8-bit output latch, a dummy read is needed to obtain correct data.

For Display Data Write operation, a dummy write **is not** needed, because data can be directly written from the data bus to internal memory cells.

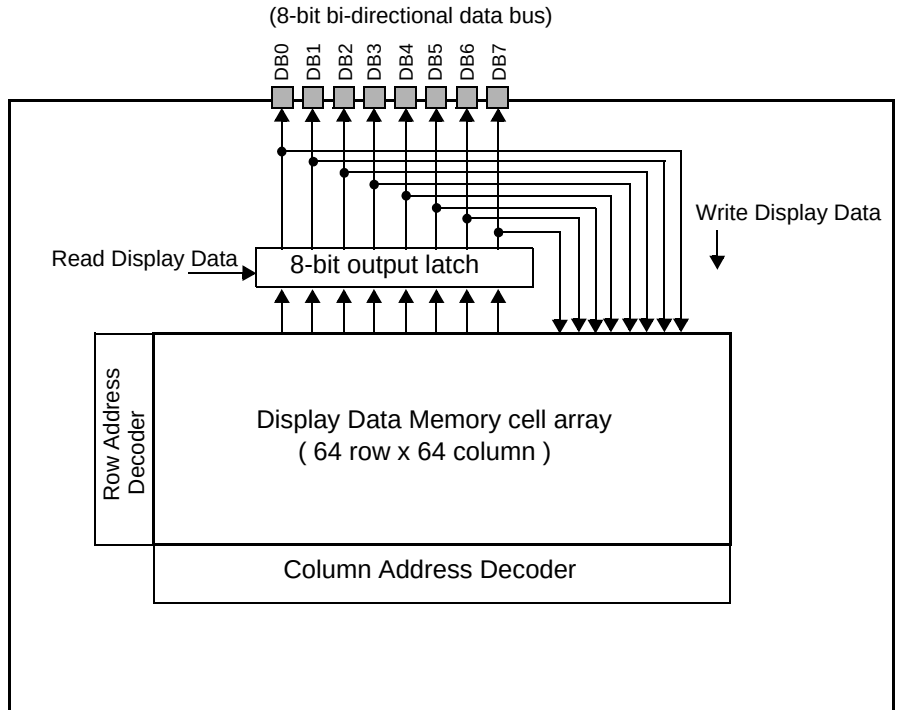


Fig.12 Read Display Data Memory

Table 19 gives the control bus setting for this command.

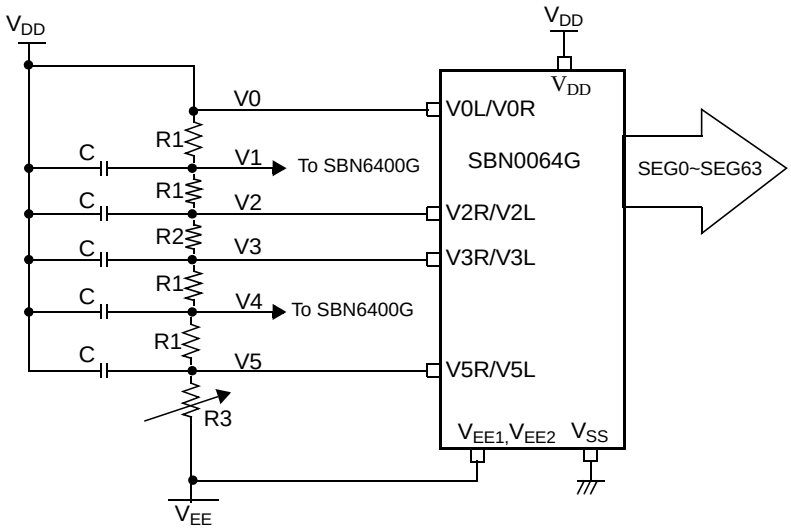
Table 19 The setting of the control bus for Read Display Data command

$\overline{C}$/D	R/$\overline{W}$
1	1

9 LCD BIAS CIRCUIT

A typical LCD bias circuit is shown Fig. 13. The condition $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must always be met. The maximum allowed voltage for LCD bias ($V_{LCD}=V_{DD}-V_5$) should not exceed 13 volts. Note that V0 should be connected to V_{DD}.

COMPONENT	RECOMMENDED VALUE
C	0.1 μF, electrolytic
R1	2.2K
R2	10K
R3	10K



Note:

(1) V0 should always be connected to V_{DD}.

(2) For cascading application, it is recommended that a buffer be added for each of V1, V2, V3, V4, and V5. For 64 COM x 64 SEG application, these buffers are not needed.

(3) The LCD bias voltage (V_{LCD} = V0 - V5) should not exceed 13 volts, without regard to display duty.

(4) The voltage difference between V_{DD} (the most positive power) and V_{EE} (the most negative power), V_{DD} - V_{EE}, should not exceeds 16 volts, without regards to display duty.

Fig.13 LCD Bias circuit

10 COMMON, SEGMENT OUTPUT VOLTAGE

The output voltage level of COMMON driver (the SBN6400G) and SEGMENT driver (SBN0064G) is given in Table 20.

The output voltage level of COMMON driver is decided by the combination of AC Frame signal (M) and internal Shift Register output.

The output voltage level of SEGMENT driver is decided by the combination of AC Frame signal (M), Display Data, and the Display ON/OFF register.

Table 20 COMMON/SEGMENT output voltage level

FR	Data	DISPLAY ON/OFF	SEG0~SEG63 (SBN0064G)	COM0~COM63 (SBN6400G)
L	L	ON	V2	V1
L	H	ON	V0	V5
H	L	ON	V3	V4
H	H	ON	V5	V0
x(don't care)	x(don't care)	OFF	V2, V3	x

Note that, in the above table, "Data" for the COM0~COM63 is actually the output of the internal Shift Register of the SBN6400G COMMON driver, which sequentially activates COM0~COM63.

11 MAXIMUM RATING

11.1 Absolute maximum rating

Table 21 Absolute maximum rating

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	voltage on the V_{DD} pin(pad)	–0.3	+7.0	volt
V_{EE}	voltage on the V_{EE} pin(pad)	V_{DD} - 16		
V_{LCD} (note 2)	LCD bias voltage, V_{LCD}=V0-V5		13	
V_I	input voltage on any pin with respect to V_{SS}	–0.3	V_{DD} + 0.3	
P_D	power dissipation		200	mW
T_{stg}	storage temperature range	–55	+125	°C
T_{amb}	operating ambient temperature range	-30	+ 85	°C
Tsol (note 3)	soldering temperature/time at pin		260 °C, 10 Second	

Notes

1. The following applies to the Absolute Maximum Rating:
   a) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.
   b) The SBN0064G includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge (ESD). However, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
   c) Parameters are valid over operating temperature range unless otherwise specified.
   d) All voltages are with respect to $V_{SS,}$ unless otherwise noted.
2. The condition $V_{DD}(V0) \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must always be met.
3. QFP-type packages are sensitive to moisture of the environment, please check the drypack indicator on the tray package before soldering. Exposure to moisture longer than the rated drypack level may lead to cracking of the plastic package or broken bonding wiring inside the chip.

12 DC CHARACTERISTICS

Table 22 DC Characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS}, unless otherwise specified; T_{amb} = −20 to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage for logic		4.5	5.0	5.5	V
V_{NEG}	$V_{NEG}=V_{DD}-V_{EE}$				16	V
V_{LCD}	LCD bias voltage $V_{LCD}= V0(V_{DD})-V5$	Note 1.			13	V
V_{IL}	LOW level input voltage	For all inputs	0		0.8	V
V_{IH}	HIGH level input voltage	For all inputs	V_{DD}-2.2		V_{DD}	V
V_{OL}	LOW level output voltage of DB0~7 at I_{OL}=1.6 mA.		0.0		0.3	V
V_{OH}	HIGH level output voltage of DB0~7 at I_{OH}=-200μA.		V_{DD} − 0.3		V_{DD}	V
I_{LKG}	Leakage current of input pins	for all inputs			0.2	μA
I_{STBY}	Stand-by current at V_{DD}=5 volts	Note 2			3.0	μA
$I_{DD(1)}$	Operating current for display-only operation	Note 3			100	μA
$I_{DD(2)}$	Operating current for display and microcontroller access at t_{CYC}=1 MHz	Note 4			500	μA
C_{in}	Input capacitance of all input pins			5.0	8.0	pF
R_{ON}	LCD driver ON resistance	Note 5		5.0	7.5	KΩ

Notes:

1. LCD bias voltage V_{LCD} is V0 - V5. V0 should always be connected to VDD.
2. Conditions for the measurement: CLK1=CLK2=V_{DD}, measured at the V_{DD} pin.
3. This value is measured when the microcontroller does not perform any READ/WRITE operation to the chip and the chip is only performing display operation, with the following condition: 1/64 duty, $F_{CLK1,CLK2}$=250 KHz, frame frequency= 70Hz, and no loading for SEG0~63.
4. This values is measured when the microcontroller continuously performs READ/WRITE operation to the chip and the chip is also performing display operation with the following condition: 1/64 duty, $F_{CLK1,CLK2}$=250 KHz, frame frequency= 70Hz, and no loading for SEG0~63.
5. This measurement is for the transmission high-voltage PMOS or NMOS of SEG0~SEG63. Please refer to Section 16 for these driver circuit. The measurement is for the case when the voltage differential between the source and the drain of the high voltage PMOS or NMOS is 0.1 volts.

13 AC TIMING CHARACTERISTICS

13.1 Display control signal (CL, FRM, and M) timing

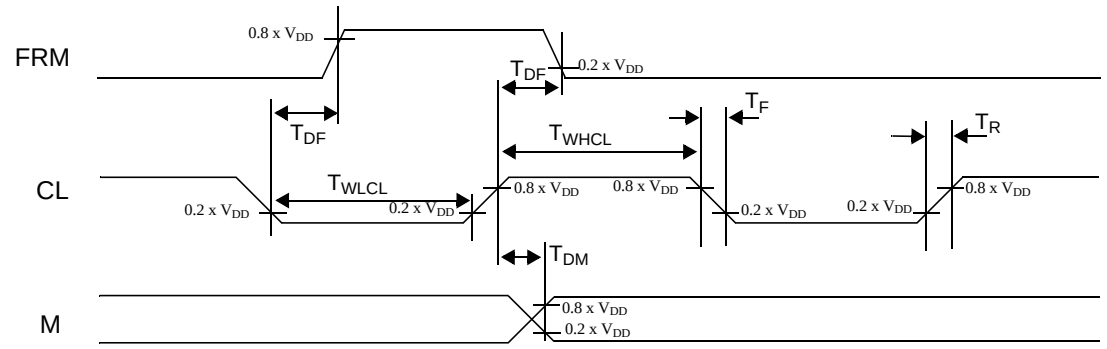


Fig.14 Display Control Signal Timgin

Table 23 Display control signal (CL, FRM, and M) timing characteristics at V_{DD}=5 volts

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = −20 to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{WHCL}	CL clock high pulse width		33			µs
T_{WLCL}	CL cock low pulse width		33			µs
T_R	CL clock rise time			28	120	ns
T_F	CL clock fall time			28	120	ns
T_{DF}	FR delay time (input)		-1.8		1.8	µS
T_{DM}	FR delay time (output)		-1.8		1.8	µS

13.2 CLK1, CLK2 timing

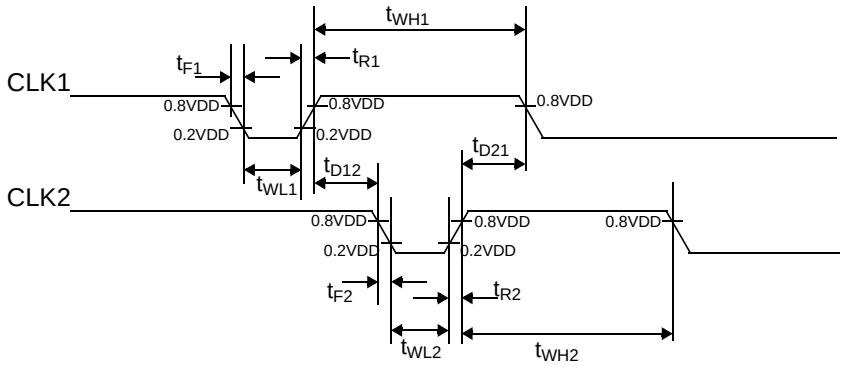


Fig.15 CLK1, CLK2 Timing

Table 24 CLK1 and CLK2 timing characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = −20 to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{WH1}	CLK1 clock high pulse width		2000			ns
T_{WL1}	CLK1 cock low pulse width		600			
T_{R1}	CLK1 clock rise time				130	
T_{F1}	CLK1 clock fall time				130	
T_{WH2}	CLK2 clock high pulse width		2000			
T_{WL2}	CLK2 clock low pulse width		600			
T_{R2}	CLK2 clock rise time				130	
T_{F2}	CLK2 clock fall time				130	
T_{D12}	CLK1-to-CLK2 delay		660			
T_{D21}	CLK2-to-CLK1 delay		660			

13.3 Microcontroller interface timing for writing to the SBN0064G

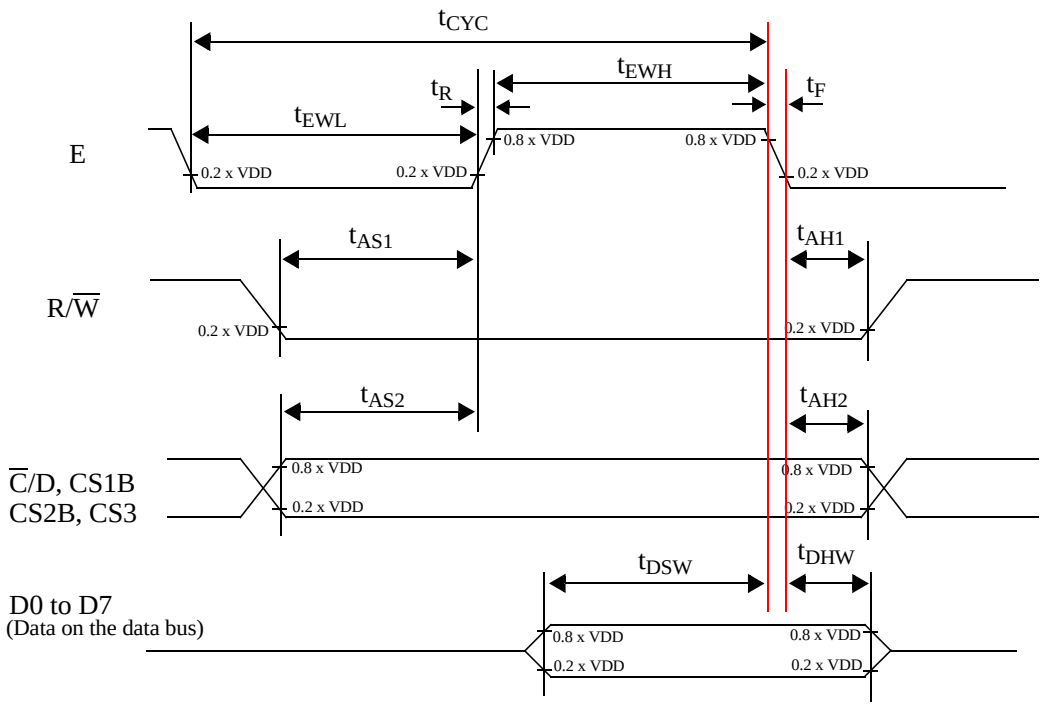


Fig.16 AC timing for writing to the SBN0064G

Table 25 AC timing for writing to the SBN0064G

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = -20 °C to +75°C.

symbol	parameter	min.	max.	test conditions	unit
t_{CYC}	Enable (E) cycle time	1000			ns
t_{EWL}	Enable (E) LOW width	450			
t_{EWH}	Enable (E) HIGH width	450			
t_R	Enable (R) rise time		20		
t_F	Enable (F) fall time		20		
t_{AS1}	Write set-up time	140			
t_{AH1}	Write hold time	10			
t_{AS2}	C/D, CS1B, CS2B, CS3 set-up time	140			
t_{AH2}	C/D, CS1B, CS2B, CS3 hold time	10			
t_{DSW}	Data setup time (on the data bus)	200		The loading on the data bus is shown in Fig. 18.	
t_{DHW}	Data hold time (on the data bus)	10			

13.4 Microcontroller interface timing for reading from the SBN0064G

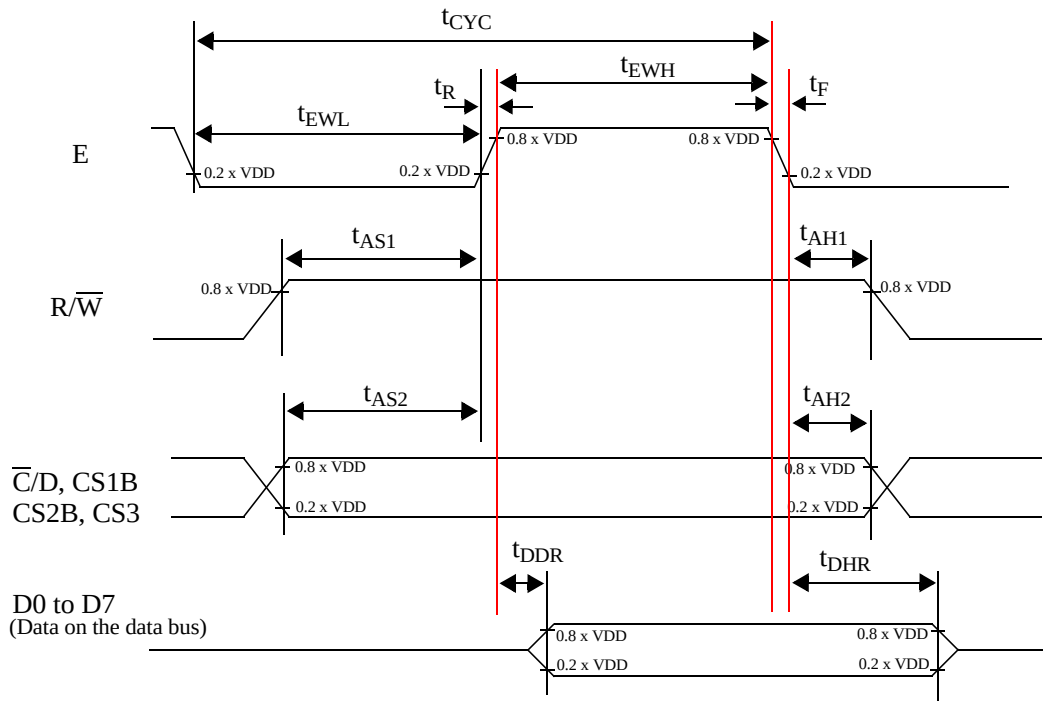
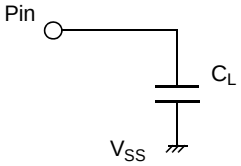


Fig.17 AC timing for reading from the SBN0064G

Table 26 AC timing for reading from the SBN0064G

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = -20 °C to +75°C.

symbol	parameter	min.	max.	test conditions	unit
t_{CYC}	Enable (E) cycle time	1000			ns
t_{EWL}	Enable (E) LOW width	450			
t_{EWH}	Enable (E) HIGH width	450			
t_R	Enable (R) rise time		20		
t_F	Enable (F) fall time		20		
t_{AS1}	READ set-up time	140			
t_{AH1}	READ hold time	20			
t_{AS2}	C/D, CS1B, CS2B, CS3 set-up time	140			
t_{AH2}	C/D, CS1B, CS2B, CS3 hold time	10			
t_{DDR}	Data delay time (on the data bus)	320		The loading on the data bus is shown in Fig. 18.	
t_{DHR}	Data hold time (on the data bus)	20			



C_L = 50 pF (including wiring and probe capacitance).

Fig.18 Load circuit for each bit of the data bus.

14 APPLICATION EXAMPLE (1/64 DISPLAY DUTY)

14.1 Application circuit for 1/64 display duty

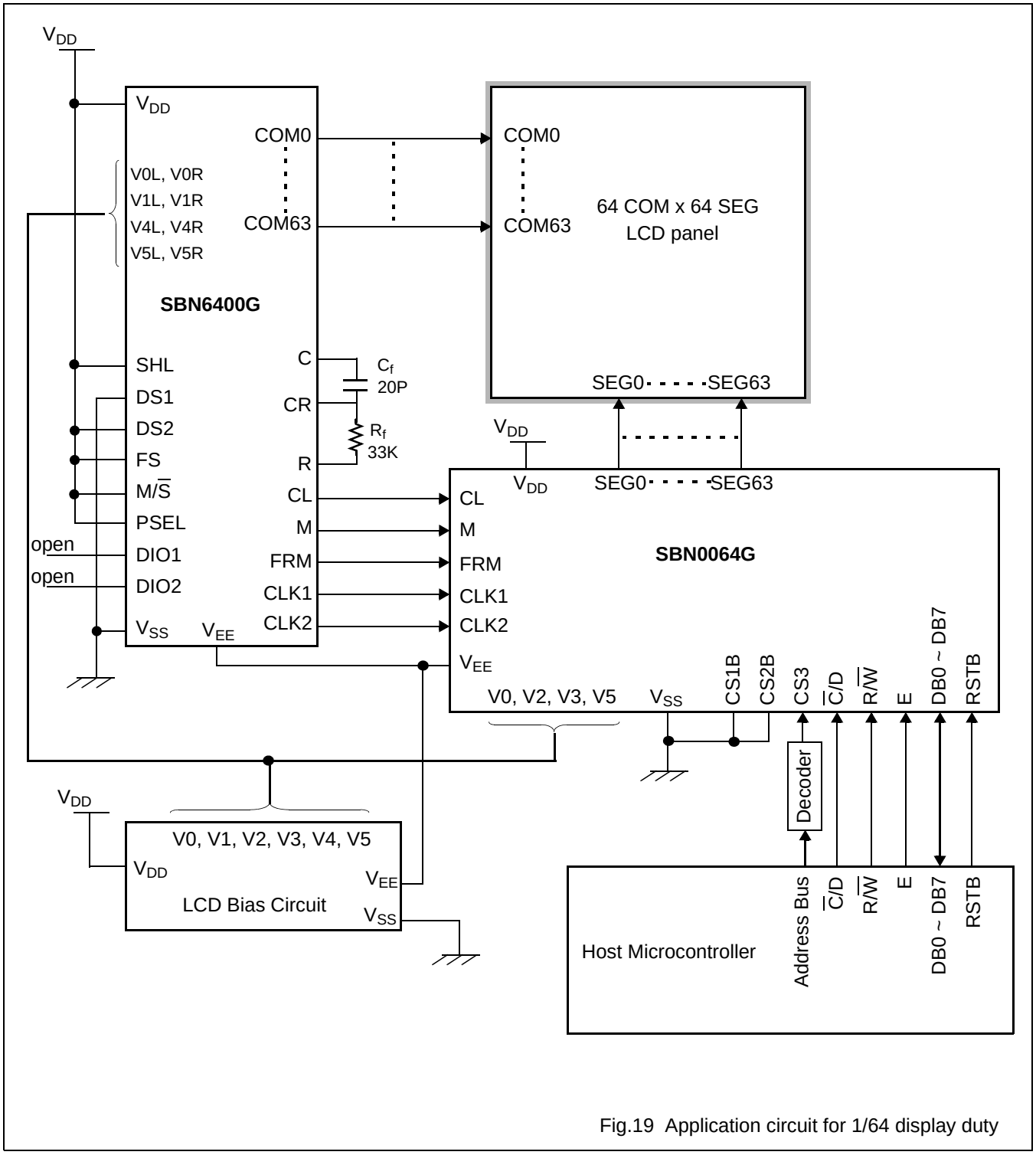
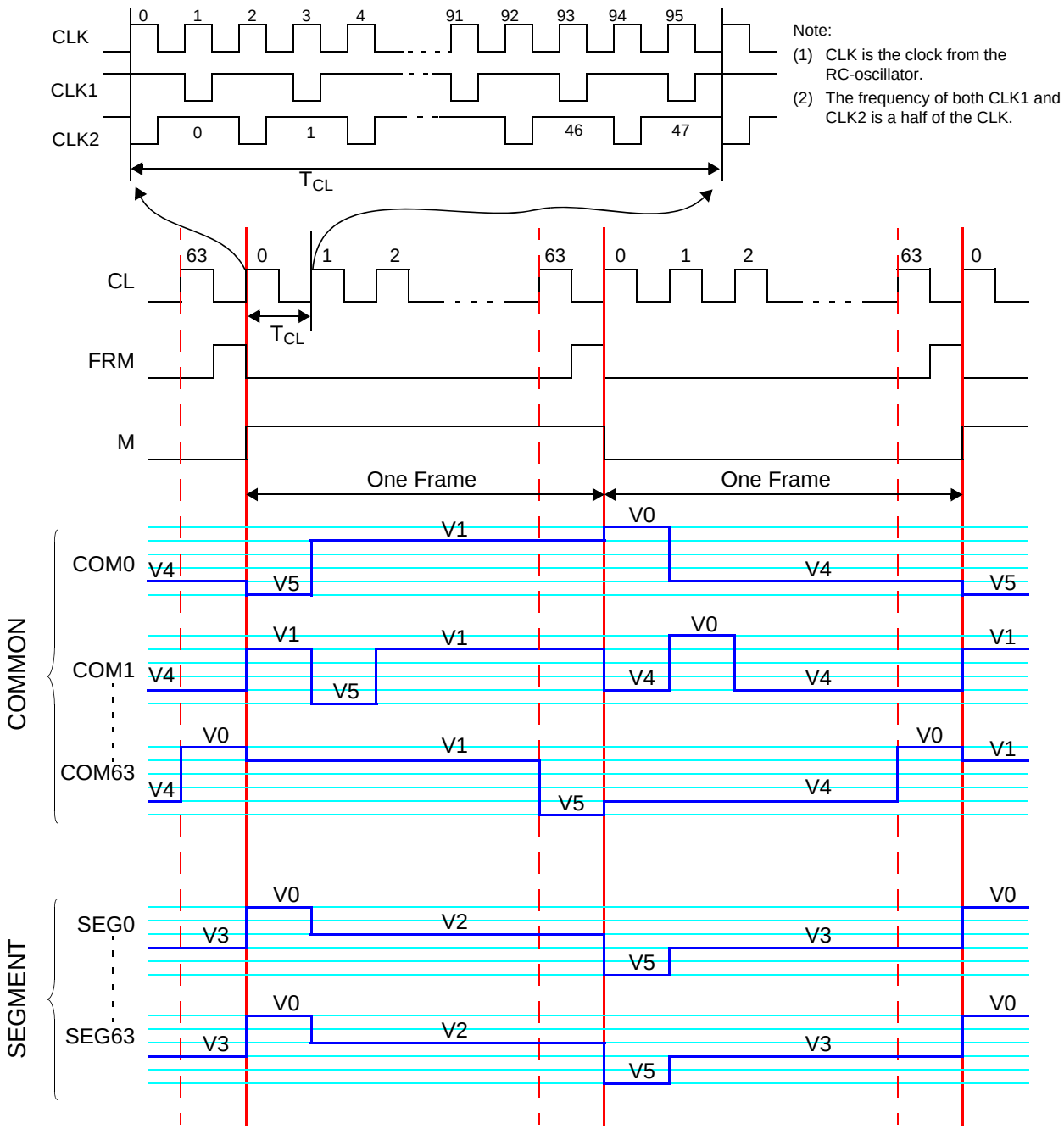


Fig.19 Application circuit for 1/64 display duty

14.2 Timing Diagram of 1/64 display duty



Note:

COMMON is the scan signal for horizontal display line.
SEGMENT is the display data from the on-chip display data. The wave form of this example shows that only the top line of the panel is turned ON.

Fig.20 Timing diagram for 1/64 display duty

15 MASTER/SLAVE APPLICATION EXAMPLE

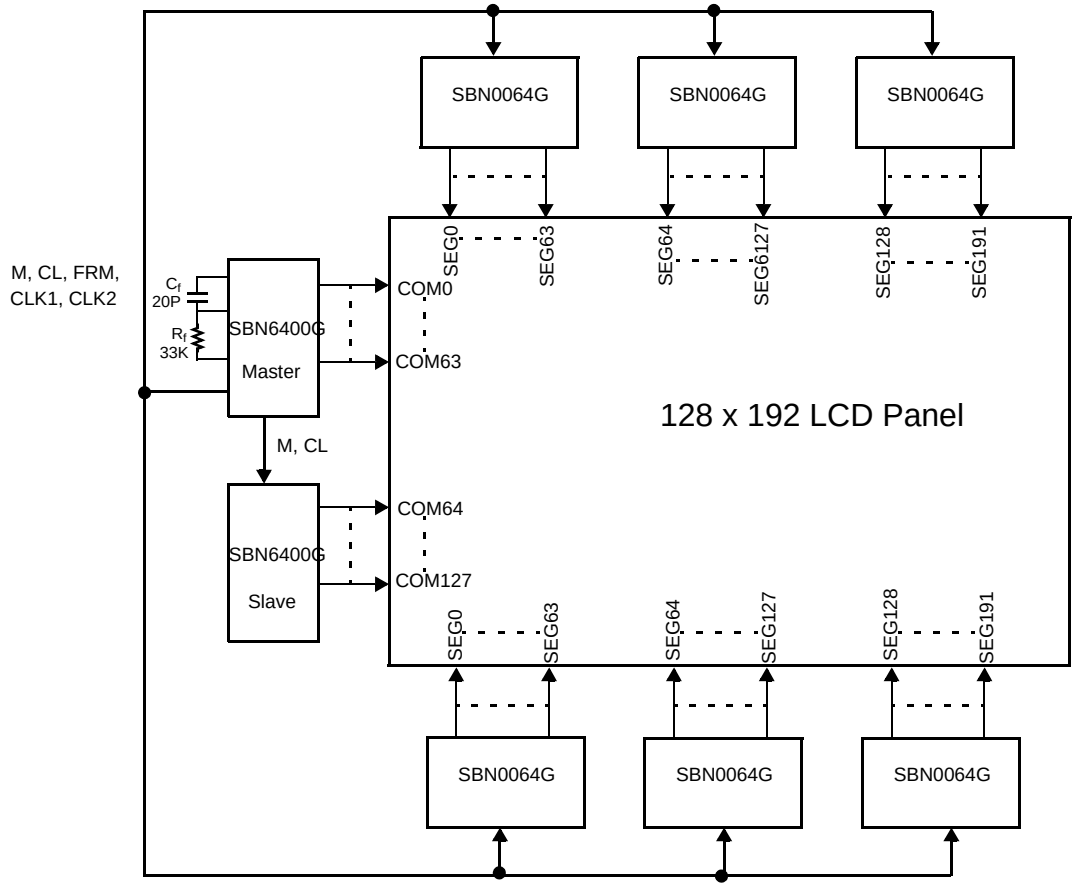
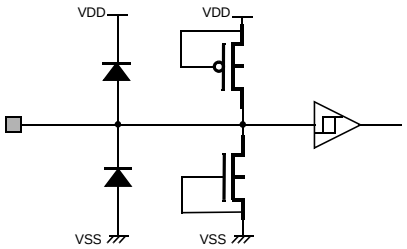
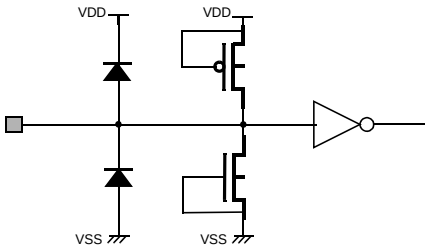
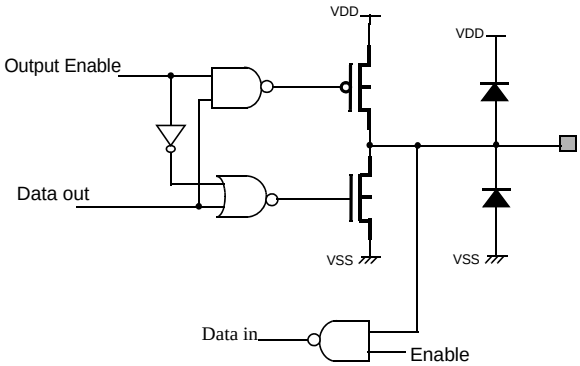
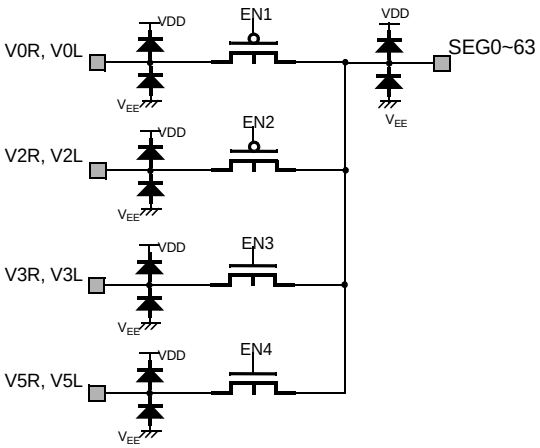


Fig.21 Master/Slave application example

16 PIN CIRCUITS

Table 27 MOS-level schematics of all input, output, and I/O pins.

SYMBOL	Input/output	CIRCUIT	NOTES
$\overline{C}$/D, R/$\overline{W}$, E, CS1B, CS2B, CS3, RSTB	Inputs		
CLK1, CLK2, FRM, CL, M, CSM	Input		
DB0~DB7	I/O		
SEG0~63			

17 APPLICATION NOTES

1. It is recommended that the following power-up sequence be followed to ensure reliable operation of your display system. As the ICs are fabricated in CMOS and there is intrinsic latch-up problem associated with any CMOS devices, proper power-up sequence can reduce the danger of triggering latch-up. When powering up the system, control logic power must be powered on first. When powering down the system, control logic must be shut off later than or at the same time with the LCD bias (V_{EE}).

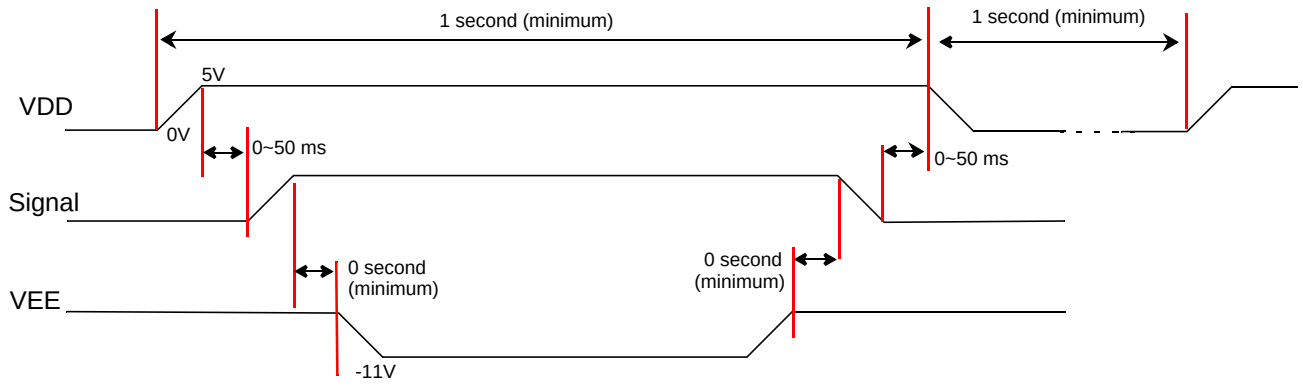


Fig.22 Recommended power up/down sequence

2. The metal frame of the LCD panel should be grounded.
3. A 0.1 μF ceramic capacitor should be connected between V_{DD} and V_{SS}.
4. A 0.1 μF ceramic capacitor should be connected between V_{DD} (or V_{SS}) and each of V1, V2, V3, V4, and V5.
5. If the length of the cable connecting the host microcontroller and the LCD module is longer than 45 cm, a ceramic capacitor of 20P~150P should be connected between V_{DD} (or V_{SS}) and each of the R/$\overline{W}$, E, and $\overline{C}$/D.

18 PACKAGE INFORMATION

Package information is provided in another document. Please contact Avant Electronics for package information.

19 SOLDERING

19.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. For more in-depth account of soldering ICs, please refer to dedicated reference materials.

19.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, please contact Avant for drypack information.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

19.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

19.4 Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

20 LIFE SUPPORT APPLICATIONS

Avant's products, unless specifically specified, are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Avant customers using or selling Avant's products for use in such applications do so at their own risk and agree to fully indemnify Avant for any damages resulting from such improper use or sale.