R61516

260–k color, 240x320-dot graphics LCD controller driver for a-Si TFT Panel

REJxxxxxxx-xxxx
Rev.0.04
July 12, 2007

Description

The R61516 is liquid crystal controller driver LSI with internal frame memory or amorphous silicon TFT panel sized 240RGB x 320-dot at the maximum. The driver supports MIPI DBI Type B (18-/16-/9-/8- bit) and Type C (Option 1, Option 3) as system interface to microcomputer as well as high-speed frame memory write function, enabling efficient data transfer.

The R61516 also supports MIPI DPI (VSYNC, HSYNC, PCLK, DE, DB[17:0]) enabling to display video images.

The R61516 incorporates step-up and voltage follower circuits to generate drive voltage required for α-Si TFT panel. Other features include 8-color display and power management functions, making the driver best suitable for small or mid sized portable devices such as digital mobile phone and small PDA.

*MIPI: Mobile Industrial Processor Interface, DBI: Display Bus Interface, DPI: Display Pixel Interface

Features

- Single chip driver for 260-k color TFT 240RGB x 320 dot graphics (with internal source, gate and power supply circuits)
- System Interface
  Command set method (based on MIPI DCS Version 1.01.00) *DCS: Display Command Set
  MIPI-DBI (based on MIPI DBI Version 2.00)
  Type B 16-/18- bit, 8-/9- bit
  Type C 4-line 9bit (Option 1), 8 bit (Option 3)
- Video image display interface
  TE-I/F (MIPI DBI + TE synchronization signal output)
  VSYNC I/F (MIPI DBI + VSYNC)
  MIPI-DPI (based on MIPI DPI-2 Version 2.00)
- Abundant color display
  260k-color display
  Partial display function
- Low-power consumption architecture (allowing direct input of interface I/O power supply)
  Deep standby function
  8-color mode (Idle mode)
  Input power supply voltage:
  Interface I/O power supply IOVCC = 1.65~3.10V
  Logic power supply VCC=2.5~3.3V
  Liquid crystal analog circuit power supply VCI=2.5~3.3V
- Internal liquid crystal drive power supply circuit
  Source driver liquid crystal drive / VCOM power supply:
  DDVDH-GND=4.5~6.0V
  VCL-GND= -1.9~ -3.0V
  VCI-VCL ≤ 6V

Gate driver power supply:
VGH-GND= 10~18.0V
VGL-GND= -4.5 ~ -13.5V
VGH-VGL≤ 28V

VCOM drive (VCOM):
VCOMH=3.0 ~ (DDVDH-0.5)V
VCOML= (VCL+0.5) ~ 0V
Amplitude between VCOMH and VCOML= max 6V

- TFT storage capacitance: Cst only (common VCOM formula)
- Internal frame memory: 172,800 bytes
- Liquid crystal display drive circuits: 720 source signal lines, 320 gate signal lines
- Single chip, gate output arranged on both sides of the chip: enables COG mounting
- RGB separate correction function
- Internal NVM (32 bits for user identification code, 7 bits for VCOM adjustment): Rewriting is guaranteed up to 5 times.
- Incorporates EEPROM interface (standard interface based on Microwire)

Power Supply Specification

Table 1 R61516 Power Supply Specification

No.	Item		R61516
1	TFT data lines drive circuit		720 outputs
2	TFT gate line drive circuit		320 outputs
3	TFT display storage capacitance		Cst only (common VCOM method)
4	Liquid crystal drive output	S1 ~ S720	V0 ~ V63 grayscales
		G1 ~ G320	VGH-VGL
		VCOM	Change VCOMH with electronic volume or from VCOMR Change VCOMH-VCOML amplitude with electronic volume
5	Input voltages	IOVCC (interface voltage)	IOVCC=1.65V ~ 3.1 V in MIPI DBI Type B, Type C, DPI operation. Power supply to CSX, DCX, WRX, RDX, DB[17:0], DIN, DOUT, VSYNC, HSYNC, PCLK, DE, TE, IM[2:0], RESX, PROTECTX Connect to VCC and VCI on the FPC when the electrical potentials are the same.
		VCC (power supply to for logic regulator or EEPROM I/F)	2.5V ~ 3.3V Connect to IOVCC and VCI on the FPC when the electrical potentials are the same.
		VCI (LCD drive power supply)	2.5V ~ 3.3V Connect to IOVCC and VCC on the FPC when the electrical potentials are the same.
6	LCD drive supply voltages	DDVDH	4.5V ~ 6.0V
		VGH	10V ~ 18.0V
		VGL	-4.5V ~ -13.5V
		VGH-VGL	Max. 28V
		VCL	-1.9V ~ -3.0V
		VCI-VCL	Max. 6V
7	Internal step-up circuits	VLOUT1 (DDVDH)	VCI1 x 2
		VLOUT2 (VGH)	VCI1 x 5, x 6
		VLOUT3 (VGL)	VCI1 x –3, -4, -5
		VLOUT4 (VCL)	VCI1 x –1

Block Diagram

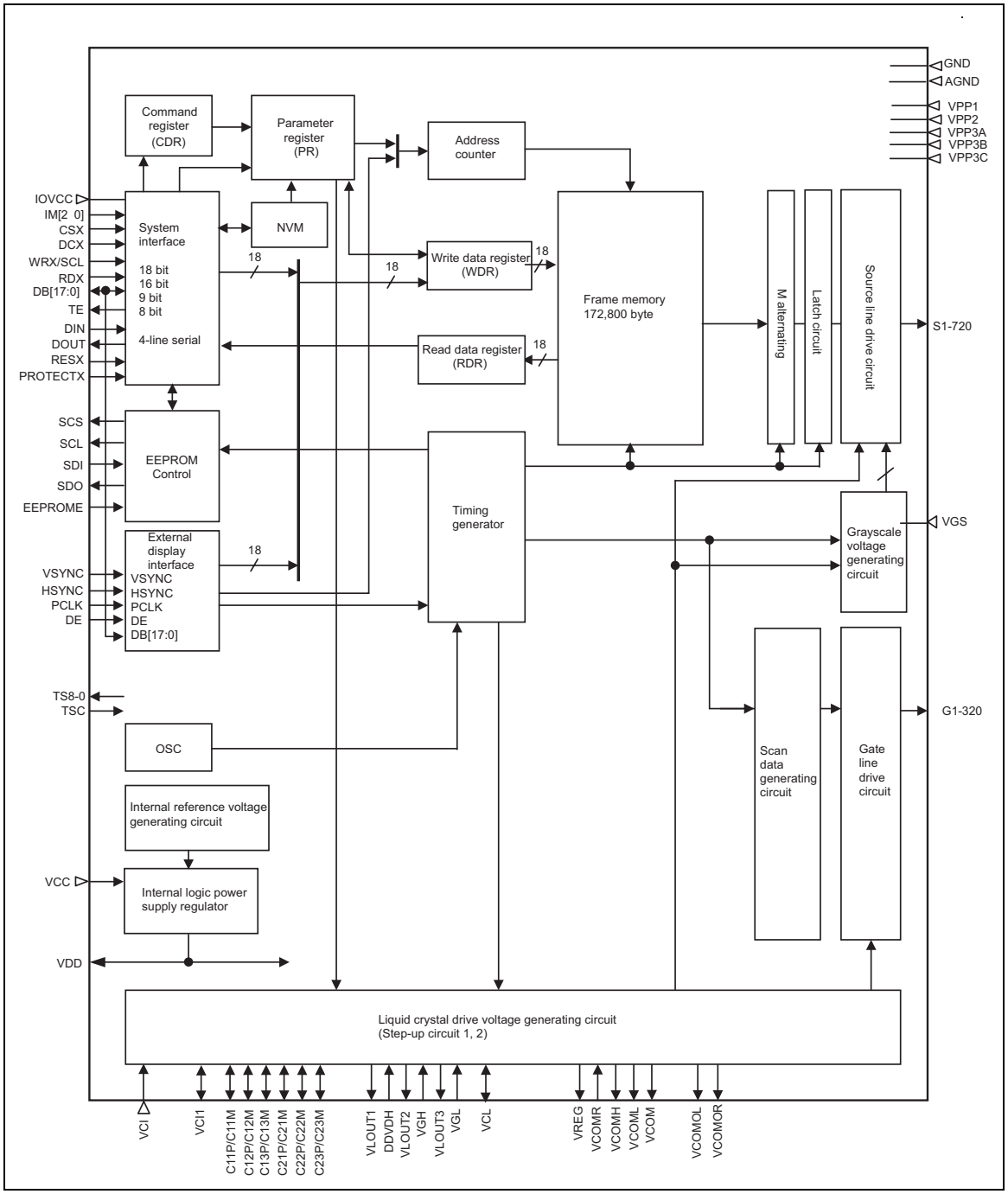


Figure 1

Block Function

1. System Interface

The R61516 supports MIPI DBI TypeB (18/16/9/8bit) and MIPI DBI TypeC (Option 1, 3). The interface is selected by setting IM0-2 pin.

Table 2

IM2	IM1	IM0	Interface	Used pin	Available color number
0	0	0	DBI TypeB 18bit	DB[17:0]	262,144
0	0	1	DBI TypeB 9bit	DB[8:0]	262,144
0	1	0	DBI TypeB 16bit	DB[15:0]	65,536 / 262,144
0	1	1	DBI TypeB 8bit	DB[7:0]	65,536 / 262,144
1	0	0	Setting inhibited	–	–
1	0	1	DBI TypeC 9bit (Option1)	DIN,DOUT	8 / 262,144
1	1	0	Setting inhibited	–	–
1	1	1	DBI Type C 8bit (Option 3)	DIN,DOUT	8 / 262,144

Set number of colors using set_pixel_format: 3Ah.

(a) MIPI DBI Type B (18-/ 16-/ 9-/ 8- bit)

The R61516 supports MIPI DBI TypeB (18/16/9/8bit). It supports. The R61516 supports command method, and has an 8-bit command register and an 8-bit parameter register. Also, the R61516 has a 18-bit write register (WDR) and read register (RDR). The WDR is used to temporarily store data that is automatically written to the internal frame memory in internal operation of the chip.

The RDR is used to temporarily store the data read out from the frame memory. When reading data from the frame memory, the R61516 first stores the data in the RDR. For this reason, invalid data is sent to the data bus at first and valid data is sent as the R61516 reads second and subsequent data from the frame memory.

Table 3 Register Selection

			Function
DCX	RDX	WRX	
0	1	↑	Command
1	↑	1	Read parameter
1	1	↑	Write parameter

(b) MIPI DBI Type B (Option 1, 3)

The R61516 supports 9bit (Option 1) and 8bit (Option 3) serial interface that uses signals CSX, DCX, SCL, DIN and DOUT.

The R61516 supports synchronous signal TE for video image. Images are updated without causing flicker on the panel by writing display data in synchronization with this TE signal.

2. External Display Interface (DPI, VSYNC-I/F)

The R61516 supports DPI and VSYNC I/F as external display interface for video image. When DPI is selected, externally supplied VSYNC, HSYNC and PCLK signals drive the chip. Display data (DB[17:0]) is written in synchronization with those synchronous signals following data enable signal (DE). This enables updating image data without flicker on the panel.When VSYNC I/F is selected, the entire operation, except for synchronization with synchronous signal VSYNC, is in synchronization with internal clock. System interface is used when display data is written to the frame memory.

3. Address Counter (AC)

The address counter (AC) gives an address to the frame memory. Address information defined by CDR and PR is transferred to the AC. The AC is automatically updated plus or minus 1 as the R61516 writes/reads data to/from the frame memory. When VCYNC-I/F is selected, the R61516 operates totally in synchronization with internal clock, with only exception of VSYNC, the synchronous signal. Display data is written to the frame memory via conventional system interface.

4. Frame Memoery

The R61516 incorporates the frame memory that has a capacity of 172,800 bytes, which can store bit-pattern data of 240RGB x 320 graphics display at the maximum using 18 bits to represent one pixel.

5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltage according to the grayscale setting value in the γ-correction register. RGB separate gamma correction setting enables the maximum of 262,144-color display.

6. LCD Drive Power Supply Circuit

The LCD drive power supply circuit generates VREG, VGH, VGL and VCOM levels to drive the liquid crystal panel.

7. Timing Generator

The timing generator is used to generate timing signals for the operation of internal circuits such as frame memory. The timing signal for display operation such as frame memory read and frame memory access by host processor are generated separately so that the two do not interfere with each other.

8. Oscillator (OSC)

The R61516 incorporates RC oscillator. The frame frequency can be adjusted by command.

9. LCD Driver Circuit

The LCD driver circuit consists of a 720-channel source driver(S[1:720]). The display pattern data is latched when 240RGB pixels of data are input. The voltage is output from the source driver according to the latched data. The shift direction of source output can be changed by setting SS bit (C0h).

The gate driver circuit consists of a 320-channel gate driver (G[1:320]). The voltage at VGH level or VGL level is output from the gate driver. The shift direction of gate output can be changed by GS bit (C0h). The scan mode of the gate driver can be changed by setting SM bit (C0h) according to the mounting condition.

10. Internal Logic Power Supply Regulator

The internal logic power supply regulator generates power supply for internal logic circuit.

11. EEPROM interface circuit

EEPROM interface circuit is used to output/input interface signals SCS, SCL, SDI and SDO.

Pin Function

Table 4 External Power Supply

<table>
<tr><th>Signal</th><th>I/O</th><th>Connect to</th><th>Function</th><th>Unused pin</th></tr>
<tr><td>VCC</td><td>I</td><td>Power supply</td><td>Power supply to internal VDD regulator.
Vcc = 2.5V~3.3V. VCC ≥ IOVCC</td><td>-</td></tr>
<tr><td>IOVCC</td><td>I</td><td>Power supply</td><td>Power supply to interface pins.
IOVCC = 1.65V ~ 3.10V in MIPI DBI Type C operation.
Connect to the external power supplies above.</td><td>-</td></tr>
<tr><td>GND</td><td>I</td><td>Power supply</td><td>Internal logic GND and interface pin GND. GND = 0V.</td><td>-</td></tr>
<tr><td>VCI</td><td>I</td><td>Power supply</td><td>Power supply to liquid crystal power supply analog circuit.
VCI=2.5V ~ 3.3V.</td><td>-</td></tr>
<tr><td>VCILVL</td><td>I</td><td>Reference power supply</td><td>VCILVL must be at the same electrical potential as VCI.
VCILVL = 2.5V ~ 3.3V. Connect to external power supply.
Connect to VCI on the FPC to prevent in case of COG.</td><td>-</td></tr>
<tr><td>AGND</td><td>I</td><td>Power supply</td><td>Analog GND (logic regulator, LCD power supply circuit).
AGND = 0V. Connect to GND on the FPC to prevent noise in case of COG.</td><td>-</td></tr>
<tr><td>VPP1</td><td>I</td><td>Power supply</td><td rowspan="3">Power supply for Internal NVM. Apply voltage to VPP1, VPP2, and VPP3A according to the operation mode shown below.
<table>
<tr><th>Operation mode</th><th>VPP1</th><th>VPP2</th><th>VPP3A</th></tr>
<tr><td>NVM write</td><td>9.0±0.1V</td><td>7.5±0.1V</td><td>GND</td></tr>
<tr><td>NVM read</td><td>OPEN</td><td>OPEN</td><td>GND or OPEN</td></tr>
<tr><td>NVM erase</td><td>9.0±0.1V</td><td>9.0±0.1V</td><td>-9.0±0.1V</td></tr>
</table></td><td>AGND (Note 2)</td></tr>
<tr><td>VPP2</td><td>I</td><td>Power supply</td><td>AGND (Note 2)</td></tr>
<tr><td>VPP3A</td><td>I</td><td>Power supply</td><td>AGND (Note 2)</td></tr>
</table>

Note 1: VCC, GND and AGND pins are located on several places on the chip. Make sure to connect electrical potential to all of them as “Connection Example” instructs.

Note 2: When internal NVM is not used (namely no write or erase operation is executed), VPP1, VPP2 and VPP3A pins must be fixed at AGND.

Table 5 Bus Interface (Amplitude: IOVCC ~ GND)

Signal	I/O	Connect to	Function	Unused pin
CSX	I	Host Processor	Chip select signal. Low: Select (Accessible) High: Not select (Inaccessible) Make sure to connect to host processor. Follow AC timing to control the signal.	-
DCX	I	Host Processor	Command/data select signal Low: Select command High: Select data	-
WRX / SCL	I	Host Processor	Write strobe signal in DBI Type B operation. Write data when WRX is Low. Synchronoous clock signal in DBI Type C operation	-
RDX	I	Host Processor	Read strobe signal. Read out data when RDX is Low.	-
DIN	I	Host Processor	Serial data input pin in DBI Type C operation to input data on the rising edge of SCL sigal.	GND or IOVCC
DOUT	O	Host Processor	Serial data output pin in DBI Type C operation to input data on the falling edge of SCL sigal.	OPEN
DB[17:0]	I/O	Host Processor	18-bit bi-directional data bus in DBI Type B operation. 8-bit interface: Use DB[7:0] 9-bit interface: Use DB[8:0] 16-bit interface: Use DB[15:0] 18-bit interface: Use DB[17:0] Abnormal current (through current) is not conducted when CSX is High and the data bus is Hi-z. 18-bit input data bus in DPI operation. 16-bit interface: Use DB[15:0] 18-bit interface: Use DB[17:0]	GND or IOVCC
DE	I	Host Processor	Data enable signal in DPI operation. Low: Select (Accessible) High: Not select (Inaccessible)	GND or IOVCC
VSYNC	I	Host Processor	Frame synchronous signal. Low active.	GND or IOVCC
HSYNC	I	Host Processor	Line synchronous signal. Low active.	GND or IOVCC
PCLK	I	Host Processor	Pixel clock signal. The data input timing is set on the rising edge.	GND or IOVCC
TE	O	Host Processor	Tearing Effect output signal	OPEN
IM0-2	I	Host Processor	Interface select signal. Select interface from DBI Type B (18-/ 16-/ 9-/ 8- bit) and Type C (Option 1 / Option 3)	-
RESX	I	Host Processor or external RC oscillator	Reset pin. The R61516 is initialized when RESX is Low. Make sure to execute power-on reset when turning the power supply on.	-

PROTECTX	I	Host Processor	Reset protect pin. The R61516 enters Reset Protect satus and hardware reset is disabled when PROTECTX=GND. Errornous opertation caused by noise is prevented. Low: Hardware reset is disabled (Reset Protect status) High: Hardware reset is enabled (Normal status).	IOVCC

Table 6 External EEPROM interface (Amplitude: VCC-GND)

Signal	I/O	Connect to	Function	Unused pin
SCS	O	EEPROM	Selects EEPROM. Low: Not selected (Inaccessible) High: Selected (Accessible)	OPEN
SCL	O	EEPROM	Serial clock signal for EEPROM.	OPEN
SDI	I	EEPROM	Input signal for EEPROM. Used to input serial data.	VCC /GND
SDO	O	EEPROM	Output signal from EEPROM. Start bit, operational code, address and serial data are outputted.	OPEN
EEPROME	I	VCC/GND	Control pin for external EEPROM. Fix the potential on the FPC. High: External EEPROM is used. Low: External EEPROM is not used.	GND

Table 7 Step-up Circuit

Signal	I/O	Connect to	Function	Unused pin
VDD	I	Stabilizing capacitor	Output from internal logic regulator. Connect to stabilizing capacitor.	-
VCI1	I/O	Stabilizing capacitor	Reference voltage for the step-up circuit 1. Set VCI1 so that the output levels of VLOUT1/2/3 are in the respective setting ranges.	-
VLOUT1	O	Stabilizing capacitor, DDVDH	The output level from the step-up circuit 1, generated from VCI1 (x2).	-
DDVDH	I	VLOUT1	Source driver liquid crystal and VCOM drive power supply. Connect to VLOUT1.	-
VLOUT2	O	Stabilizing capacitor, VGH	The output level form the step-up circuit 2, generated from VCI1 and DDVDH. The output level is determined by the step-up factor, which is set by instruction (BT*).	-
VGH	I	LCD panel	LCD drive power supply. Connect to VLOUT2.	-
VLOUT3	O	Stabilizing capacitor, VGL	The output level form the step-up circuit 2, generated from VCI1 and DDVDH. The output level is determined by the step-up factor, which is set by instruction (BT*).	-
VGL	I	LCD panel	LCD drive power supply. Connect to VLOUT3.	-
VCL	I/O	Stabilizing capacitor	VCOML drive power supply.	-
C11P, C11M C12P, C12M	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.	-
C13P, C13M C21P, C21M, C22P, C22M	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.	-

Table 8 LCD Drive Power Supply

Signal	I/O	Connect to	Function	Unused pin
VREG	O	Stabilizing capacitor	The output level generated from VCIR. The output level is determined by the factor, which is set by instruction (VRH*). VREG serves as reference of (1) source driver grayscale, (2) VCOMH level and (3) VCOM width. Connect a stabilizing capacitor to use this pin. VREG = 4.0V ~ (DDVDH – 0.500)V	-
VCOM	O	TFT panel's common electrode	Power supply to TFT panel's common electrode. VCOM output level alternates between VCOMH and VCOML. The alternating cycle is set by a register. Also, the VCOM output can be started and halted by register setting.	-
VCOMOL	O	TFT panel's common electrode	Power supply to TFT panel's common electrode. VCOMOL and VCOMOR output alternating current at VCOMH – VCOML level. The pins are connected to VCOM output pin in the die. Use both VCOMOL and VCOMOR pins.	-
VCOMOR	O	TFT panel's common electrode		-
VCOMH	O	Stabilizing capacitor	VCOM High level, which is set by internal electronic volume VCM or VCOMR.	-
VCOML	O	Stabilizing capacitor	VCOM Low level, which is set by instruction (VDV). VCOML = (VCL + 0.5)V ~ 0V	-
VCOMR	I	Variable resistance or OPEN	Used when VCOMH is adjusted using external variable resistor. Connect variable resistance between VREG and GND.	OPEN
VGS	I	GND	Reference level of the grayscale voltage generating circuit.	-
S[1:720]	O	LCD panel	Liquid crystal application voltages.	OPEN
G[1:320]	O	LCD panel	Gate line output signals. VGH: gate line is selected VGL: gate line is not selected	OPEN

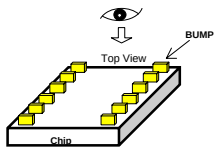
Table 9 Other pins (Test, Dummy)

Signal	I/O	Connect to	Function	Unused pin
VTEST	O	OPEN	Test pin. Leave it open.	OPEN
VREFC	I	GND	Test pin. Make sure to connecto to GND.	-
VREFD	O	OPEN	Test pin. Leave it open.	OPEN
VREF	O	OPEN	Test pin. Leave it open.	OPEN
VDDTEST	I	GND	Test pin. Make sure to connecto to GND.	-
VMON	O	OPEN	Test pin. Leave open.	OPEN
VCIR	O	OPEN	Test pin. Leave it open.	OPEN
GNDDUM[1:9], AGNDDUM[1:4], VCCDUM, IOVCCDUM[1:2]	O	-	Used to fix electrical potential by connecting unused I/F and test pins to these pins on the glass. Leave open when these dummy pins are not used.	OPEN
DUMMYR [1:8]	-	-	Short-circuited in the LSI to to measure COG contact resistance. DUMMYR1 and DUMMYR8, DUMMYR2 and DUMMYR7, DUMMYR3 and DUMMYR6, DUMMYR4 and DUMMYR5 are short-circuited.	OPEN
VGLDMY [1:4]	O	Unused gate line	Output VGL. Use to fix electrical potential of unused gate lines.	OPEN
TESTO[1:14]	O	-	Dummy pad. Leave open.	OPEN
TEST[1:5]	I	GND	Test pin. Connect to GND.	GND
TSC	I	GND	Test pin. Connect to GND.	GND
TS[0-8]	O	OPEN	Test pin. Leave open.	OPEN
VPP3B, C	I	AGND	Test pin. Connect to AGND.	-

Patents of dummy pin which is used to fix pin to VCC or GND are pending and granted.

PATENT ISSUED: United States Patent No. 6,323,930
PATENT PENDING: Japanese Application No. 10-514484
Korean Application No. 19997002322
Taiwanese Application No.086103756
(PCT/JP96/02728(W098/12597)

R61516 Pad Arrangement Rev 0.02



No			
1	DUMMYR1	TESTO14	
2	DUMMYR2	TESTO13	
3	AGNDDUM1	DUMMYR8	
4	VPP3C	DUMMYR7	
5	VPP3C	VGLDMY4	
6	VPP3B	G1	
7	VPP3B	G3	
8	AGNDDUM2	G5	
9	VPP3A	G7	
10	VPP3A		
11	VPP2		
12	VPP2		
13	VPP2		
14	VPP2		
15	VPP2		
16	VPP1		
17	VPP1		
18	GNDDUM1		
19	VDDTEST		
20	VREFC		
21	VREFD		
22	VREF		
23	VCCDUM		
24	EEPROME		
25	SCS		
26	SCL		
27	SDI		
28	SDO		
29	GNDDUM2		
30	AGND		
31	AGND		
32	AGND		
33	AGND		
34	AGND		
35	AGND		
36	GND		
37	GND		
38	GND		
39	GND		
40	GND		
41	VCC		
42	VCC		
43	VCC		
44	VCC		
45	VCC		
46	VCC		
47	VCC		
48	VCC		
49	VCC		
50	TS8		
51	TS7		
52	TS6		
53	TS5		
54	TS4		
55	TS3		
56	TS2		
57	TS1		
58	TS0		
59	TEST5		
60	TEST4		
61	TEST3		
62	TEST2		
63	TEST1	G315	
64	GNDDUM3	G317	
65	TSC	G319	
66	IM2	VGLDMY3	
67	IM1	TESTO12	
68	IM0		
69	IOVCCDUM1		
70	PROTECTX		
71	RESX	TESTO11	
72	VSYNC	VCOMOL	
73	HSYNC	VCOMOL	
74	IOVCCDUM2	VCOMOL	
75	DE	VCOMOL	
76	PCLK	VCOMOL	
77	DB17	TESTO10	
78	DB16		
79	GNDDUM4		
80	DB15		
81	DB14		
82	DB13	TESTO9	
83	DB12	S1	
84	GNDDUM5	S2	
85	DB11	S3	
86	DB10	S4	
87	DB9	S5	
88	IOVCC	S6	
89	IOVCC	S7	
90	IOVCC		
91	IOVCC		
92	IOVCC		
93	IOVCC		
94	IOVCC		
95	IOVCC		
96	DB8		
97	GNDDUM6		
98	DB7		
99	DB6		
100	DB5		
101	DB4		
102	GNDDUM7		
103	DB3		
104	DB2		
105	DB1		
106	DB0		
107	GNDDUM8		
108	CSX		
109	DCX		
110	WRX/SCL		
111	RDX		
112	GNDDUM9		
113	TE		
114	DBN		
115	DOUT		
116	VDD		
117	VDD		
118	VDD		
119	VDD		
120	VDD		
121	VDD		
122	VDD	S356	
123	VDD	S357	
124	VDD	S358	
125	VMON	S359	
126	VCOM	S360	
127	VCOM	TESTO8	
128	VCOM		
129	VCOM		
130	VCOM		
131	VCOM		
132	VCOMH		
133	VCOMH		
134	VCOMH	TESTO7	
135	VCOMH	S361	
136	VCOMH	S362	
137	VCOMH	S363	
138	VCOML	S364	
139	VCOML	S365	
140	VCOML	S366	
141	VCOML		
142	VCOML		
143	VCOML		
144	GND		
145	GND		
146	GND		
147	GND		
148	GND		
149	GND		
150	GND		
151	GND		
152	GND		
153	VGS		
154	AGND		
155	AGND		
156	AGND		
157	AGND		
158	AGND		
159	AGND		
160	AGND		
161	AGND		
162	AGND		
163	VTEST		
164	VCIR		
165	VREG		
166	VCOMR		
167	C11M		
168	C11M		
169	C11M		
170	C11M	S714	
171	C11M	S715	
172	C11P	S716	
173	C11P	S717	
174	C11P	S718	
175	C11P	S719	
176	C11P	S720	
177	C12M	TESTO6	
178	C12M		
179	C12M		
180	C12M		
181	C12M		
182	C12P	TESTO5	
183	C12P	VCOMOR	
184	C12P	VCOMOR	
185	C12P	VCOMOR	
186	C12P	VCOMOR	
187	VLOUT1	VCOMOR	
188	VLOUT1	TESTO4	
189	VLOUT1		
190	DDVDH		
191	DDVDH	TESTO3	
192	DDVDH	VGLDMY2	
193	DDVDH	G320	
194	DDVDH	G318	
195	DDVDH		
196	VCI1		
197	VCI1		
198	VCI1		
199	VCI1		
200	VCI		
201	VCI		
202	VCI		
203	VCI		
204	VCI		
205	VCI		
206	VCILVL		
207	VCC		
208	VCC		
209	VCC		
210	VCC		
211	VCC		
212	GND		
213	GND		
214	GND		
215	GND		
216	GND		
217	AGND		
218	AGND		
219	AGND		
220	AGND		
221	AGND		
222	VGL		
223	VGL		
224	VGL		
225	VGL		
226	VGL		
227	VGL		
228	VGL		
229	VGL		
230	VLOUT3		
231	VLOUT3		
232	AGNDDUM3		
233	VLOUT2		
234	VLOUT2		
235	VGH		
236	VGH		
237	VGH		
238	VGH		
239	AGNDDUM4		
240	VCL		
241	VCL		
242	VCL		
243	C13M		
244	C13M		
245	C13M		
246	C13P		
247	C13P		
248	C13P		
249	C21M		
250	C21M		
251	C21M		
252	C21P		
253	C21P	G8	
254	C21P	G6	
255	C22M	G4	
256	C22M	G2	
257	C22M	VGLDMY1	
258	C22P	DUMMYR6	
259	C22P	DUMMYR5	
260	C22P	TESTO2	
261	DUMMYR3	TESTO1	
262	DUMMYR4		

Bump space: 51um

51um

Bump space:88um

88um

Bump space: 68um

68um

Bump space: 51um

51um

●Chip size: 19.0mm x 0.99mm

●Chip thickness: 280μm (typ)

●Pad coordinate: Pad center

●Pad origin: Chip center

●Au bump size:

1. 50μm x 90μm (I/O side, No.1-262)
2. 17μm x 100μm (LCD output side, No.263-1334)

●Au bump pitch: See Pad Coordinate.

●Au bump height: 12μm

●Numbers referred to in the figures in this document correspond to the numbers in the Pa d Coordinates table.

●Alignment Mark (1-a), (1-b)

Alignment mark shape		X	Y
● Type A	(1-a)	-9366	-361
	(1-b)	9366	-361

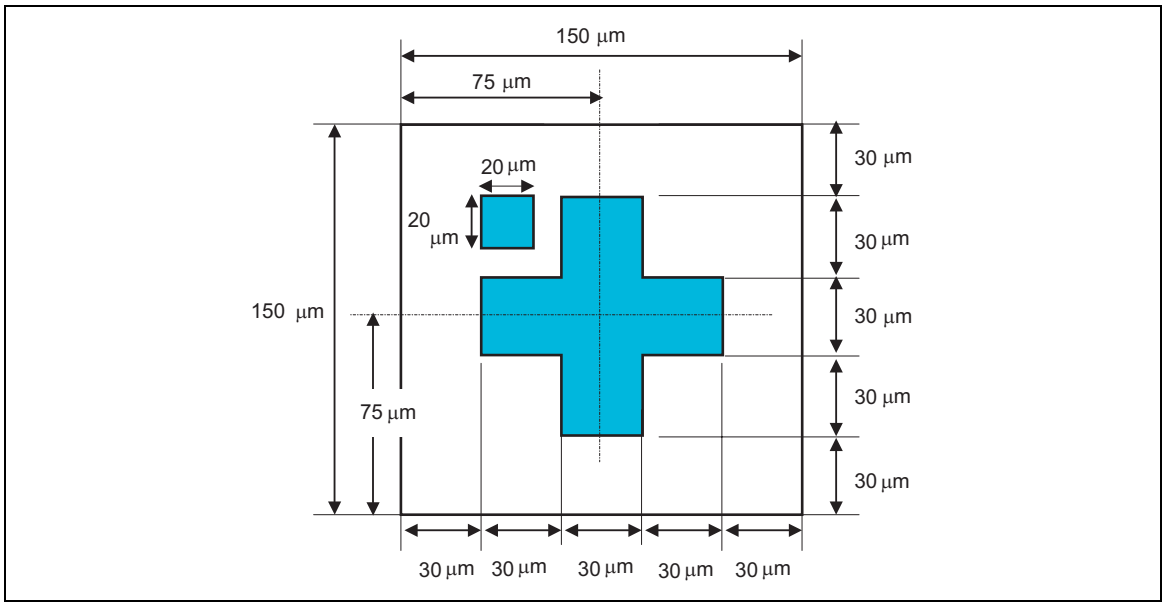


Figure 2

R61516 Pad Coordinate (unit:um)

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Pad No.	Pad Name	X	Y
1	DUMMYR1	-9135	-386
2	DUMMYR2	-9065	-386
3	AGNDDUM1	-8995	-386
4	VPP3C	-8925	-386
5	VPP3C	-8855	-386
6	VPP3B	-8785	-386
7	VPP3B	-8715	-386
8	AGNDDUM2	-8645	-386
9	VPP3A	-8575	-386
10	VPP3A	-8505	-386
11	VPP2	-8435	-386
12	VPP2	-8365	-386
13	VPP2	-8295	-386
14	VPP2	-8225	-386
15	VPP2	-8155	-386
16	VPP1	-8085	-386
17	VPP1	-8015	-386
18	GNDDUM1	-7945	-386
19	VDDTEST	-7875	-386
20	VREFC	-7805	-386
21	VREFD	-7735	-386
22	VREF	-7665	-386
23	VCCDUM	-7595	-386
24	EEPROME	-7525	-386
25	SCS	-7455	-386
26	SCL	-7385	-386
27	SDI	-7315	-386
28	SDO	-7245	-386
29	GNDDUM2	-7175	-386
30	AGND	-7105	-386
31	AGND	-7035	-386
32	AGND	-6965	-386
33	AGND	-6895	-386
34	AGND	-6825	-386
35	AGND	-6755	-386
36	GND	-6685	-386
37	GND	-6615	-386
38	GND	-6545	-386
39	GND	-6475	-386
40	GND	-6405	-386
41	VCC	-6335	-386
42	VCC	-6265	-386
43	VCC	-6195	-386
44	VCC	-6125	-386
45	VCC	-6055	-386
46	VCC	-5985	-386
47	VCC	-5915	-386
48	VCC	-5845	-386
49	VCC	-5775	-386
50	TS8	-5705	-386
51	TS7	-5635	-386
52	TS6	-5565	-386
53	TS5	-5495	-386
54	TS4	-5425	-386
55	TS3	-5355	-386
56	TS2	-5285	-386
57	TS1	-5215	-386
58	TS0	-5145	-386
59	TEST5	-5075	-386
60	TEST4	-5005	-386
61	TEST3	-4935	-386
62	TEST2	-4865	-386
63	TEST1	-4795	-386
64	GNDDUM3	-4725	-386
65	TSC	-4655	-386
66	IM2	-4585	-386
67	IM1	-4515	-386
68	IM0	-4445	-386
69	IOVCCDUM1	-4375	-386
70	PROTECTX	-4305	-386
71	RESX	-4235	-386
72	VSYNC	-4165	-386
73	HSYNC	-4095	-386
74	IOVCCDUM2	-4025	-386
75	DE	-3955	-386
76	PCLK	-3885	-386
77	DB17	-3815	-386
78	DB16	-3745	-386
79	GNDDUM4	-3675	-386
80	DB15	-3605	-386
81	DB14	-3535	-386
82	DB13	-3465	-386
83	DB12	-3395	-386
84	GNDDUM5	-3325	-386
85	DB11	-3255	-386
86	DB10	-3185	-386
87	DB9	-3115	-386
88	IOVCC	-3045	-386
89	IOVCC	-2975	-386
90	IOVCC	-2905	-386
91	IOVCC	-2835	-386
92	IOVCC	-2765	-386
93	IOVCC	-2695	-386
94	IOVCC	-2625	-386
95	IOVCC	-2555	-386
96	DB8	-2485	-386
97	GNDDUM6	-2415	-386
98	DB7	-2345	-386
99	DB6	-2275	-386
100	DB5	-2205	-386
101	DB4	-2135	-386
102	GNDDUM7	-2065	-386
103	DB3	-1995	-386
104	DB2	-1925	-386
105	DB1	-1855	-386
106	DB0	-1785	-386
107	GNDDUM8	-1715	-386
108	CSX	-1645	-386
109	DCX	-1575	-386
110	WRX/SCL	-1505	-386
111	RDX	-1435	-386
112	GNDDUM9	-1365	-386
113	TE	-1295	-386
114	DIN	-1225	-386
115	DOUT	-1155	-386
116	VDD	-1085	-386
117	VDD	-1015	-386
118	VDD	-945	-386
119	VDD	-875	-386
120	VDD	-805	-386
121	VDD	-735	-386
122	VDD	-665	-386
123	VDD	-595	-386
124	VDD	-525	-386
125	VMON	-455	-386
126	VCOM	-385	-386
127	VCOM	-315	-386
128	VCOM	-245	-386
129	VCOM	-175	-386
130	VCOM	-105	-386
131	VCOM	-35	-386
132	VCOMH	35	-386
133	VCOMH	105	-386
134	VCOMH	175	-386
135	VCOMH	245	-386
136	VCOMH	315	-386
137	VCOMH	385	-386
138	VCOML	455	-386
139	VCOML	525	-386
140	VCOML	595	-386
141	VCOML	665	-386
142	VCOML	735	-386
143	VCOML	805	-386
144	GND	875	-386
145	GND	945	-386
146	GND	1015	-386
147	GND	1085	-386
148	GND	1155	-386
149	GND	1225	-386
150	GND	1295	-386

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Pad No.	Pad Name	X	Y
151	GND	1365	-386
152	GND	1435	-386
153	VGS	1505	-386
154	AGND	1575	-386
155	AGND	1645	-386
156	AGND	1715	-386
157	AGND	1785	-386
158	AGND	1855	-386
159	AGND	1925	-386
160	AGND	1995	-386
161	AGND	2065	-386
162	AGND	2135	-386
163	VTEST	2205	-386
164	VCIR	2275	-386
165	VREG	2345	-386
166	VCOMR	2415	-386
167	C11M	2485	-386
168	C11M	2555	-386
169	C11M	2625	-386
170	C11M	2695	-386
171	C11M	2765	-386
172	C11P	2835	-386
173	C11P	2905	-386
174	C11P	2975	-386
175	C11P	3045	-386
176	C11P	3115	-386
177	C12M	3185	-386
178	C12M	3255	-386
179	C12M	3325	-386
180	C12M	3395	-386
181	C12M	3465	-386
182	C12P	3535	-386
183	C12P	3605	-386
184	C12P	3675	-386
185	C12P	3745	-386
186	C12P	3815	-386
187	VLOUT1	3885	-386
188	VLOUT1	3955	-386
189	VLOUT1	4025	-386
190	DDVDH	4095	-386
191	DDVDH	4165	-386
192	DDVDH	4235	-386
193	DDVDH	4305	-386
194	DDVDH	4375	-386
195	DDVDH	4445	-386
196	VCI1	4515	-386
197	VCI1	4585	-386
198	VCI1	4655	-386
199	VCI1	4725	-386
200	VCI	4795	-386

Pad No.	Pad Name	X	Y
201	VCI	4865	-386
202	VCI	4935	-386
203	VCI	5005	-386
204	VCI	5075	-386
205	VCI	5145	-386
206	VCILVL	5215	-386
207	VCC	5285	-386
208	VCC	5355	-386
209	VCC	5425	-386
210	VCC	5495	-386
211	VCC	5565	-386
212	GND	5635	-386
213	GND	5705	-386
214	GND	5775	-386
215	GND	5845	-386
216	GND	5915	-386
217	AGND	5985	-386
218	AGND	6055	-386
219	AGND	6125	-386
220	AGND	6195	-386
221	AGND	6265	-386
222	VGL	6335	-386
223	VGL	6405	-386
224	VGL	6475	-386
225	VGL	6545	-386
226	VGL	6615	-386
227	VGL	6685	-386
228	VGL	6755	-386
229	VGL	6825	-386
230	VLOUT3	6895	-386
231	VLOUT3	6965	-386
232	AGNDDUM3	7035	-386
233	VLOUT2	7105	-386
234	VLOUT2	7175	-386
235	VGH	7245	-386
236	VGH	7315	-386
237	VGH	7385	-386
238	VGH	7455	-386
239	AGNDDUM4	7525	-386
240	VCL	7595	-386
241	VCL	7665	-386
242	VCL	7735	-386
243	C13M	7805	-386
244	C13M	7875	-386
245	C13M	7945	-386
246	C13P	8015	-386
247	C13P	8085	-386
248	C13P	8155	-386
249	C21M	8225	-386
250	C21M	8295	-386

Pad No.	Pad Name	X	Y
251	C21M	8365	-386
252	C21P	8435	-386
253	C21P	8505	-386
254	C21P	8575	-386
255	C22M	8645	-386
256	C22M	8715	-386
257	C22M	8785	-386
258	C22P	8855	-386
259	C22P	8925	-386
260	C22P	8995	-386
261	DUMMYR3	9065	-386
262	DUMMYR4	9135	-386
263	TESTO1	9367	387
264	TESTO2	9350	262
265	DUMMYR5	9333	387
266	DUMMYR6	9316	262
267	VGLDMY1	9299	387
268	G2	9282	262
269	G4	9265	387
270	G6	9248	262
271	G8	9231	387
272	G10	9214	262
273	G12	9197	387
274	G14	9180	262
275	G16	9163	387
276	G18	9146	262
277	G20	9129	387
278	G22	9112	262
279	G24	9095	387
280	G26	9078	262
281	G28	9061	387
282	G30	9044	262
283	G32	9027	387
284	G34	9010	262
285	G36	8993	387
286	G38	8976	262
287	G40	8959	387
288	G42	8942	262
289	G44	8925	387
290	G46	8908	262
291	G48	8891	387
292	G50	8874	262
293	G52	8857	387
294	G54	8840	262
295	G56	8823	387
296	G58	8806	262
297	G60	8789	387
298	G62	8772	262
299	G64	8755	387
300	G66	8738	262

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Pad No.	Pad Name	X	Y
301	G68	8721	387
302	G70	8704	262
303	G72	8687	387
304	G74	8670	262
305	G76	8653	387
306	G78	8636	262
307	G80	8619	387
308	G82	8602	262
309	G84	8585	387
310	G86	8568	262
311	G88	8551	387
312	G90	8534	262
313	G92	8517	387
314	G94	8500	262
315	G96	8483	387
316	G98	8466	262
317	G100	8449	387
318	G102	8432	262
319	G104	8415	387
320	G106	8398	262
321	G108	8381	387
322	G110	8364	262
323	G112	8347	387
324	G114	8330	262
325	G116	8313	387
326	G118	8296	262
327	G120	8279	387
328	G122	8262	262
329	G124	8245	387
330	G126	8228	262
331	G128	8211	387
332	G130	8194	262
333	G132	8177	387
334	G134	8160	262
335	G136	8143	387
336	G138	8126	262
337	G140	8109	387
338	G142	8092	262
339	G144	8075	387
340	G146	8058	262
341	G148	8041	387
342	G150	8024	262
343	G152	8007	387
344	G154	7990	262
345	G156	7973	387
346	G158	7956	262
347	G160	7939	387
348	G162	7922	262
349	G164	7905	387
350	G166	7888	262
351	G168	7871	387
352	G170	7854	262
353	G172	7837	387
354	G174	7820	262
355	G176	7803	387
356	G178	7786	262
357	G180	7769	387
358	G182	7752	262
359	G184	7735	387
360	G186	7718	262
361	G188	7701	387
362	G190	7684	262
363	G192	7667	387
364	G194	7650	262
365	G196	7633	387
366	G198	7616	262
367	G200	7599	387
368	G202	7582	262
369	G204	7565	387
370	G206	7548	262
371	G208	7531	387
372	G210	7514	262
373	G212	7497	387
374	G214	7480	262
375	G216	7463	387
376	G218	7446	262
377	G220	7429	387
378	G222	7412	262
379	G224	7395	387
380	G226	7378	262
381	G228	7361	387
382	G230	7344	262
383	G232	7327	387
384	G234	7310	262
385	G236	7293	387
386	G238	7276	262
387	G240	7259	387
388	G242	7242	262
389	G244	7225	387
390	G246	7208	262
391	G248	7191	387
392	G250	7174	262
393	G252	7157	387
394	G254	7140	262
395	G256	7123	387
396	G258	7106	262
397	G260	7089	387
398	G262	7072	262
399	G264	7055	387
400	G266	7038	262
401	G268	7021	387
402	G270	7004	262
403	G272	6987	387
404	G274	6970	262
405	G276	6953	387
406	G278	6936	262
407	G280	6919	387
408	G282	6902	262
409	G284	6885	387
410	G286	6868	262
411	G288	6851	387
412	G290	6834	262
413	G292	6817	387
414	G294	6800	262
415	G296	6783	387
416	G298	6766	262
417	G300	6749	387
418	G302	6732	262
419	G304	6715	387
420	G306	6698	262
421	G308	6681	387
422	G310	6664	262
423	G312	6647	387
424	G314	6630	262
425	G316	6613	387
426	G318	6596	262
427	G320	6579	387
428	VGLDMY2	6562	262
429	TESTO3	6545	387
430	TESTO4	6477	387
431	VCOMOR	6460	262
432	VCOMOR	6443	387
433	VCOMOR	6426	262
434	VCOMOR	6409	387
435	VCOMOR	6392	262
436	TESTO5	6375	387
437	TESTO6	6290	262
438	S720	6273	387
439	S719	6256	262
440	S718	6239	387
441	S717	6222	262
442	S716	6205	387
443	S715	6188	262
444	S714	6171	387
445	S713	6154	262
446	S712	6137	387
447	S711	6120	262
448	S710	6103	387
449	S709	6086	262
450	S708	6069	387

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Pad No.	Pad Name	X	Y
451	S707	6052	262
452	S706	6035	387
453	S705	6018	262
454	S704	6001	387
455	S703	5984	262
456	S702	5967	387
457	S701	5950	262
458	S700	5933	387
459	S699	5916	262
460	S698	5899	387
461	S697	5882	262
462	S696	5865	387
463	S695	5848	262
464	S694	5831	387
465	S693	5814	262
466	S692	5797	387
467	S691	5780	262
468	S690	5763	387
469	S689	5746	262
470	S688	5729	387
471	S687	5712	262
472	S686	5695	387
473	S685	5678	262
474	S684	5661	387
475	S683	5644	262
476	S682	5627	387
477	S681	5610	262
478	S680	5593	387
479	S679	5576	262
480	S678	5559	387
481	S677	5542	262
482	S676	5525	387
483	S675	5508	262
484	S674	5491	387
485	S673	5474	262
486	S672	5457	387
487	S671	5440	262
488	S670	5423	387
489	S669	5406	262
490	S668	5389	387
491	S667	5372	262
492	S666	5355	387
493	S665	5338	262
494	S664	5321	387
495	S663	5304	262
496	S662	5287	387
497	S661	5270	262
498	S660	5253	387
499	S659	5236	262
500	S658	5219	387

Pad No.	Pad Name	X	Y
501	S657	5202	262
502	S656	5185	387
503	S655	5168	262
504	S654	5151	387
505	S653	5134	262
506	S652	5117	387
507	S651	5100	262
508	S650	5083	387
509	S649	5066	262
510	S648	5049	387
511	S647	5032	262
512	S646	5015	387
513	S645	4998	262
514	S644	4981	387
515	S643	4964	262
516	S642	4947	387
517	S641	4930	262
518	S640	4913	387
519	S639	4896	262
520	S638	4879	387
521	S637	4862	262
522	S636	4845	387
523	S635	4828	262
524	S634	4811	387
525	S633	4794	262
526	S632	4777	387
527	S631	4760	262
528	S630	4743	387
529	S629	4726	262
530	S628	4709	387
531	S627	4692	262
532	S626	4675	387
533	S625	4658	262
534	S624	4641	387
535	S623	4624	262
536	S622	4607	387
537	S621	4590	262
538	S620	4573	387
539	S619	4556	262
540	S618	4539	387
541	S617	4522	262
542	S616	4505	387
543	S615	4488	262
544	S614	4471	387
545	S613	4454	262
546	S612	4437	387
547	S611	4420	262
548	S610	4403	387
549	S609	4386	262
550	S608	4369	387

Pad No.	Pad Name	X	Y
551	S607	4352	262
552	S606	4335	387
553	S605	4318	262
554	S604	4301	387
555	S603	4284	262
556	S602	4267	387
557	S601	4250	262
558	S600	4233	387
559	S599	4216	262
560	S598	4199	387
561	S597	4182	262
562	S596	4165	387
563	S595	4148	262
564	S594	4131	387
565	S593	4114	262
566	S592	4097	387
567	S591	4080	262
568	S590	4063	387
569	S589	4046	262
570	S588	4029	387
571	S587	4012	262
572	S586	3995	387
573	S585	3978	262
574	S584	3961	387
575	S583	3944	262
576	S582	3927	387
577	S581	3910	262
578	S580	3893	387
579	S579	3876	262
580	S578	3859	387
581	S577	3842	262
582	S576	3825	387
583	S575	3808	262
584	S574	3791	387
585	S573	3774	262
586	S572	3757	387
587	S571	3740	262
588	S570	3723	387
589	S569	3706	262
590	S568	3689	387
591	S567	3672	262
592	S566	3655	387
593	S565	3638	262
594	S564	3621	387
595	S563	3604	262
596	S562	3587	387
597	S561	3570	262
598	S560	3553	387
599	S559	3536	262
600	S558	3519	387

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Pad No.	Pad Name	X	Y
601	S557	3502	262
602	S556	3485	387
603	S555	3468	262
604	S554	3451	387
605	S553	3434	262
606	S552	3417	387
607	S551	3400	262
608	S550	3383	387
609	S549	3366	262
610	S548	3349	387
611	S547	3332	262
612	S546	3315	387
613	S545	3298	262
614	S544	3281	387
615	S543	3264	262
616	S542	3247	387
617	S541	3230	262
618	S540	3213	387
619	S539	3196	262
620	S538	3179	387
621	S537	3162	262
622	S536	3145	387
623	S535	3128	262
624	S534	3111	387
625	S533	3094	262
626	S532	3077	387
627	S531	3060	262
628	S530	3043	387
629	S529	3026	262
630	S528	3009	387
631	S527	2992	262
632	S526	2975	387
633	S525	2958	262
634	S524	2941	387
635	S523	2924	262
636	S522	2907	387
637	S521	2890	262
638	S520	2873	387
639	S519	2856	262
640	S518	2839	387
641	S517	2822	262
642	S516	2805	387
643	S515	2788	262
644	S514	2771	387
645	S513	2754	262
646	S512	2737	387
647	S511	2720	262
648	S510	2703	387
649	S509	2686	262
650	S508	2669	387

Pad No.	Pad Name	X	Y
651	S507	2652	262
652	S506	2635	387
653	S505	2618	262
654	S504	2601	387
655	S503	2584	262
656	S502	2567	387
657	S501	2550	262
658	S500	2533	387
659	S499	2516	262
660	S498	2499	387
661	S497	2482	262
662	S496	2465	387
663	S495	2448	262
664	S494	2431	387
665	S493	2414	262
666	S492	2397	387
667	S491	2380	262
668	S490	2363	387
669	S489	2346	262
670	S488	2329	387
671	S487	2312	262
672	S486	2295	387
673	S485	2278	262
674	S484	2261	387
675	S483	2244	262
676	S482	2227	387
677	S481	2210	262
678	S480	2193	387
679	S479	2176	262
680	S478	2159	387
681	S477	2142	262
682	S476	2125	387
683	S475	2108	262
684	S474	2091	387
685	S473	2074	262
686	S472	2057	387
687	S471	2040	262
688	S470	2023	387
689	S469	2006	262
690	S468	1989	387
691	S467	1972	262
692	S466	1955	387
693	S465	1938	262
694	S464	1921	387
695	S463	1904	262
696	S462	1887	387
697	S461	1870	262
698	S460	1853	387
699	S459	1836	262
700	S458	1819	387

Pad No.	Pad Name	X	Y
701	S457	1802	262
702	S456	1785	387
703	S455	1768	262
704	S454	1751	387
705	S453	1734	262
706	S452	1717	387
707	S451	1700	262
708	S450	1683	387
709	S449	1666	262
710	S448	1649	387
711	S447	1632	262
712	S446	1615	387
713	S445	1598	262
714	S444	1581	387
715	S443	1564	262
716	S442	1547	387
717	S441	1530	262
718	S440	1513	387
719	S439	1496	262
720	S438	1479	387
721	S437	1462	262
722	S436	1445	387
723	S435	1428	262
724	S434	1411	387
725	S433	1394	262
726	S432	1377	387
727	S431	1360	262
728	S430	1343	387
729	S429	1326	262
730	S428	1309	387
731	S427	1292	262
732	S426	1275	387
733	S425	1258	262
734	S424	1241	387
735	S423	1224	262
736	S422	1207	387
737	S421	1190	262
738	S420	1173	387
739	S419	1156	262
740	S418	1139	387
741	S417	1122	262
742	S416	1105	387
743	S415	1088	262
744	S414	1071	387
745	S413	1054	262
746	S412	1037	387
747	S411	1020	262
748	S410	1003	387
749	S409	986	262
750	S408	969	387

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Pad No.	Pad Name	X	Y
751	S407	952	262
752	S406	935	387
753	S405	918	262
754	S404	901	387
755	S403	884	262
756	S402	867	387
757	S401	850	262
758	S400	833	387
759	S399	816	262
760	S398	799	387
761	S397	782	262
762	S396	765	387
763	S395	748	262
764	S394	731	387
765	S393	714	262
766	S392	697	387
767	S391	680	262
768	S390	663	387
769	S389	646	262
770	S388	629	387
771	S387	612	262
772	S386	595	387
773	S385	578	262
774	S384	561	387
775	S383	544	262
776	S382	527	387
777	S381	510	262
778	S380	493	387
779	S379	476	262
780	S378	459	387
781	S377	442	262
782	S376	425	387
783	S375	408	262
784	S374	391	387
785	S373	374	262
786	S372	357	387
787	S371	340	262
788	S370	323	387
789	S369	306	262
790	S368	289	387
791	S367	272	262
792	S366	255	387
793	S365	238	262
794	S364	221	387
795	S363	204	262
796	S362	187	387
797	S361	170	262
798	TESTO7	153	387
799	TESTO8	−153	387
800	S360	−170	262

Pad No.	Pad Name	X	Y
801	S359	−187	387
802	S358	−204	262
803	S357	−221	387
804	S356	−238	262
805	S355	−255	387
806	S354	−272	262
807	S353	−289	387
808	S352	−306	262
809	S351	−323	387
810	S350	−340	262
811	S349	−357	387
812	S348	−374	262
813	S347	−391	387
814	S346	−408	262
815	S345	−425	387
816	S344	−442	262
817	S343	−459	387
818	S342	−476	262
819	S341	−493	387
820	S340	−510	262
821	S339	−527	387
822	S338	−544	262
823	S337	−561	387
824	S336	−578	262
825	S335	−595	387
826	S334	−612	262
827	S333	−629	387
828	S332	−646	262
829	S331	−663	387
830	S330	−680	262
831	S329	−697	387
832	S328	−714	262
833	S327	−731	387
834	S326	−748	262
835	S325	−765	387
836	S324	−782	262
837	S323	−799	387
838	S322	−816	262
839	S321	−833	387
840	S320	−850	262
841	S319	−867	387
842	S318	−884	262
843	S317	−901	387
844	S316	−918	262
845	S315	−935	387
846	S314	−952	262
847	S313	−969	387
848	S312	−986	262
849	S311	−1003	387
850	S310	−1020	262

Pad No.	Pad Name	X	Y
851	S309	−1037	387
852	S308	−1054	262
853	S307	−1071	387
854	S306	−1088	262
855	S305	−1105	387
856	S304	−1122	262
857	S303	−1139	387
858	S302	−1156	262
859	S301	−1173	387
860	S300	−1190	262
861	S299	−1207	387
862	S298	−1224	262
863	S297	−1241	387
864	S296	−1258	262
865	S295	−1275	387
866	S294	−1292	262
867	S293	−1309	387
868	S292	−1326	262
869	S291	−1343	387
870	S290	−1360	262
871	S289	−1377	387
872	S288	−1394	262
873	S287	−1411	387
874	S286	−1428	262
875	S285	−1445	387
876	S284	−1462	262
877	S283	−1479	387
878	S282	−1496	262
879	S281	−1513	387
880	S280	−1530	262
881	S279	−1547	387
882	S278	−1564	262
883	S277	−1581	387
884	S276	−1598	262
885	S275	−1615	387
886	S274	−1632	262
887	S273	−1649	387
888	S272	−1666	262
889	S271	−1683	387
890	S270	−1700	262
891	S269	−1717	387
892	S268	−1734	262
893	S267	−1751	387
894	S266	−1768	262
895	S265	−1785	387
896	S264	−1802	262
897	S263	−1819	387
898	S262	−1836	262
899	S261	−1853	387
900	S260	−1870	262

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Pad No.	Pad Name	X	Y
901	S259	-1887	387
902	S258	-1904	262
903	S257	-1921	387
904	S256	-1938	262
905	S255	-1955	387
906	S254	-1972	262
907	S253	-1989	387
908	S252	-2006	262
909	S251	-2023	387
910	S250	-2040	262
911	S249	-2057	387
912	S248	-2074	262
913	S247	-2091	387
914	S246	-2108	262
915	S245	-2125	387
916	S244	-2142	262
917	S243	-2159	387
918	S242	-2176	262
919	S241	-2193	387
920	S240	-2210	262
921	S239	-2227	387
922	S238	-2244	262
923	S237	-2261	387
924	S236	-2278	262
925	S235	-2295	387
926	S234	-2312	262
927	S233	-2329	387
928	S232	-2346	262
929	S231	-2363	387
930	S230	-2380	262
931	S229	-2397	387
932	S228	-2414	262
933	S227	-2431	387
934	S226	-2448	262
935	S225	-2465	387
936	S224	-2482	262
937	S223	-2499	387
938	S222	-2516	262
939	S221	-2533	387
940	S220	-2550	262
941	S219	-2567	387
942	S218	-2584	262
943	S217	-2601	387
944	S216	-2618	262
945	S215	-2635	387
946	S214	-2652	262
947	S213	-2669	387
948	S212	-2686	262
949	S211	-2703	387
950	S210	-2720	262

Pad No.	Pad Name	X	Y
951	S209	-2737	387
952	S208	-2754	262
953	S207	-2771	387
954	S206	-2788	262
955	S205	-2805	387
956	S204	-2822	262
957	S203	-2839	387
958	S202	-2856	262
959	S201	-2873	387
960	S200	-2890	262
961	S199	-2907	387
962	S198	-2924	262
963	S197	-2941	387
964	S196	-2958	262
965	S195	-2975	387
966	S194	-2992	262
967	S193	-3009	387
968	S192	-3026	262
969	S191	-3043	387
970	S190	-3060	262
971	S189	-3077	387
972	S188	-3094	262
973	S187	-3111	387
974	S186	-3128	262
975	S185	-3145	387
976	S184	-3162	262
977	S183	-3179	387
978	S182	-3196	262
979	S181	-3213	387
980	S180	-3230	262
981	S179	-3247	387
982	S178	-3264	262
983	S177	-3281	387
984	S176	-3298	262
985	S175	-3315	387
986	S174	-3332	262
987	S173	-3349	387
988	S172	-3366	262
989	S171	-3383	387
990	S170	-3400	262
991	S169	-3417	387
992	S168	-3434	262
993	S167	-3451	387
994	S166	-3468	262
995	S165	-3485	387
996	S164	-3502	262
997	S163	-3519	387
998	S162	-3536	262
999	S161	-3553	387
1000	S160	-3570	262

Pad No.	Pad Name	X	Y
1001	S159	-3587	387
1002	S158	-3604	262
1003	S157	-3621	387
1004	S156	-3638	262
1005	S155	-3655	387
1006	S154	-3672	262
1007	S153	-3689	387
1008	S152	-3706	262
1009	S151	-3723	387
1010	S150	-3740	262
1011	S149	-3757	387
1012	S148	-3774	262
1013	S147	-3791	387
1014	S146	-3808	262
1015	S145	-3825	387
1016	S144	-3842	262
1017	S143	-3859	387
1018	S142	-3876	262
1019	S141	-3893	387
1020	S140	-3910	262
1021	S139	-3927	387
1022	S138	-3944	262
1023	S137	-3961	387
1024	S136	-3978	262
1025	S135	-3995	387
1026	S134	-4012	262
1027	S133	-4029	387
1028	S132	-4046	262
1029	S131	-4063	387
1030	S130	-4080	262
1031	S129	-4097	387
1032	S128	-4114	262
1033	S127	-4131	387
1034	S126	-4148	262
1035	S125	-4165	387
1036	S124	-4182	262
1037	S123	-4199	387
1038	S122	-4216	262
1039	S121	-4233	387
1040	S120	-4250	262
1041	S119	-4267	387
1042	S118	-4284	262
1043	S117	-4301	387
1044	S116	-4318	262
1045	S115	-4335	387
1046	S114	-4352	262
1047	S113	-4369	387
1048	S112	-4386	262
1049	S111	-4403	387
1050	S110	-4420	262

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Pad No.	Pad Name	X	Y
1051	S109	-4437	387
1052	S108	-4454	262
1053	S107	-4471	387
1054	S106	-4488	262
1055	S105	-4505	387
1056	S104	-4522	262
1057	S103	-4539	387
1058	S102	-4556	262
1059	S101	-4573	387
1060	S100	-4590	262
1061	S99	-4607	387
1062	S98	-4624	262
1063	S97	-4641	387
1064	S96	-4658	262
1065	S95	-4675	387
1066	S94	-4692	262
1067	S93	-4709	387
1068	S92	-4726	262
1069	S91	-4743	387
1070	S90	-4760	262
1071	S89	-4777	387
1072	S88	-4794	262
1073	S87	-4811	387
1074	S86	-4828	262
1075	S85	-4845	387
1076	S84	-4862	262
1077	S83	-4879	387
1078	S82	-4896	262
1079	S81	-4913	387
1080	S80	-4930	262
1081	S79	-4947	387
1082	S78	-4964	262
1083	S77	-4981	387
1084	S76	-4998	262
1085	S75	-5015	387
1086	S74	-5032	262
1087	S73	-5049	387
1088	S72	-5066	262
1089	S71	-5083	387
1090	S70	-5100	262
1091	S69	-5117	387
1092	S68	-5134	262
1093	S67	-5151	387
1094	S66	-5168	262
1095	S65	-5185	387
1096	S64	-5202	262
1097	S63	-5219	387
1098	S62	-5236	262
1099	S61	-5253	387
1100	S60	-5270	262

Pad No.	Pad Name	X	Y
1101	S59	-5287	387
1102	S58	-5304	262
1103	S57	-5321	387
1104	S56	-5338	262
1105	S55	-5355	387
1106	S54	-5372	262
1107	S53	-5389	387
1108	S52	-5406	262
1109	S51	-5423	387
1110	S50	-5440	262
1111	S49	-5457	387
1112	S48	-5474	262
1113	S47	-5491	387
1114	S46	-5508	262
1115	S45	-5525	387
1116	S44	-5542	262
1117	S43	-5559	387
1118	S42	-5576	262
1119	S41	-5593	387
1120	S40	-5610	262
1121	S39	-5627	387
1122	S38	-5644	262
1123	S37	-5661	387
1124	S36	-5678	262
1125	S35	-5695	387
1126	S34	-5712	262
1127	S33	-5729	387
1128	S32	-5746	262
1129	S31	-5763	387
1130	S30	-5780	262
1131	S29	-5797	387
1132	S28	-5814	262
1133	S27	-5831	387
1134	S26	-5848	262
1135	S25	-5865	387
1136	S24	-5882	262
1137	S23	-5899	387
1138	S22	-5916	262
1139	S21	-5933	387
1140	S20	-5950	262
1141	S19	-5967	387
1142	S18	-5984	262
1143	S17	-6001	387
1144	S16	-6018	262
1145	S15	-6035	387
1146	S14	-6052	262
1147	S13	-6069	387
1148	S12	-6086	262
1149	S11	-6103	387
1150	S10	-6120	262

Pad No.	Pad Name	X	Y
1151	S9	-6137	387
1152	S8	-6154	262
1153	S7	-6171	387
1154	S6	-6188	262
1155	S5	-6205	387
1156	S4	-6222	262
1157	S3	-6239	387
1158	S2	-6256	262
1159	S1	-6273	387
1160	TESTO9	-6290	262
1161	TESTO10	-6375	387
1162	VCOMOL	-6392	262
1163	VCOMOL	-6409	387
1164	VCOMOL	-6426	262
1165	VCOMOL	-6443	387
1166	VCOMOL	-6460	262
1167	TESTO11	-6477	387
1168	TESTO12	-6545	387
1169	VGLDMY3	-6562	262
1170	G319	-6579	387
1171	G317	-6596	262
1172	G315	-6613	387
1173	G313	-6630	262
1174	G311	-6647	387
1175	G309	-6664	262
1176	G307	-6681	387
1177	G305	-6698	262
1178	G303	-6715	387
1179	G301	-6732	262
1180	G299	-6749	387
1181	G297	-6766	262
1182	G295	-6783	387
1183	G293	-6800	262
1184	G291	-6817	387
1185	G289	-6834	262
1186	G287	-6851	387
1187	G285	-6868	262
1188	G283	-6885	387
1189	G281	-6902	262
1190	G279	-6919	387
1191	G277	-6936	262
1192	G275	-6953	387
1193	G273	-6970	262
1194	G271	-6987	387
1195	G269	-7004	262
1196	G267	-7021	387
1197	G265	-7038	262
1198	G263	-7055	387
1199	G261	-7072	262
1200	G259	-7089	387

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Pad No.	Pad Name	X	Y
1201	G257	-7106	262
1202	G255	-7123	387
1203	G253	-7140	262
1204	G251	-7157	387
1205	G249	-7174	262
1206	G247	-7191	387
1207	G245	-7208	262
1208	G243	-7225	387
1209	G241	-7242	262
1210	G239	-7259	387
1211	G237	-7276	262
1212	G235	-7293	387
1213	G233	-7310	262
1214	G231	-7327	387
1215	G229	-7344	262
1216	G227	-7361	387
1217	G225	-7378	262
1218	G223	-7395	387
1219	G221	-7412	262
1220	G219	-7429	387
1221	G217	-7446	262
1222	G215	-7463	387
1223	G213	-7480	262
1224	G211	-7497	387
1225	G209	-7514	262
1226	G207	-7531	387
1227	G205	-7548	262
1228	G203	-7565	387
1229	G201	-7582	262
1230	G199	-7599	387
1231	G197	-7616	262
1232	G195	-7633	387
1233	G193	-7650	262
1234	G191	-7667	387
1235	G189	-7684	262
1236	G187	-7701	387
1237	G185	-7718	262
1238	G183	-7735	387
1239	G181	-7752	262
1240	G179	-7769	387
1241	G177	-7786	262
1242	G175	-7803	387
1243	G173	-7820	262
1244	G171	-7837	387
1245	G169	-7854	262
1246	G167	-7871	387
1247	G165	-7888	262
1248	G163	-7905	387
1249	G161	-7922	262
1250	G159	-7939	387

Pad No.	Pad Name	X	Y
1251	G157	-7956	262
1252	G155	-7973	387
1253	G153	-7990	262
1254	G151	-8007	387
1255	G149	-8024	262
1256	G147	-8041	387
1257	G145	-8058	262
1258	G143	-8075	387
1259	G141	-8092	262
1260	G139	-8109	387
1261	G137	-8126	262
1262	G135	-8143	387
1263	G133	-8160	262
1264	G131	-8177	387
1265	G129	-8194	262
1266	G127	-8211	387
1267	G125	-8228	262
1268	G123	-8245	387
1269	G121	-8262	262
1270	G119	-8279	387
1271	G117	-8296	262
1272	G115	-8313	387
1273	G113	-8330	262
1274	G111	-8347	387
1275	G109	-8364	262
1276	G107	-8381	387
1277	G105	-8398	262
1278	G103	-8415	387
1279	G101	-8432	262
1280	G99	-8449	387
1281	G97	-8466	262
1282	G95	-8483	387
1283	G93	-8500	262
1284	G91	-8517	387
1285	G89	-8534	262
1286	G87	-8551	387
1287	G85	-8568	262
1288	G83	-8585	387
1289	G81	-8602	262
1290	G79	-8619	387
1291	G77	-8636	262
1292	G75	-8653	387
1293	G73	-8670	262
1294	G71	-8687	387
1295	G69	-8704	262
1296	G67	-8721	387
1297	G65	-8738	262
1298	G63	-8755	387
1299	G61	-8772	262
1300	G59	-8789	387

Pad No.	Pad Name	X	Y
1301	G57	-8806	262
1302	G55	-8823	387
1303	G53	-8840	262
1304	G51	-8857	387
1305	G49	-8874	262
1306	G47	-8891	387
1307	G45	-8908	262
1308	G43	-8925	387
1309	G41	-8942	262
1310	G39	-8959	387
1311	G37	-8976	262
1312	G35	-8993	387
1313	G33	-9010	262
1314	G31	-9027	387
1315	G29	-9044	262
1316	G27	-9061	387
1317	G25	-9078	262
1318	G23	-9095	387
1319	G21	-9112	262
1320	G19	-9129	387
1321	G17	-9146	262
1322	G15	-9163	387
1323	G13	-9180	262
1324	G11	-9197	387
1325	G9	-9214	262
1326	G7	-9231	387
1327	G5	-9248	262
1328	G3	-9265	387
1329	G1	-9282	262
1330	VGLDMY4	-9299	387
1331	DUMMYR7	-9316	262
1332	DUMMYR8	-9333	387
1333	TESTO13	-9350	262
1334	TESTO14	-9367	387

BUMP Arrangement

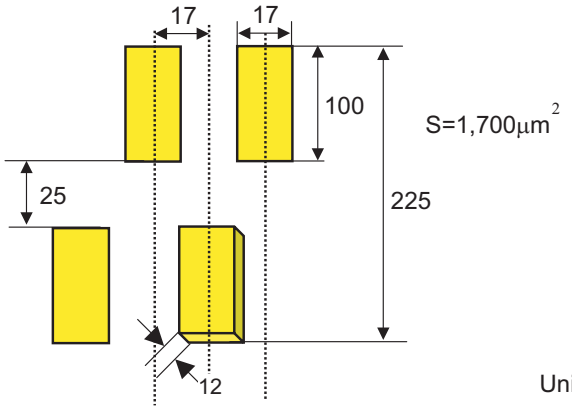
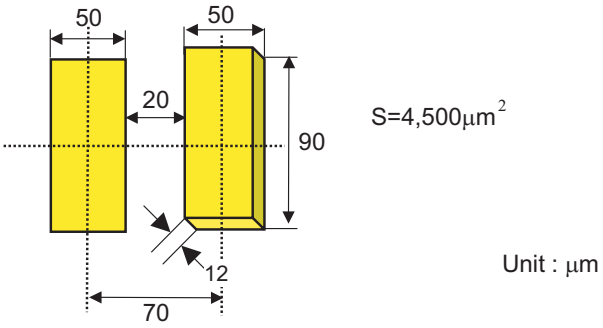
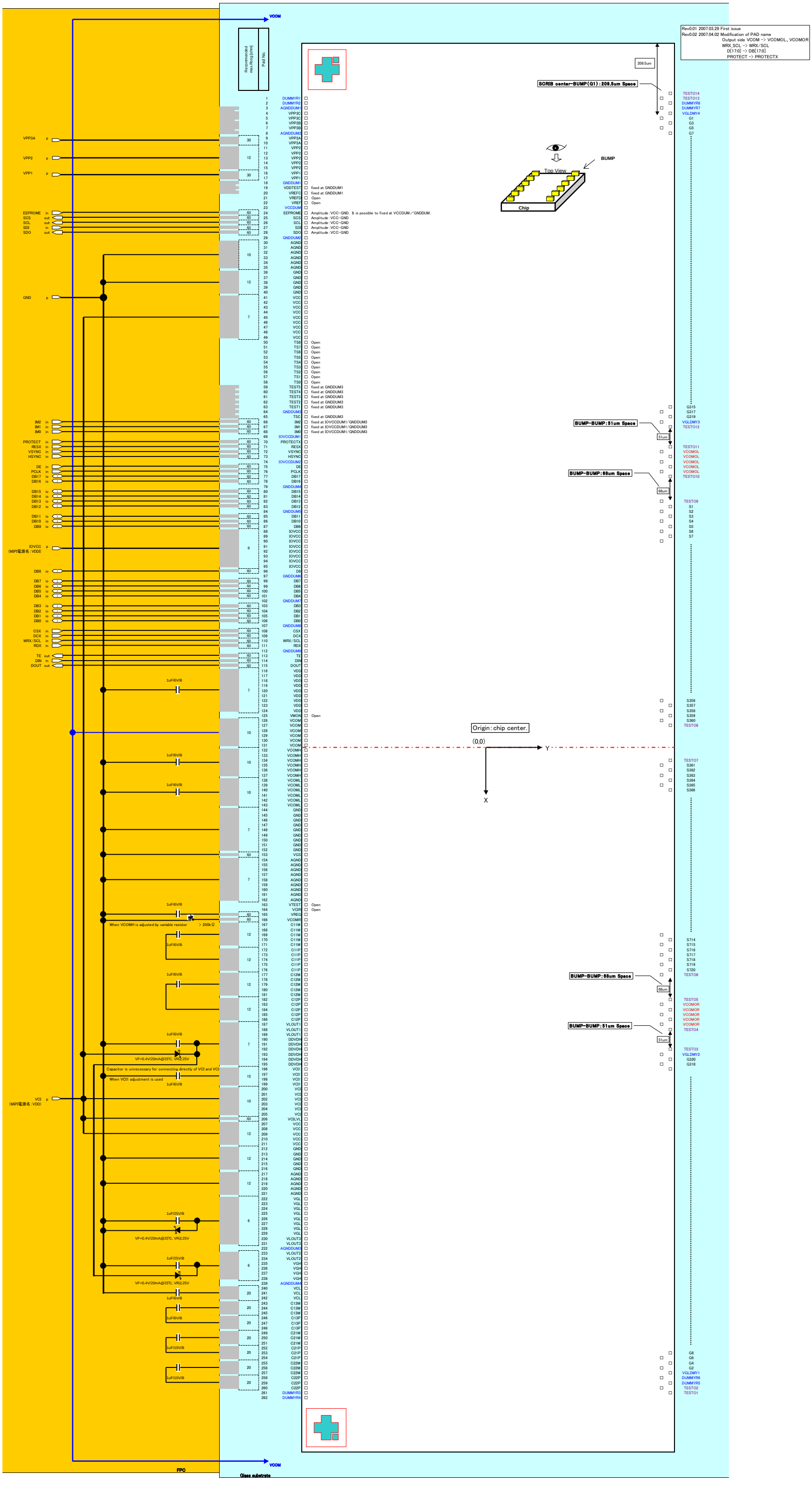
S1 ~ S720 G1 ~ G320 VCOMOL/R, VGLDMY1-4, DUMMYR1-8 TESTO1-14 (No263 ~ 1334)	
I/O pins (No. 1~262)	

Figure 3


VOOM
Recommended max.Rcog (ohm)
Pad No.
Rev0.01 2007.03.29 First issue
Rev0.02 2007.04.02 Modification of PAD name
Output side VCOM -> VCOMOL, VCOMOR
WRX_SCL -> WRX/SCL
D[17:0] -> DB[17:0]
PROTECT -> PROTECTX
209.5um
SCRIB center-BUMP(G1):209.5um Space
BUMP
Top View
Chip
BUMP-BUMP:51um Space
BUMP-BUMP:68um Space
BUMP-BUMP:68um Space
BUMP-BUMP:51um Space
51um
68um
68um
51um
Origin:chip center.
(0,0)
X
Y
When VCOMH is adjusted by variable resistor > 200kΩ
Capacitor is unnecessary for connecting directly of VCI and VCI1
When VCI1 adjustment is used
VF<0.4V/20mA@25℃, VR≧25V
FPC
Glass substrate
VCOM

System Interface (Display Bus Interface, DBI)

DBI Type B

Outline

The R61516 adopts 18-/16-/ 9-/ 8-bit bus display command interface to interface to high-performance host processor. The R61516 starts internal processing after storing control information of externally sent 18-/16-/ 9-/ 8-bit data in the command register (CDR) and the parameter register (PR). Since the internal operation of the R61516 is determined by signals sent from the host processor, command/parameter signal, read/write status signal (RDX/WRX), and internal 18-bit data bus signals (DB[17:0]) are called command.

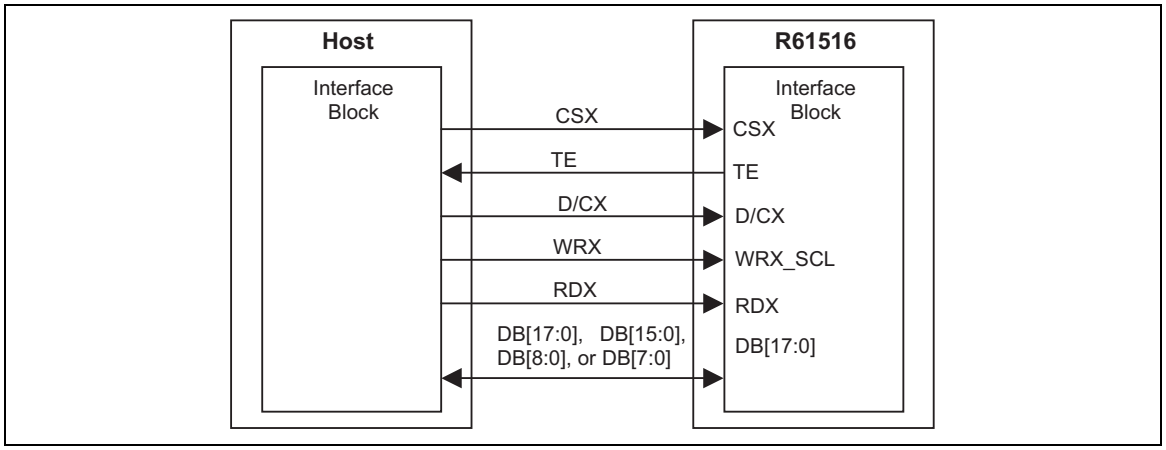


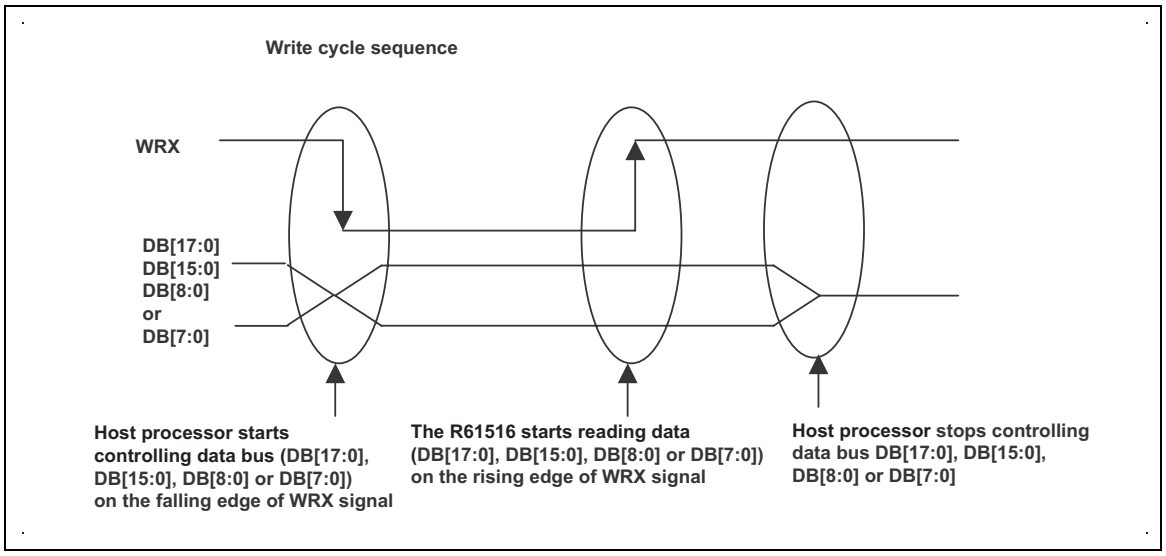
Figure 4 Example : DBI Type B

Write Cycle Sequence

In write cycle, data and/or command are written to the R61516 via the interface between the R61516 and the host processor. Each step of write cycle sequence (WRX high, WRX low, WRX high) comprises three control signals (DCX, RDX, WRX) and 8(DB[7:0]), 9(DB[8:0]), 16(DB[15:0]), or 18(DB[17 : 0]) bit data. The DCX bit indicates signal that is used to select command or data sent on the data bus.

When DCX=”1”, data on DB[17:0], DB[15:0], DB[8:0] or DB[7:0] is image data or command parameter. When DCX = 0, data on DB[7:0] is command.

Setting RDX and WRX to “Low” simultaneously is prohibited. See the figure below for the write cycle sequence.



Note: WRX is an not synchronous signal (can be halted).

Figure 5 Write Cycle Sequence

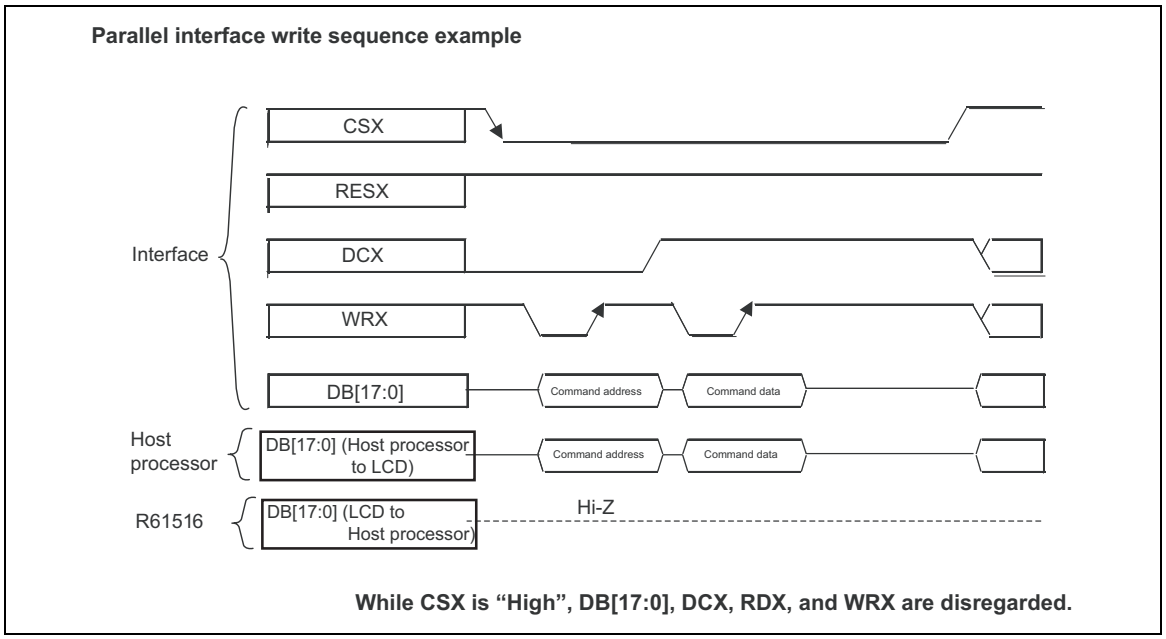
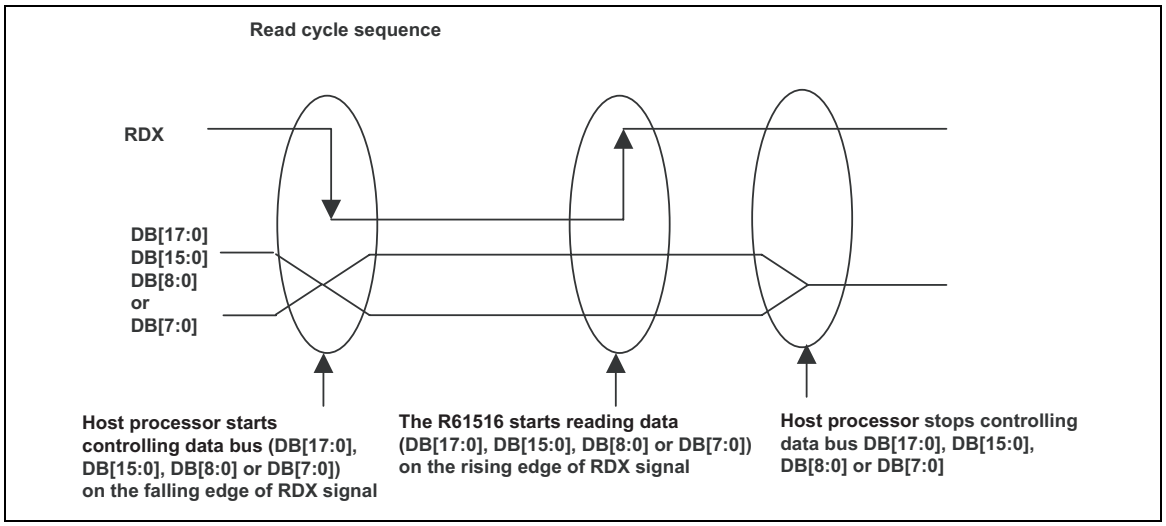


Figure 6

Read Cycle Sequence

In read cycle, data and/or commands are read from the R61516 via the interface between the R61516 and the host processor. The data (DB[17:0], [15:0], [8:0] or [7:0]) is transmitted from the R61516 to the host processor on the falling edge of RDX. The host processor reads the data on the rising edge of RDX. Setting RDX and WRX to Low simultaneously is prohibited. See below for the write cycle sequence.



Note: RDX is not synchronouos signal (can be halted).

Figure 7 Read Cycle Sequence

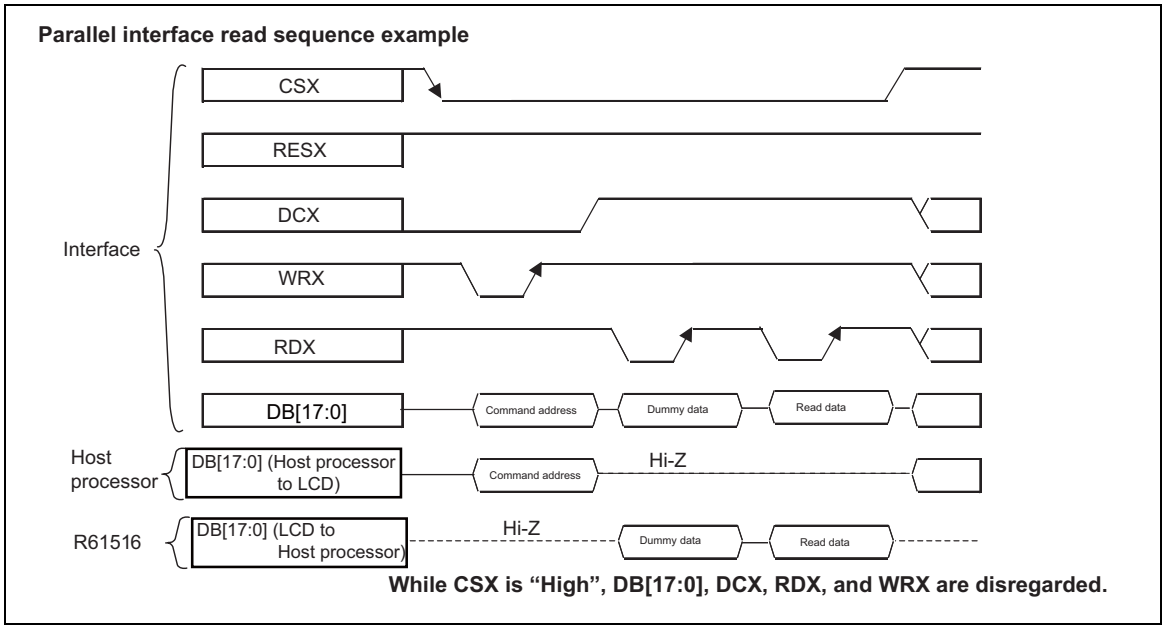


Figure 8

Data Transfer Break

When a break occurs in the transmission of parameter for command from the host processor to the R61516 before the last parameter of the command is sent to the R61516 and the host processor transmits the parameter(s) of a new command rather than the parameters of the interrupted command, the R61516 rejects the parameters of the new command following the break. The command parameters sent to the R61516 before the break occurs are stored in the register of the R61516. However those parameters sent after the break are disregarded, and the data in the register is not overwritten.

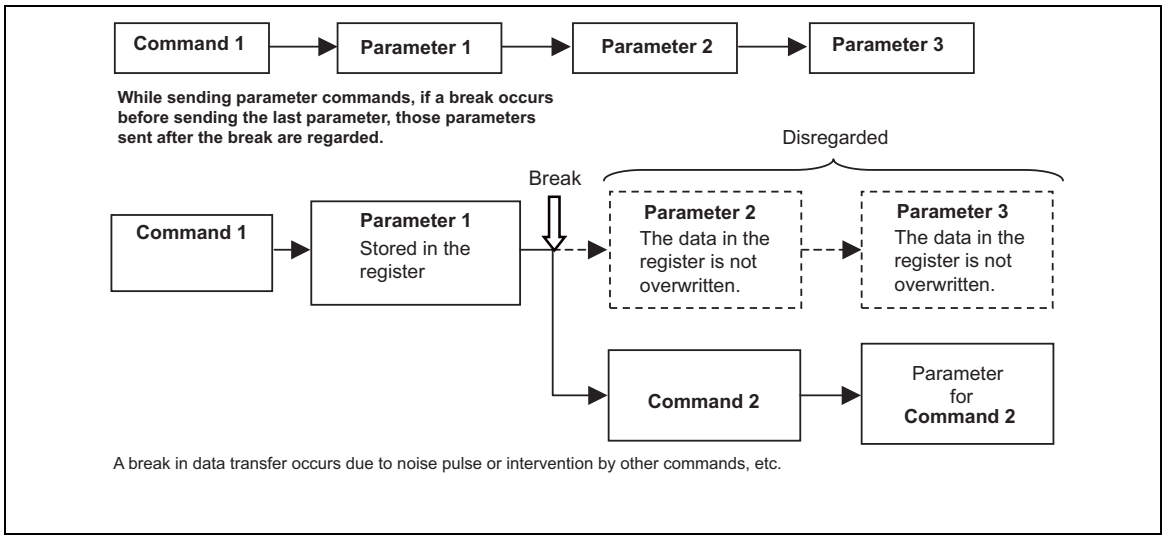


Figure 9

Data Transfer Pause (Command/Pause/Command)

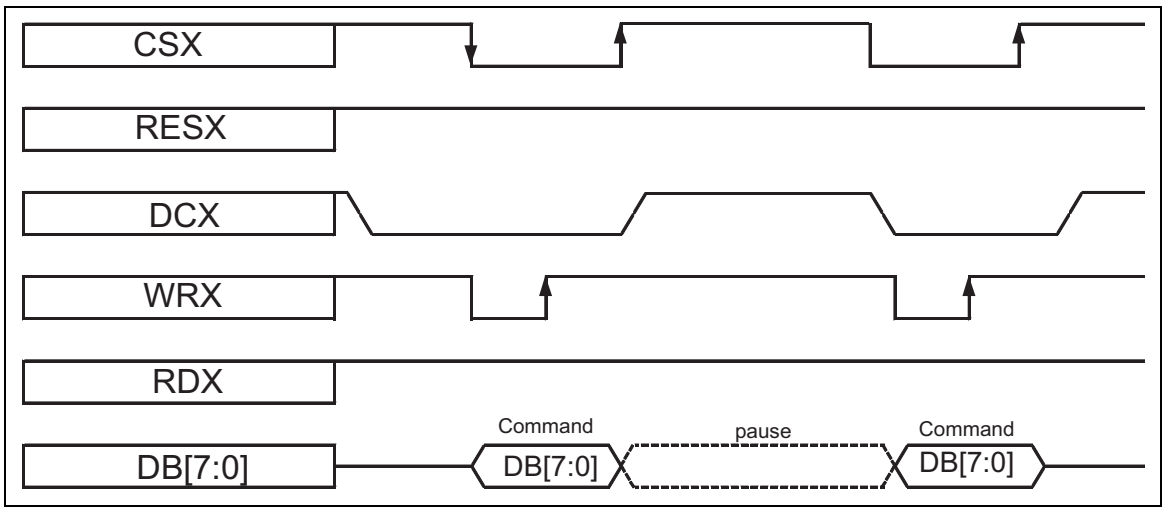


Figure 10

Data Transfer Pause (Command/Pause/Parameter)

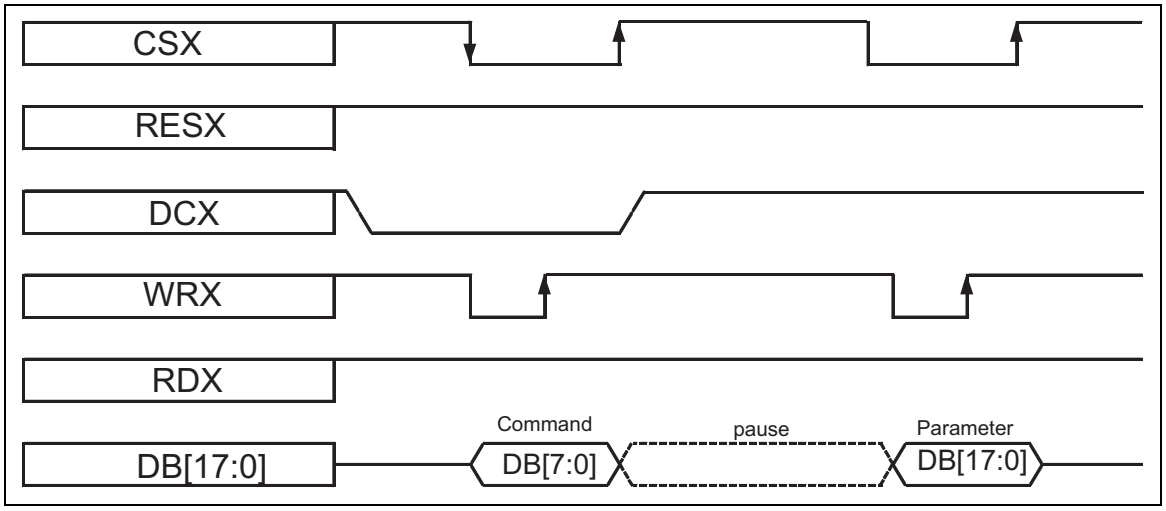


Figure 11

Data Transfer Pause (Parameter/Pause/Command)

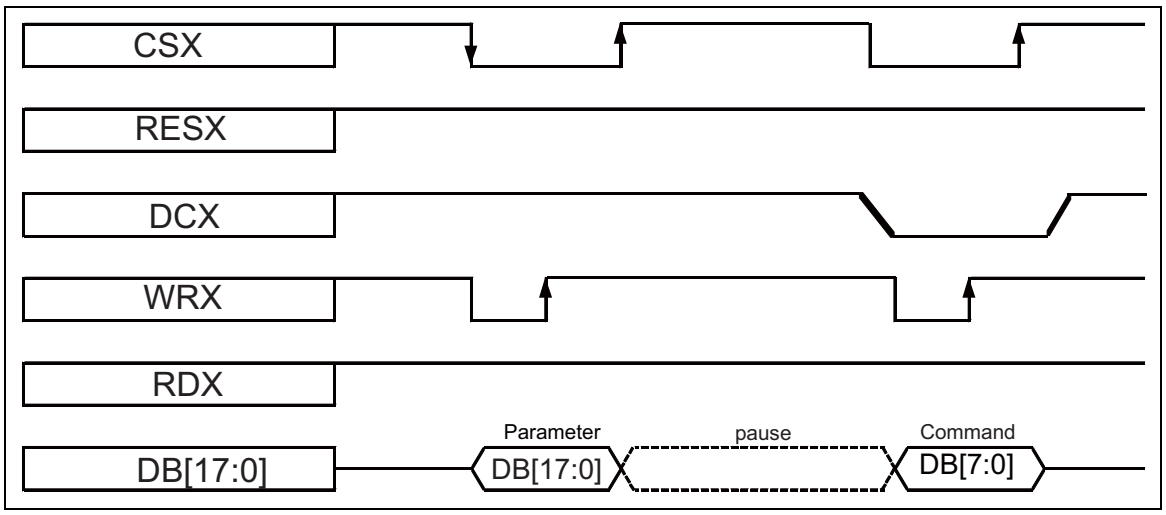


Figure 12

Data Transfer Pause (Parameter/Pause/Parameter)

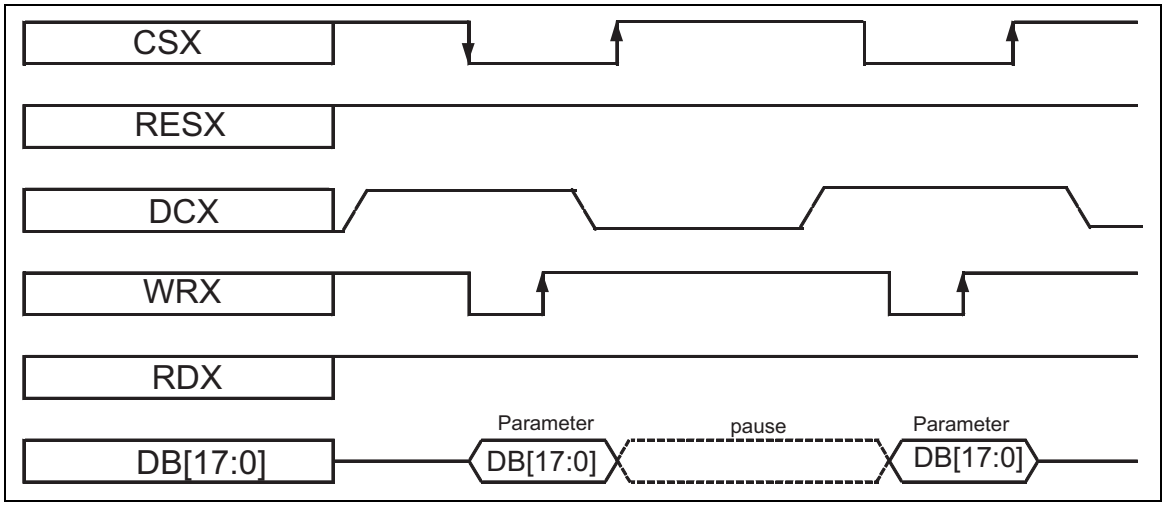


Figure 13

Data Transfer Mode

Two methods are available for writing data to the frame memory in the R61516.

(1) Write Method 1 (Default)

One frame of image data is written to the frame memory. The amount of the transmitted data is over 1 frame, the data is disregarded. The write operation of the data to the frame memory is terminated when a command intervenes in the middle fo the course. The R61516 writes the image data to the next frame when write_memory_start command (2Ch) is written. Set WEMODE =0 (Frame Memory Access and Interface setting (B3h)).

Start writing data to the frame memory (2Ch)	Image data for Frame 1	Any command	Start writing data to the frame memory (2Ch)	Image data for Frame 2	Any command

……	Any command

Figure 14

(2) Write Method 2

The image data is written consequtively to the frame memory. The frame memory pointer is reset to the start point when the frame memory becomes full and the driver starts writing the image data of the next frame. Set WEMODE =1 (Frame Memory Access and Interface setting (B3h)).

Start Stop

Start writing data to the frame memory (2Ch)	Image data for Frame 1	Image data for Frame 2	Image data for Frame 3	……	Any command

Figure 15

Note 1: Two write methods are available for all data transfer color modes in 18-/ 16-/ 9-/ 8- bit bus display command I/F.

Note 2: The number of pixel in one frame can be odd or even in both download methods. Only complete data sets are retained in the frame memory.

Note 3: The data write operation to the frame memory is terminated when a command intervenes in the middle of the course. In this case, if write_memory_continue (3Ch) is executed, the write operation can be started again from the address where the write operation is halted.

DBI Type C

The R61516 supports serial interface DBI Type C (Option 1 and 3).

Nine / Eight bit data, transmitted from the R61516 to the host processor, is stored in command register (CDR) or parameter register (PR) to start internal operation which is determined by signals from the host processor.

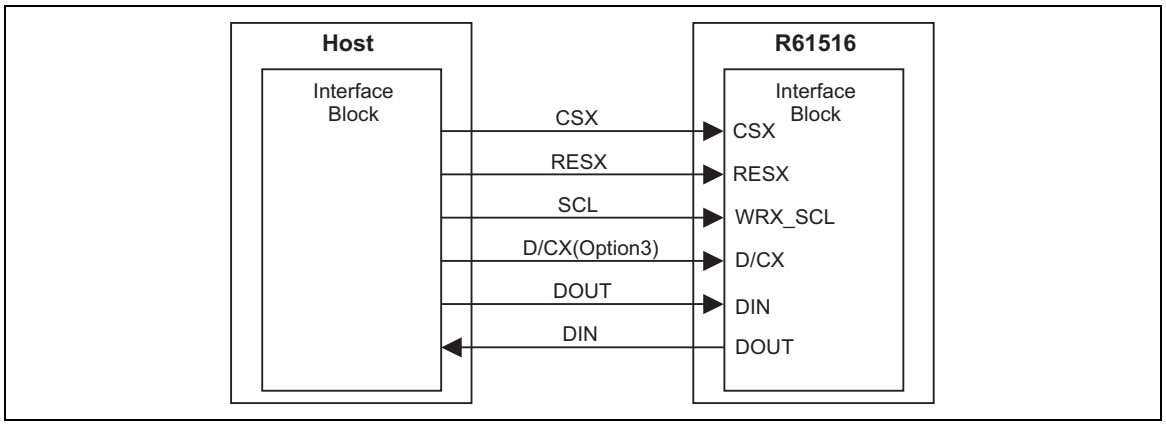
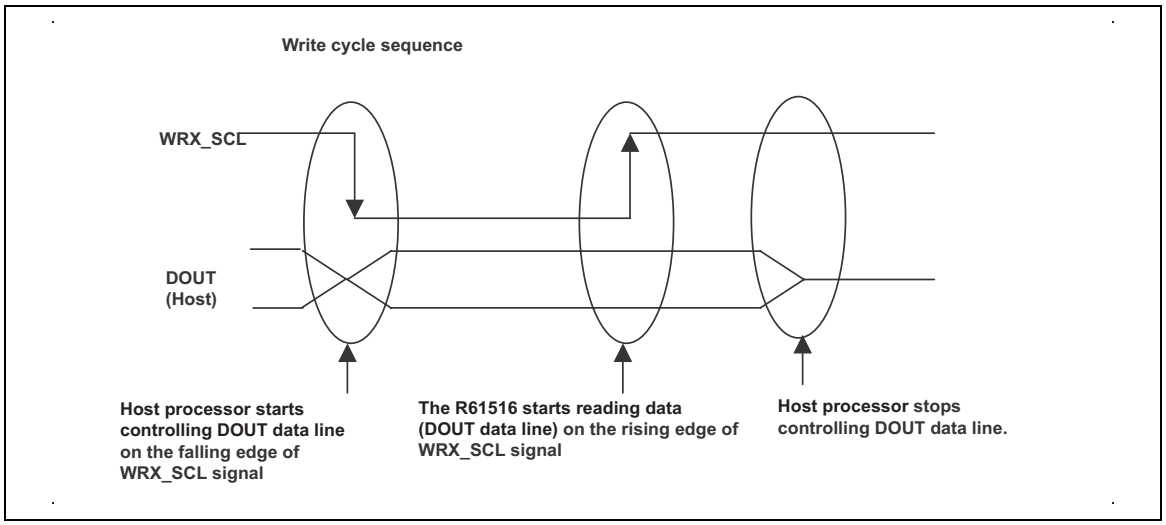


Figure 16 Example: DBI TypeC

Write Cycle Sequence

In write cycle, data and/or command are written to the R61516 via the interface between the R61516 and the host processor. Each step of write cycle sequence (WRX_SCL High Low High) has two or three control signals (DCX, WRX_SCL, D/CX) and data output from DOUT. During Write Cycle Sequence, the host processor outputs data while the R61516 accepts data at the rising edge of WRX_SCL.

If D/CX is used in DBI Type C Option 3 operation, data on DOUT is command when DCX="0". When DCX = 1, data on DOUT is image data or command parameter. See next figure for Write Cycle Sequene.



Note: WRX_SCL is not synchronous signal (can be halted).

Figure 17 Type C Write Cycle Sequence

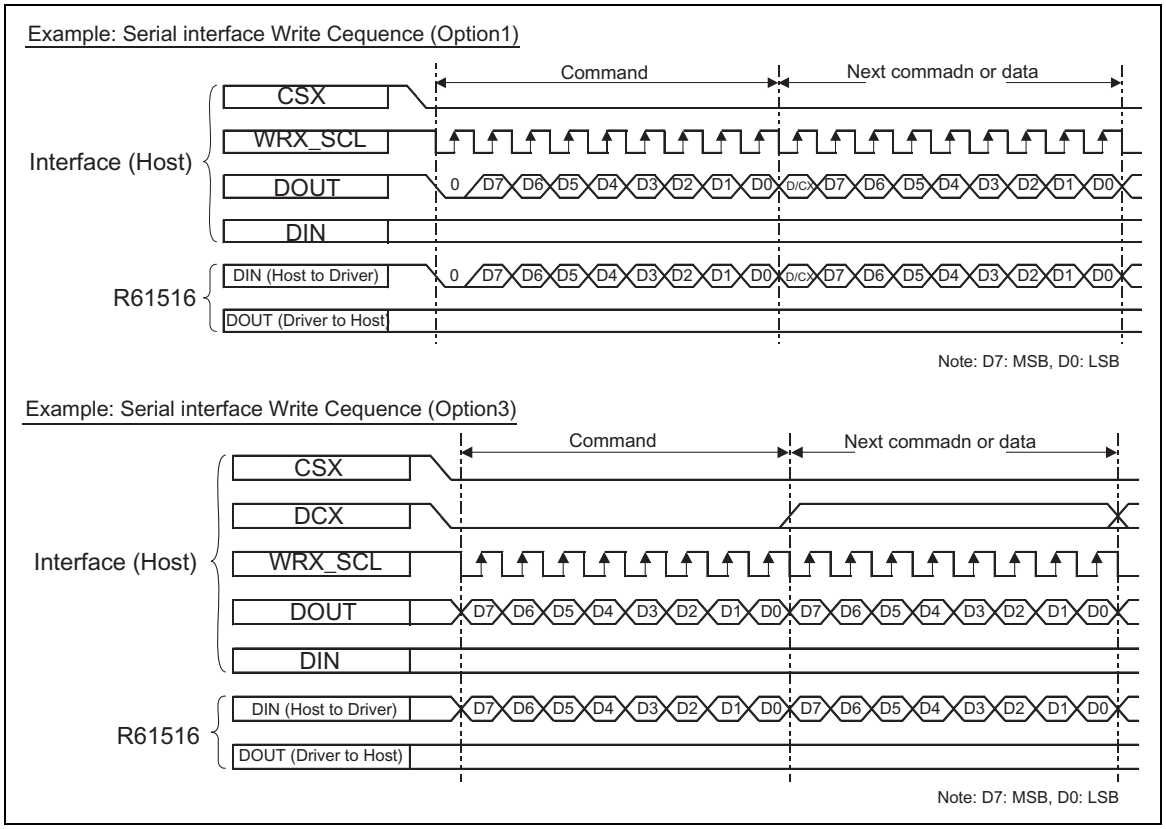
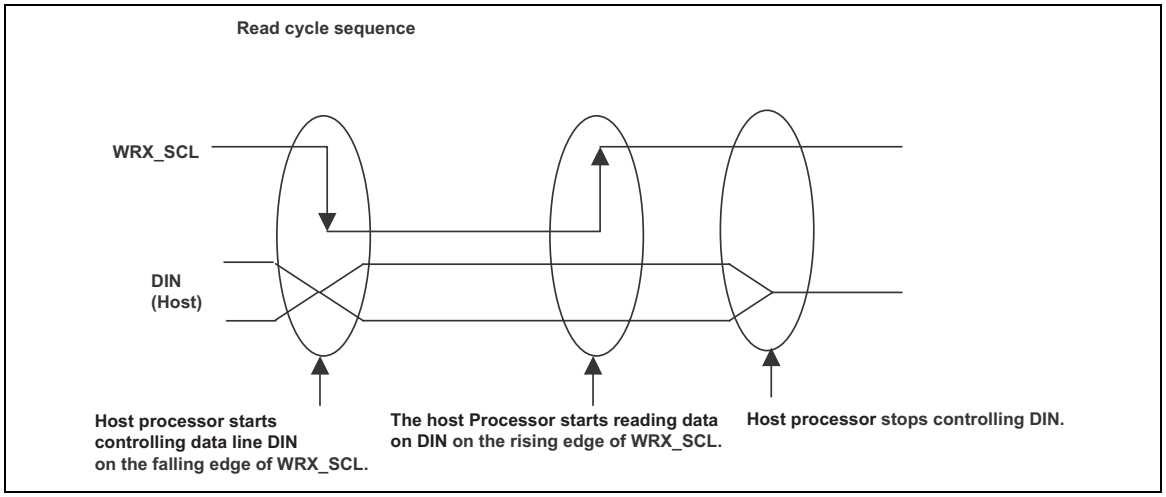


Figure 18 Serial Interface Write Cycle Sequence (Example)

Read Cycle Seqeuence

In read cycle, data and/or commands are read from the R61516 via the interface between the R61516 and the host processor. Data is transmitted from the R61516 to the host processor via DIN on the falling edge of WRX_SCL. The host processor reads the data on the rising edge of WRX_SCL. See next figure for the read cycle sequence.



Note: WRX_SCL is not synchronous signal (can be halted).

Figure 19 Read Cycle Sequence

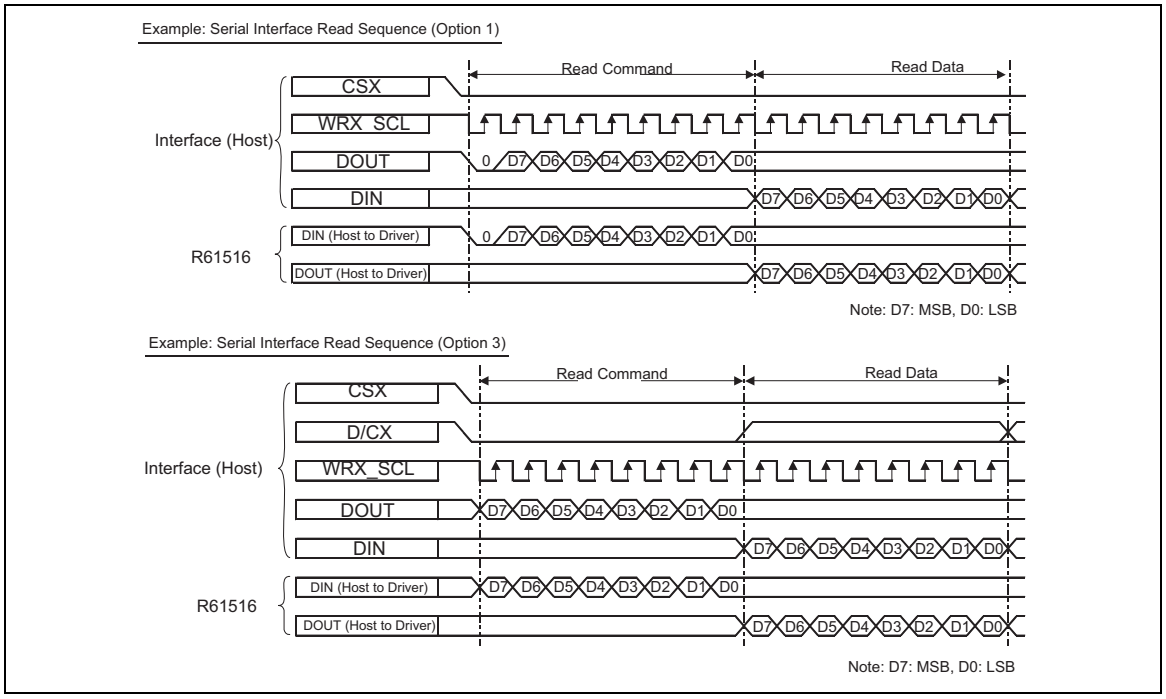


Figure 20 Serial Interface Write Cycle Sequence (Example)

Data Transfer Break

When a break occurs in the transmission of parameter for command from the host processor to the R61516 before the last parameter of the command is sent to the R61516 and the host processor transmits the parameter(s) of a new command rather than the parameters of the interrupted command, the R61516 rejects the parameters of the new command following the break. The command parameters sent to the R61516 before the break occurs are stored in the register of the R61516. However those parameters sent after the break are disregarded, and the data in the register is not overwritten.

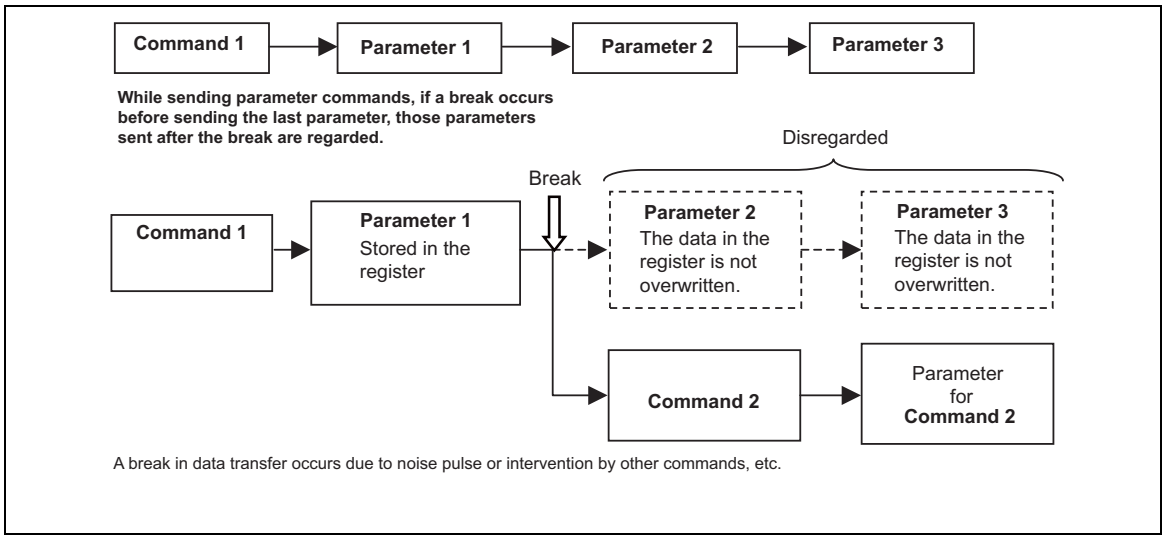


Figure 21

DBI Data Format

The R61516 supports color formats shown in the table below. At least one color format is supported by each of Type B 18-/ 16-/ 9- /8- bit and Type C interface.

Table 10

Type	IM2-0	Data pin	color format	MIPI Spec.	R61516
TypeB	000	DB[17:0]	18bpp	Not Defined	Yes
	010	DB[15:0]	8bpp	Yes	No
			12bpp	Yes	No
			16bpp	Yes	Yes
			18bpp (262K-color Option1)	Yes	Yes
			18bpp (262K-cloor Option2)	Yes	Yes
			24bpp (16M-cloor Option1)	Yes	No
			24bpp (16M-cloor Option2)	Yes	No
	001	DB[8:0]	18bpp	Yes	Yes
	011	DB[7:0]	8bpp	Yes	No
			12bpp	Yes	No
			16bpp	Yes	Yes
			18bpp	Yes	Yes
			24bpp	Yes	No
TypeC	101	DIN / DOUT	3bpp (8-color Option1)	Yes	Yes
			3bpp (8-color Option2)	Yes	Yes
			18bpp	Not Defined	Yes
	111	DIN / DOUT	3bpp (8-color Option1)	Yes	Yes
			3bpp (8-color Option2)	Yes	Yes
			18bpp	Not Defined	Yes

■DBI TypeB Data Format　　Note: This page shows example with BGR=0. If BGR=1, allocation of R and B in the frame memory is swapped.

● Data format for 18bit interface (DB[17:0] is used) IM2-0=000

	set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*											D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	*											D7	D6	D5	D4	D3	D2	D1	D0

	set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

●Pin connection for 16bit Bus interface (DB[15:0] is used) IM2-0=010

	set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*									D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	*									D7	D6	D5	D4	D3	D2	D1	D0

			First Transmission																Second Transmission														Third Transmission													
	set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	*	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]																																				
18bpp Frame Memory Write	3'h6	0	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]			G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]			B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]			R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]			G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]			B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]		
		1									R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]																		
Frame Memory Read	*	0	r1[5]	r1[4]	r1[3]	r1[2]	r1[1]	r1[0]			g1[5]	g1[4]	g1[3]	g1[2]	g1[1]	g1[0]			b1[5]	b1[4]	b1[3]	b1[2]	b1[1]	b1[0]			r2[5]	r2[4]	r2[3]	r2[2]	r2[1]	r2[0]			g2[5]	g2[4]	g2[3]	g2[2]	g2[1]	g2[0]			b2[5]	b2[4]	b2[3]	b2[2]	b2[1]	b2[0]		
		1									r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]																		

●Data format for 9bit interface (DB[8:0] is used) IM2-0=001

	set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*		D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	*		D7	D6	D5	D4	D3	D2	D1	D0

			First Transmission									Second Transmission								
	set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

●Data format for 8bit interface (DB[7:0] is used) IM2-0=011

	set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*	D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	*	D7	D6	D5	D4	D3	D2	D1	D0

			First Transmission								Second Transmission								Third Transmission							
	set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	*	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]								
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]		

●Extended format for 18bit/pixel data

		Frame Memory Data (18bpp)																
set_pixel_format	EPF	r5	r4	r3	r2	r1	r0	g5	g4	g3	g2	g1	g0	b5	b4	b3	b2	b1	b0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
16bpp	2'h0	R[4]	R[3]	R[2]	R[1]	R[0]	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	0
	2'h1	R[4]	R[3]	R[2]	R[1]	R[0]	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1
	2'h2	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]

R[4:0], B[4:0] = 5'h1F → r[5:0], b[5:0] = 6'hFF
R[4:0], B[4:0] = 5'h00 → r[5:0], b[5:0] = 6'h00

*The first Command Parameter Read and Frame Memory Read after read command is issued is invalid (dummy read).

Note 1: Data is written to the Frame Memory when data for one pixel is input. In 2-pixel 3- transfer operation (16bit I/F 18bpp Option1), the first and second pixels are written in the 2nd and 3rd transfers respectively.

Note 2: If data transfer stops after 2nd transfer in 2-pixel 3-transfer operation, the first pixel data is written normally. This applies to the last address when number of pixel is odd according to window setting.

■DBI TypeC Data Format

Note: This page shows example with BGR=0. If BGR=1, allocation of R and B in the frame memory is swapped.

●Data Format for Serial Interface Option1/Option3 IM2-0=101/111

	set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*	D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	*	D7	D6	D5	D4	D3	D2	D1	D0

			First Transmission								Second Transmission								Third Transmission							
	set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3bpp Frame Memory Write	3'h3	0			R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]																
		1		R1[0]	G1[0]	B1[0]		R2[0]	G2[0]	B2[0]																
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]		

●Extended format for 18bit/pixel data

		Frame Memory Data (18bpp)																	
set_pixel_format	EPF	r5	r4	r3	r2	r1	r0	g5	g4	g3	g2	g1	g0	b5	b4	b3	b2	b1	b0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
3pbb	*	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	G[0]	G[0]	G[0]	G[0]	G[0]	G[0]	B[0]	B[0]	B[0]	B[0]	B[0]	B[0]

*The first Command Parameter Read and Frame Memory Read after read command is issued is invalid (dummy read).

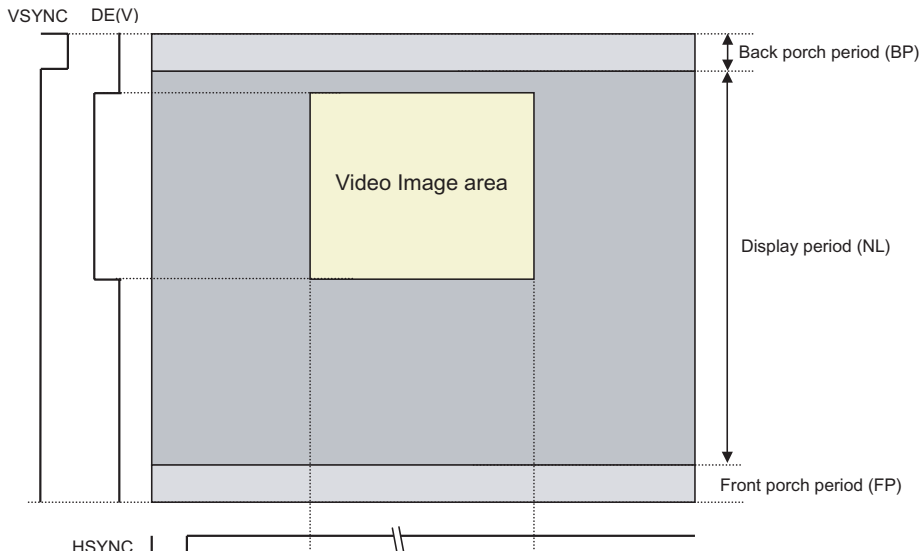
Display Pixel Interface (DPI)

Display Pixel Interface (DPI)

In Diplay Pixel Interface (DPI) operation, display operation is in synchronization with synchronization signals VSYNC, HSYNC and PCLK. If High Speed Write Mode (HWM=1) and Window Address Function are used together, the data is transferred only to the video image ara so that the R61516 conmumes only a small amount of power.

In DPI operation, front and back porch periods must be made before and after the display period. Commands must be transfeered via DBI Type B serial interface. DPI and DBI Type B cannot be used simultanaeously.

DPI and DBI TypeB cannot be used simultaneously.



VSYNC: Frame synchronization signal. Specifies the start position of a frame.
HSYNC: Line synchronization signal. Specifies the start of a horizontal line.
PCLK: Pixel clock. Data is accepted at the rising edge of this sgnal.
DE: Data enable signal. DE=High means the R61516 is in data enable period.
DB[17:0]: Display data (RGB).

Back porch period (BP) BP≧2H.
Front porch period (FP) FP≧3H.
Display period (DP) NL≦320H
Number of line in 1frame period = FP + NL + BP

Figure 22

DPI Timing

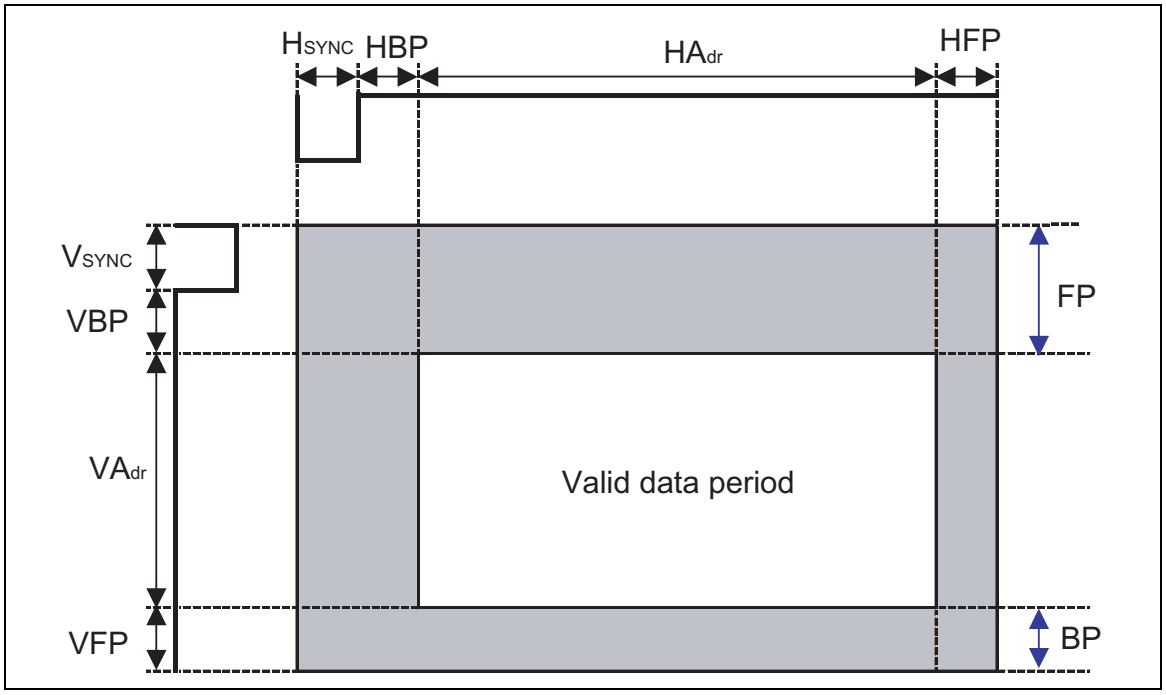


Figure 23

Table 11

Parameters	Symbols	Min.	Typ.	Max.	Step	Unit
Horizontal Synchronization	Hsync	2	10	16	1	PCLKCYC
Horizontal Back Porch	HBP	2	20	24	1	PCLKCYC
Horizontal Address	HAdr	–	240	–	1	PCLKCYC
Horizontal Front Porch	HFP	2	10	16	1	PCLKCYC
Vertical Synchronization	Vsync	1	2	4	1	Line
Vertical Back Porch	VBP	1	2	–	1	Line
Vertical Address	VAdr	–	320	–	1	Line
Vertical Front Porch	VFP	3	4	–	1	Line

Typical values are setting example when used with panel resolution QVGA (240 x 320), clock frequency 5.28MHz and frame frequency about 60Hz.

Note: Make sure that Vsync+VFP = BP, VFP = FP and Vadr＝line number specified by NL.

Also make sure that
(Number of PCLK per 1H) ≥ (Numebr of RTN clock) x Division ratio (DIV) x (PCDIVL+PCDIVH)

Setting example is as follows.

Setting Example for Display Control Clock in DPI Operation

Register Display operation using DPI is in synchronization with internal clock PCLKD which is generated by dividing PCLK.

PCDIVH [3:0]: Number of PCLK during internal clock CLKD's high period. In units of 1 clock.
PCDIVL [3:0]: Number of PCLK during internal clock CLKD's low period. In units of 1 clock.

PCDIVH and PCDIVL, specifying PCLK's division ratio, are determined so that dufference between PCLKD's frequency and internal oscillation clock 678KHz is the smallest. Set PCDIVL = PCDIVH or PCDIVL - 1. Follow the restriction (Number of PCLK in 1H) ≥ (Number of RTN clock) * (Division ratio (DIV)) * (PCDIVL + PCDIVH).

Setting Example

To set frame frequency to 60Hz:

Internal Clock

Internal Oscillation Clock: 678KHz
DIV=2'b1 (x 1/2)
RTN =17 clocks
FP=8'h8, BP=8'h8, NL=4F (320 lines)
→ **59.35Hz**

PCLK

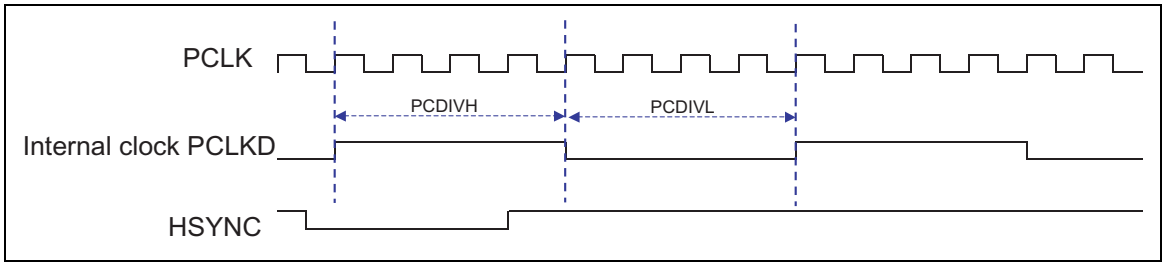
HSYNC = 10CLK
HBP = 20CLK
HFP=10CLK

60Hz x (8 + 320 + 8) line x (10 + 20 + 240 + 10) clock = 5.64MHz
PCLK frequency = 5.64MHz

5.64MHz / 678KHz = 8.32 → Set PCDIVH and PCDIVL so that PCLK is divided by 8.

5.64 / 8 = 705KHz
(705KHz / 2) / 17clock / 336 line = 61.7Hz

PCDIVH = 4'h4
PCDIVL = 4'h4



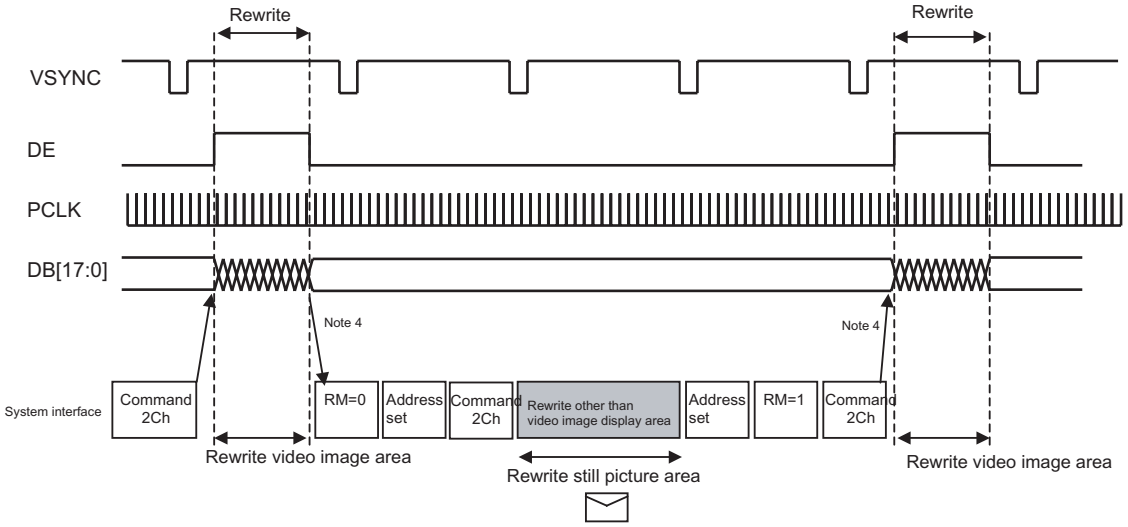
Video Image Display via DPI

The R61516 supports video image capable DPI and frame memory to store display data so that the driver has strong points such as

1. Window address function enabling data transfer for only video image area.
2. High-speed frame memory write mode enabling low power consumption operation and high-speed access.
3. Data only for video image display area can be transferred.
4. Reduced amount of data transfer enables low power consumption operation as the system as a whole.
5. Still picture area is rewritten even in video image display period by using system interface together with DPI.

To access Frame Memory via System Interface (DBI) in DPI operation

Frame memory can be accessed via system interface in DPI operation as well. However in DPI operation, the frame memory is always written in synchronization with PCLK when DE="High". Therefore, make sure to stop display data write operation via DPI to write data to frame memory via system interface. If RM=0, the frame memory is accessed via system interface. To return to DPI operation, make write/read bus cycle time and then set RM=1 and execute a write_memory_start command (2Ch) and then start frame memory access. If both interfaces are used to access the frame memory, write data is not guaranteed.



Note 1: In DPI operation, address is set at every falling efge of VSYNC.
Note 2: Set address and write_memory_start command (2Ch) before frame memory access via DPI starts.
Note 3: High-speed RAM write mode (HWM=1) must be selected in DPI operation.
Note 4: Wait 1 write cycle (tcycw) or more to switch to system interface after writing data via DPI.

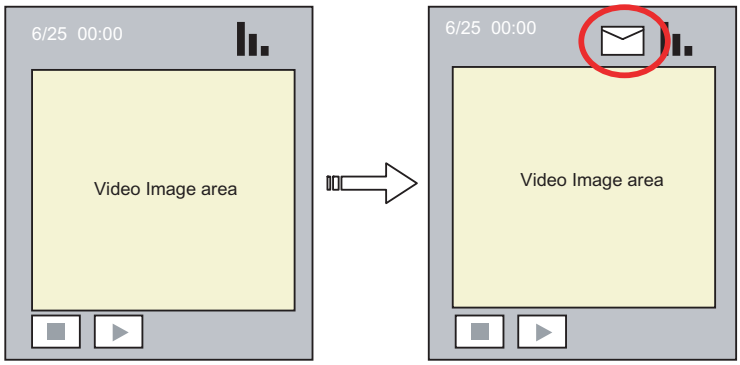


Figure 24

16-bit DPI connection

16-bit DPI is selected when RIM[1:0] = 2'h1. Image is displayed in synchronization with synchronization signals VSYNC, HSYNC and PCLK. 16-bit RGB data (DB[15:0]) is transferred to internal frame memory in synchronization with data enable signal DE and display operation.

* Commands are set only via system interface (DBI Type C).

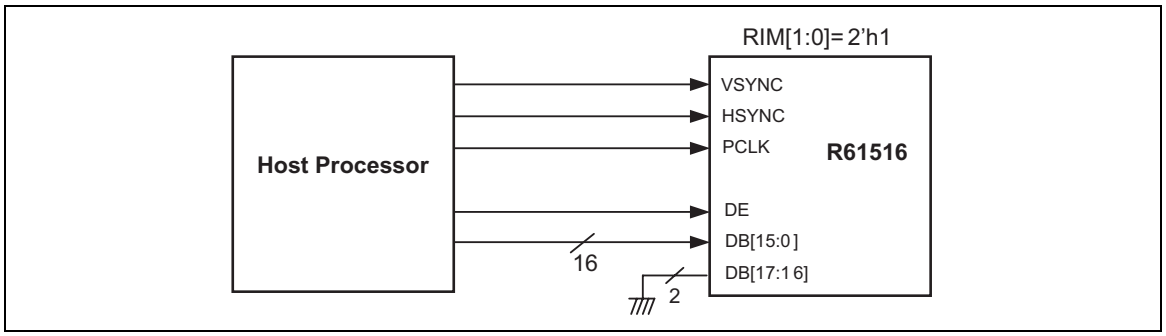


Figure 25

18-bit DPI connection

18-bit DPI is selected when RIM[1:0] = 2'h2. Image is displayed in synchronization with synchronization signals VSYNC, HSYNC and PCLK. 18-bit RGB data (DB[17:0]) is transferred to internal frame memory in synchronization with data enable signal DE and display operation.

* Setting command is possible only via system interface (DBI Type C).

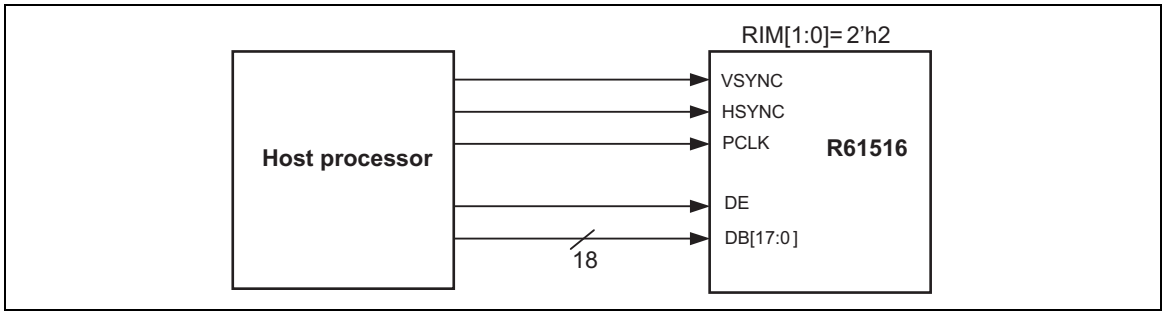


Figure 26

Note to DPI

a. In DPI operation, functions noted "disabled" in the table below are invalid.

Table 12

Function	External display interface	Internal dislay operation
Partial display function	Disabled	Enabled
Scrolling function	Disabled	Enabled
Idle mode	Disabled	Enabled

b. It is necessary to supply VSYNC, HSYNC and PCLK all the time during DPI operation.

c. Panel control signal reference clock is PCLK in DPI operation unlike usual internal oscillation clock.

d. Make sure to follow mode switching sequence to transit from/to display by internal operation mode to/from display via DPI.

e. Make sure to set HWM =1 (High speed frame memory write mode) in DPI operation.

f. Address is set every frame on the falling edge of VSYNC during DPI operation.

DPI Data Format

The R61516 supports color formats as below:

Table 13

RIM[1:0]	Data pin	color format	MIPI Spec.	R61516
—	—	24bpp	Yes	No
2'h2	DB[17:0]	18bpp	Yes	Yes
2'h1	DB[15:0]	16bpp	Yes	Yes

See next figure for connection of host professor and the R61516's pins.

■DPI Data Format

Note: This page shows example with BGR=0. If BGR=1, allocation of R and B in the frame memory is swapped.

●Pin connection for 18bit interface Used pin: DB[17:0] RIM[1:0]=2'h2, set pixel format D[6:4]=3'h6: 18bpp

Configuration1

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
							↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
R61516 pin							DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Configuration2

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0
			↓	↓	↓	↓	↓	↓			↓	↓	↓	↓	↓	↓			↓	↓	↓	↓	↓	↓
R61516 pin			DB17	DB16	DB15	DB14	DB13	DB12			DB11	DB10	DB9	DB8	DB7	DB6			DB5	DB4	DB3	DB2	DB1	DB0
			R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0

●Pin connection for 16bit interface Used pin: DB[15:0] RIM[1:0]=2'h1, set pixel format D[6:4]=3'h5: 18bpp

Configuration1

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
									↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
R61516 pin									DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
									R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Configuration2

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0				B4	B3	B2	B1	B0
				↓	↓	↓	↓	↓			↓	↓	↓	↓	↓	↓				↓	↓	↓	↓	↓
R61516 pin				DB15	DB14	DB13	DB12	DB11			DB10	DB9	DB8	DB7	DB6	DB5				DB4	DB3	DB2	DB1	DB0
				R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0				B4	B3	B2	B1	B0

Configuration3

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			R4	R3	R2	R1	R0				G5	G4	G3	G2	G1	G0			B4	B3	B2	B1	B0	
			↓	↓	↓	↓	↓				↓	↓	↓	↓	↓	↓			↓	↓	↓	↓	↓	
R61516 pin			DB15	DB14	DB13	DB12	DB11				DB10	DB9	DB8	DB7	DB6	DB5			DB4	DB3	DB2	DB1	DB0	
			R4	R3	R2	R1	R0				G5	G4	G3	G2	G1	G0			B4	B3	B2	B1	B0	

●Extended format for 18bit/pixel data

			Frame Memory Data (18bpp)																	
set_pixel_format	RIM	EPF	r5	r4	r3	r2	r1	r0	g5	g4	g3	g2	g1	g0	b5	b4	b3	b2	b1	b0
18bpp	1	*	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16bpp	2	2'h0	R4	R3	R2	R1	R0	0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0
		2'h1	R4	R3	R2	R1	R0	1	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1
		2'h2	R4	R3	R2	R1	R0	R4	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4

R[4:0], B[4:0] = 5'h1F → r[5:0], b[5:0] = 6'hFF
R[4:0], B[4:0] = 5'h00 → r[5:0], b[5:0] = 6'h00

Command Description

Table 14 User Command

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter	MIPI DCS Type1 Requirement	R61516 Implementation	Note
00h	nop	C	0	Yes	Yes	
01h	soft_reset	C	0	Yes	Yes	
06h	get_red_channel	R	1	No	No	
07h	get_green_channel	R	1	No	No	
08h	get_blue_channel	R	1	No	No	
0Ah	get_power_mode	R	1	Yes	Yes	
0Bh	get_address_mode	R	1	Yes (Bit7-0)	Yes (Bit7/6/5/4/0 Only)	
0Ch	get_pixel_format	R	1	Yes	Yes	
0Dh	get_display_mode	R	1	Yes	Yes	1
0Eh	get_signal_mode	R	1	Yes	Yes	
0Fh	get_diagnostic _result	R	1	Bit7/6: Yes Bit5/4: Optional	Yes (Bit7/6 Only)	
10h	enter_sleep_mode	C	0	Yes	Yes	
11h	exit_sleep_mode	C	0	Yes	Yes	
12h	enter_partial_mode	C	0	Yes	Yes	
13h	enter_normal_mode	C	0	Yes	Yes	
20h	exit_invert_mode	C	0	Yes	Yes	
21h	enter_invert_mode	C	0	Yes	Yes	
26h	set_gamma_curve	W	1	Yes	No	1
28h	set_display_off	C	0	Yes	Yes	
29h	set_display_on	C	0	Yes	Yes	
2Ah	set_column_address	W	4	Yes	Yes	
2Bh	set_page_address	W	4	Yes	Yes	

User Command (continued)

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter	MIPI DCS Type1 Requirement	R61516 Implementation	Note
2Ch	write_memory_start	W	Variable	Yes	Yes	2
2Dh	wite_LUT	W	Variable	Optional	No	
2Eh	read_memory_start	R	Variable	Yes	Yes	2
30h	set_partial_area	W	4	Yes	Yes	
33h	set_scroll_area	W	6	Yes	Yes	
34h	set_tear_off	C	0	Yes	Yes	
35h	set_tear_on	W	1	Yes	Yes	
36h	set_address_mode	W	1	Yes (Bit7-0)	Yes (Bit7/6/5/4/0 Only)	
37h	set_scroll_start	W	2	Yes	Yes	
38h	exit_idle_mode	C	0	Yes	Yes	
39h	enter_idle_mode	C	0	Yes	Yes	
3Ah	set_pixel_format	W	1	Yes	Yes	
3Ch	write_memory _continue	W	Variable	Yes	Yes	2
3Eh	read_memory _continue	R	Variable	Yes	Yes	2
44h	set_tear_scanline	W	2	Yes	Yes	
45h	get_scanline	R	2	Yes	Yes	
A1h	read_DDB_start	R	5	Yes	Yes	
A8h	read_DDB_continue	R	Variable	Yes	Yes	

Note1: The R61516 supports one type of gamma curve specified by gamma adjustment register G0. Therefore, D [2:0] bit (get_display_mode, 0Dh) is fixed at 0.

Note 2: See Data Format List to find about formats of write and read data for the Frame Memory.

Table 15 Manufacturer Command

Operational Code (Hex)	Function	Command(C) /Read(R) /Write(W)	Number Of Parameter	Category
B0h	Manufacturer Command Access Protect	W/R	1	Additional User Command
B1h	Low Power Mode Control	W/R	1	Additional User Command
B3h	Frame Memory Access and Interface setting	W/R	5	Additional User Command
B4h	Display Mode and Frame Memory Write Mode seting	W/R	1	Additional User Command
BFh	Device code Read	R	4	
C0h	Panel Driving Setting	W/R	8	
C1h	Display Timing Setting for Normal Mode	W/R	5	
C2h	Display Timing Setting for Partial Mode	W/R	5	
C3h	Display Timing Setting for Idle Mode	W/R	5	
C4h	Source/VCOM/Gate Driving Timing setting	W/R	5	
C8h	Gamma Setting for Red	W/R	20	
C9h	Gamma Setting for Green	W/R	20	
CAh	Gamma Setting for Blue	W/R	20	
D0h	Power Setting (Common)	W/R	7	
D1h	VCOM Setting	W/R	3	
D2h	Power Setting for Normal Mode	W/R	2	
D3h	Power Setting for Partial Mode	W/R	2	
D4h	Power Setting for Idle Mode	W/R	2	
E0h	NV Memory Access Control	W/R	2	
E1h	NV Memory Write Data	W/R	2	
E2h	NV Memory Data Load Register for User	W/R	6	
E8h	EEPROM Write Enable	C	0	
E9h	EEPROM Write Disable	C	0	
EAh	EEPROM Word Write	W/R	2	
EBh	EEPROM Word Read	R	3	
ECh	EEPROM Address Set	W/R	1	
B0～FF Except above command	LSI TEST Registers	W/R	Variable	

Command Accessibility

In initial state, only User Command and B0h Manufacuturer Command Access Protect command are accessible. Other commands are treated as nop.

Of Manufacturer Command (B0h-ECh) defined in the table below, additional user commands (B1h-B4h) are accessible only when MCAP=2'h2.

Other Manufacturer Commands (C0h-ECh) are accessible only when MCAP=2'h0. See MCAP command description for detail.

Table 16 User Command

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idel Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idel Mode On Sleep Mode Off	Sleep Mode On
00h	nop	Yes	Yes	Yes	Yes	Yes
01h	soft_reset	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
0Ah	get_power_mode	Yes	Yes	Yes	Yes	Yes
0Bh	get_address_mode	Yes	Yes	Yes	Yes	Yes
0Ch	get_pixel_format	Yes	Yes	Yes	Yes	Yes
0Dh	get_display_mode	Yes	Yes	Yes	Yes	Yes
0Eh	get_signal_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
0Fh	get_diagnostic _result	Yes	Yes	Yes	Yes	Yes
10h	enter_sleep_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
11h	exit_sleep_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
12h	enter_partial_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
13h	enter_normal_mode	Yes	Yes	Yes	Yes	Yes
20h	exit_invert_mode	Yes	Yes	Yes	Yes	Yes
21h	enter_invert_mode	Yes	Yes	Yes	Yes	Yes
28h	set_display_off	Yes	Yes	Yes	Yes	Yes
29h	set_display_on	Yes	Yes	Yes	Yes	Yes
2Ah	set_column_address	Yes	Yes	Yes	Yes	Yes
2Bh	set_page_address	Yes	Yes	Yes	Yes	Yes

User Command (continued)

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idel Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idel Mode On Sleep Mode Off	Sleep Mode On
2Ch	write_memory_start	Yes	Yes	Yes	Yes	Yes
2Eh	read_memory_start	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
30h	set_partial_area	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
33h	set_scroll_area	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
34h	set_tear_off	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
35h	set_tear_on	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
36h	set_address_mode	Yes	Yes	Yes	Yes	Yes
37h	set_scroll_start	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
38h	exit_idle_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
39h	enter_idle_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
3Ah	set_pixel_format	Yes	Yes	Yes	Yes	Yes
3Ch	write_memory _continue	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
3Eh	read_memory _continue	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
44h	set_tear_scanline	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
45h	get_scanline	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
A1h	read_DDB_start	Yes	Yes	Yes	Yes	Yes
A8h	read_DDB_continue	Yes	Yes	Yes	Yes	Yes

Note: Command may be accessed only when DM=0 (display operation is in synchronization with internal oscillation clock).

To access these commands is disabled when DM=1 and DPI is selected.

Table 17 Manufacturer Command

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idel Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idel Mode On Sleep Mode Off	Sleep Mode On
B0h	Manufacturer Command Access Protect	Yes	Yes	Yes	Yes	Yes
B1h	Low Power Mode Control	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
B3h	Frame Memory Access and Interface setting	Yes	Yes	Yes	Yes	Yes
B4h	Display Mode and Frame Memory Write Mode seting	Yes	Yes	Yes	Yes	No
BFh	Device Code Read	Yes	Yes	Yes	Yes	Yes
C0h	Panel Driving Setting	Yes	Yes	Yes	Yes	Yes
C1h	Display Timing Setting for Normal Mode	Yes	Yes	Yes	Yes	Yes
C2h	Display Timing Setting for Partial Mode	Yes	Yes	Yes	Yes	Yes
C3h	Display Timing Setting for Idle Mode	Yes	Yes	Yes	Yes	Yes
C4h	Source/VCOM/Gate Driving Timing setting	Yes	Yes	Yes	Yes	Yes
C8h	Gamma Setting for Red	Yes	Yes	Yes	Yes	Yes
C9h	Gamma Setting for Green	Yes	Yes	Yes	Yes	Yes
CAh	Gamma Setting for Blue	Yes	Yes	Yes	Yes	Yes
D0h	Power Setting (Common)	Yes	Yes	Yes	Yes	Yes
D1h	VCOM Setting	Yes	Yes	Yes	Yes	Yes
D2h	Power Setting for Normal Mode	Yes	Yes	Yes	Yes	Yes
D3h	Power Setting for Partial Mode	Yes	Yes	Yes	Yes	Yes
D4h	Power Setting for Idle Mode	Yes	Yes	Yes	Yes	Yes
E0h	NV Memory Access Control	Yes	Yes	Yes	Yes	Yes
E1h	NV Memory Write Data	Yes	Yes	Yes	Yes	Yes
E2h	NV Memory Data Load Register for User	Yes	Yes	Yes	Yes	Yes
E8h	EEPROM Write Enable	Yes	Yes	Yes	Yes	Yes
E9h	EEPROM Write Disable	Yes	Yes	Yes	Yes	Yes
EAh	EEPROM Word Write	Yes	Yes	Yes	Yes	Yes

EBh	EEPROM Word Read	Yes	Yes	Yes	Yes	Yes
ECh	EEPROM Address Set	Yes	Yes	Yes	Yes	Yes
B0～FF Except above command	LSI TEST Registers	No	No	No	No	No

Note: Command may be accessed only when DM=0 (display operation is in synchronization with internal oscillation clock).

To access these commands is disabled when DM=1 and DPI is selected.

Default Modes and Values

Table 18 User Command

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
00h	nop	None	N/A	N/A	N/A
01h	soft_reset	None	N/A	N/A	N/A
0Ah	get_power_mode	1st	08h	08h	08h
0Bh	get_address_mode	1st	00h	No Change (Note1)	00h
0Ch	get_pixel_format	1st	66h	No Change (Note1)	66h
0Dh	get_display_mode	1st	00h	00h	00h
0Eh	get_signal_mode	1st	00h	00h	00h
0Fh	get_diagnostic _result	1st	00h	00h	00h
10h	enter_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
11h	exit_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
12h	enter_partial_mode	None	Normal Display Mode On	Normal Display Mode On	Normal Display Mode On
13h	enter_normal_mode	None	Normal Display Mode On	Normal Display Mode On	Normal Display Mode On
20h	exit_invert_mode	None	Display Inversion Off	Display Inversion Off	Display Inversion Off
21h	enter_invert_mode	None	Display Inversion Off	Display Inversion Off	Display Inversion Off
28h	set_display_off	None	Display Off	Display Off	Display Off
29h	set_display_on	None	Display Off	Display Off	Display Off
2Ah	set_column_address	1st/2nd SC[8:0]	000h	000h	000h
		3rd/4th EC[8:0]	0EFh	If set_address_mode B5=0 : 0EFh B5=1 : 13Fh	0EFh
2Bh	set_page_address	1st/2nd SP[8:0]	000h	000h	000h
		3rd/4th EP[8:0]	13Fh	If set_address_mode B5=0 : 13Fh B5=1 : 0EFh	13Fh

User command (continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
2Ch	write_memory_start	all	Random Values	Not Cleared	Not Cleared
2Eh	read_memory_start	all	Random Values	Not Cleared	Not Cleared
30h	set_partial_area	1st/2nd SR[8:0]	000h	000h	000h
		3rd/4th ER[8:0]	13Fh	13Fh	13Fh
33h	set_scroll_area	1st/2nd TFA[8:0]	000h	000h	000h
		3rd/4th VSA[8:0]	140h	140h	140h
		4th/5th BFA[8:0]	000h	000h	000h
34h	set_tear_off	None	TE line output Off	TE line output Off	TE line output Off
35h	set_tear_on	1st	TE line output Off	TE line output Off	TE line output Off
36h	set_address_mode	1st	00h	No Change (Note1)	00h
37h	set_scroll_start	1st/2nd VSP[8:0]	000h	000h	000h
38h	exit_idle_mode	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
39h	enter_idle_mode	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
3Ah	set_pixel_format	1st	66h	No Change (Note1)	66h
3Ch	write_memory _continue	all	Random Values	Not Cleared	Not Cleared
3Eh	read_memory _continue	all	Random Values	Not Cleared	Not Cleared
44h	set_tear_scanline	1st/2nd STS[8:0]	000h	000h	000h
45h	get_scanline	1st/2nd GTS[9:0]	000h (invalid)	000h (invalid)	000h (invalid)

User command (continued)

A1h	read_DDB_start	1st	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)
		2nd	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)
		3rd	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		4th	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		5th	FFh	FFh	FFh
A8h	read_DDB_continue	-	See read_DDB_start	See read_DDB_start	See read_DDB_start

Note1) No Change from the value before soft_reset command.

Note2) If external EEPROM is used (EEPROME=VCC), data is loaded from the EEPROM. If external EEPROM is not used (EEPROME=GND), data is loaded from internal NVM. If user writes VCM register value, Supplier ID and Supplier Elective Data to the NVM, the values are set as default.

Table 19 Manufacturer Command

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
B0h	Manufacturer Command Access Protect	1st	MCAP=2h3	No Change (Note1)	MCAP=2h3
B1h	Low Power Mode Control	1st	DSTB=0 Sleep Mode On	DSTB=0 Sleep Mode On	DSTB=0 Sleep Mode On
B3h	Frame Memory Access and Interface setting	1st	WEMODE=0 HWM=0	No Change (Note1)	WEMODE=0 HWM=0
		2nd	TEI[2:0]=0	No Change (Note1)	TEI[2:0]=0
		3rd	ENC[2:0]=0	No Change (Note1)	ENC[2:0]=0
		4th	EPF[1:0]=2'h0 DFM=0	No Change (Note1)	EPF[1:0]=2'h0 DFM=0
		5th	RIM[1:0]=2'h2	No Change (Note1)	RIM[1:0]=2'h2
B4h	Display Mode and Frame Memory Write Mode seting	1st	RM=0 DM[1:0]=2'h0	No Change (Note1)	RM=0 DM[1:0]=2'h0
BFh	Device Code Read	1st	8'h01	8'h01	8'h01
		2nd	8'h22	8'h22	8'h22
		3rd	8'h15	8'h15	8'h15
		4th	8'h16	8'h16	8'h16
C0h	Panel Driving Setting	1st	GMM=0 REV=0 SM=0 GS=0 BGR=0 SS=0	No Change (Note1)	GMM=0 REV=0 SM=0 GS=0 BGR=0 SS=0
		2nd	NL[6:0]=7'h4F	No Change (Note1)	NL[6:0]=7'h4F
		3rd	SCN[6:0]=7'h00	No Change (Note1)	SCN[6:0]=7'h00
		4th	NW=0	No Change (Note1)	NW=0
		5th	PTDC=0 BLV=1 PTV=0	No Change (Note1)	PTDC=0 BLV=1 PTV=0
		6th	BLS=0 NDL=0 PTS[1:0]=0	No Change (Note1)	BLS=0 NDL=0 PTS[1:0]=0

		7th	PTG=0 ISC[3:0]=4'h1	No Change (Note1)	PTG=0 ISC[3:0]=4'h1
		8th	PCDIVH[2:0]=3'h0 PCDIVL[2:0]=3'h0	No Change (Note1)	PCDIVH[2:0]=3'h0 PCDIVL[2:0]=3'h0
C1h,C2h, C3h	Display Timing Setting -for Normal Mode -forPartial Mode -for Idle Mode	1st	BCx=1	No Change (Note1)	BCx=1
		2nd	DIVx[1:0]=2'h1	No Change (Note1)	DIVx[1:0]=2'h1
		3rd	RTNx[5:0]=6'h11	No Change (Note1)	RTNx[5:0]=6'h11
		4th	BPx[7:0]=8'h08	No Change (Note1)	BPx[7:0]=8'h08
		5th	FPx[7:0]=8'h08	No Change (Note1)	FPx[7:0]=8'h08
C4h	Source/VCOM/Gate Driving Timing setting	1st	SDT[2:0]=3'h1 NOW[2:0]=3'h1	No Change (Note1)	SDT[2:0]=3'h1 NOW[2:0]=3'h1
		2nd	MCP[2:0]=3'h1	No Change (Note1)	MCP[2:0]=3'h1
		3rd	VEQW[3:0]=4'h0 VEM[1:0]=2'h0	No Change (Note1)	VEQW[3:0]=4'h0 VEM[1:0]=2'h0
		4th	SPCW[3:0]=4'h0	No Change (Note1)	SPCW[3:0]=4'h0
C8h	Gamma Setting for Red	1st-18th	All "0"	No Change (Note1)	All "0"
C9h	Gamma Setting for Green	1st-18th	All "0"	No Change (Note1)	All "0"
CAh	Gamma Setting for Blue	1st-18th	All "0"	No Change (Note1)	All "0"
D0h	Power Setting (Common)	1st	VC[2:0]=3'h7	No Change (Note1)	VC[2:0]=3'h7
		2nd	BT[2:0]=3'h5	No Change (Note1)	BT[2:0]=3'h5
		3rd	8'hDF (VRH[4:0]=5'h1F)	No Change (Note1)	8'hDF (VRH[4:0]=5'h1F)
D1h	VCOM Setting	1st	VCM[6:0]=7'h7F	No Change (Note1)	VCM[6:0]=7'h7F
		2nd	VDV[4:0]=5'h00	No Change (Note1)	VDV[4:0]=5'h00
		3rd	VCMR=1 SELVCM=0	No Change (Note1)	VCMR=1 SELVCM=0
D2h,D3h D4h	Power Setting -for Normal Mode -forPartial Mode -for Idle Mode	1st	APx[1:0]=2'h3	No Change (Note1)	APx[1:0]=2'h3
		2nd	DC1x[2:0]=3'h2 DC0x[2:0]=3'h5	No Change (Note1)	DC1x[2:0]=3'h2 DC0x[2:0]=3'h5

E0h	NV Memory Access Control	1st	FTT=0 CALB=0 OP[1:0]=2'h0 NVAD[2:0]=3'h0	FTT=0 CALB=0 OP[1:0]=2'h0 NVAD[2:0]=3'h0	FTT=0 CALB=0 OP[1:0]=2'h0 NVAD[2:0]=3'h0
		2nd	NVVRF=0	NVVRF=0	NVVRF=0
E1h	NV Memory Write Data	1st	NVDAT[15:8] =8'h00	NVDAT[15:8] =8'h00	NVDAT[15:8] =8'h00
		2nd	NVDAT[7:0] =8'h00	NVDAT[7:0] =8'h00	NVDAT[7:0] =8'h00
E2h	NV Memory Data Load Register for User	1st	8'hFF (T_VCM[6:0] =7'h7F) (Note2)	8'hFF (T_VCM[6:0] =7'h7F) (Note2)	8'hFF (T_VCM[6:0] =7'h7F) (Note2)
		2nd	8'hFF	8'hFF	8'hFF
		3rd	T_ID1[15:8] =8'hFF (Note2)	T_ID1[15:8] =8'hFF (Note2)	T_ID1[15:8] =8'hFF (Note2)
		4th	T_ID1[7:0] =8'hFF (Note2)	T_ID1[7:0] =8'hFF (Note2)	T_ID1[7:0] =8'hFF (Note2)
		5th	T_ID2[15:8] =8'hFF (Note2)	T_ID2[15:8] =8'hFF (Note2)	T_ID2[15:8] =8'hFF (Note2)
		6th	T_ID2[7:0] =8'hFF (Note2)	T_ID2[7:0] =8'hFF (Note2)	T_ID2[7:0] =8'hFF (Note2)
E8h	EEPROM Write Enable	None	Disabled	Disabled	Disabled
E9h	EEPROM Write Disable	None	Disabled	Disabled	Disabled
EAh	EEPROM Word Write	1st	DW[15:8] =8'h00	DW[15:8] =8'h00	DW[15:8] =8'h00
		2nd	DW[7:0] =8'h00	DW[7:0] =8'h00	DW[7:0] =8'h00
EBh	EEPROM Word Read	1st	DR[15:8] =8'h00	DR[15:8] =8'h00	DR[15:8] =8'h00
		2nd	DR[7:0] =8'h00	DR[7:0] =8'h00	DR[7:0] =8'h00
ECh	EEPROM Address Set	1st	A[7:0]=8'h00	A[7:0]=8'h00	A[7:0]=8'h00

Note 1: If external EEPROM is used (EEPROME=VCC), data is loaded from the EEPROM. If external EEPROM is not used (EEPROME=GND), data is same as before executing soft_reset command.

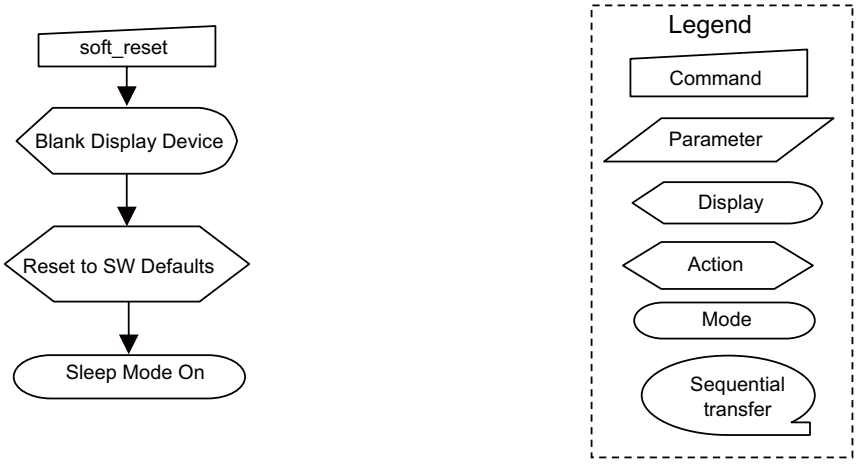
Note 2: If user writes VCM register value, Supplier ID and Supplier Elective Data to the NVM, the values are set as default.

User Command

nop : 00h

00h	nop												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	0	0	0	0	00h
Parameter	None												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read. X = Don't Care												
Restriction	-												
Flow Chart	-												

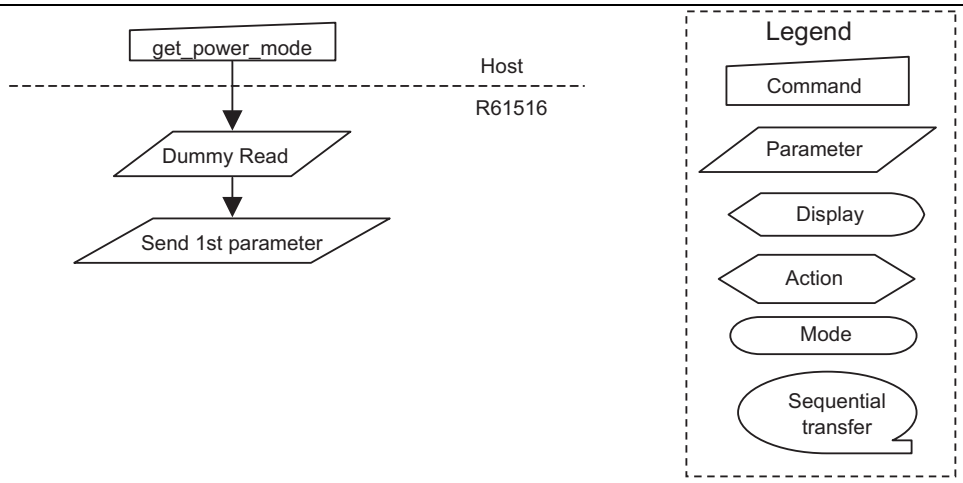
soft_reset: 01h

01H	soft_reset												
	DCX	RDX	WRX	DB 17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	0	0	0	1	01h
Parameter	None												
Description	The display module performs a software reset. Commands and parameters are written with their SW Reset default values. (See “Default Modes and Values”.) Note: The Frame Memory contents are unaffected by this command. X = Don’t care												
Restriction	If a soft_reset is sent when the display module is in Sleep Mode, the host processor must wait 120 milliseconds before sending an exit_sleep_mode command. soft_reset should not be sent during exit_sleep_mode sequence. The R61516 reads data in external EEPROM when external EEPROM is used (EEPROM=1) at software reset. No new command setting is allowed until the R61516 enters the Sleep Mode. See “State & Command sequence” for sequence to enter Sleep Mode. If a soft_reset is sent when the display module is in Sleep Mode, data in NVM and EEPROM are read. No new command setting is inhibited when data is read (5ms).												
Flow Chart													

get_power_mode: 0Ah

0Ah	get_power_mode												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	0	1	0	1	0	0Ah
1st parameter	1	↑	1	x	0	IDMON	PTLON	SLPOUT	NORON	DSPON	0	0	xx
Description	The display module returns the current power mode.												

Bit	Description	Comment	Command list Symbol
D7	Reserved	Set to “0”	-
D6	Idle Mode On/Off		IDMON
D5	Partial Mode On/Off		PTLON
D4	Sleep Mode On/Off		SLPOUT
D3	Display Normal Mode On/Off		NORON
D2	Display On/Off		DSPON
D1	Reserved	Set to “0”	-
D0	Reserved	Set to “0”	-

0Ah	get_power_mode
	• Bit D7 – Not defined This bit is not applicable. Set to “0”. • Bit D6 – Idle Mode On/Off ‘0’ = Idle Mode Off. ‘1’ = Idle Mode On. • Bit D5 – Partial Mode On/Off ‘0’ = Partial Mode Off. ‘1’ = Partial Mode On. • Bit D4 – Sleep Mode On/Off ‘0’ = Sleep Mode On ‘1’ = Sleep Mode Off • Bit D3 – Display Normal Mode On/Off ‘0’ = Display Normal Mode Off ‘1’ = Display Normal Mode On • Bit D2 – Display On/Off ‘0’ = Display is Off ‘1’ = Display is On • Bit D1 – Not Defined This bit is not applicable. Set to “0”. • Bit D0 – Not Defined This bit is not applicable. Set to “0”. X = Don’t care.
Restriction	-
Flow chart	

get_address_mode: 0Bh

<table>
<tr><td>0Bh</td><td colspan="13">get_address_mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB17-8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0Bh</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>0</td><td>0</td><td>0</td><td>B0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="13">The display module returns the current status of the display as described in the table below. This command setting depends on set_address_mode (36h).
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list symbol</th></tr>
<tr><td>D7</td><td>Page Address Order</td><td></td><td>B7</td></tr>
<tr><td>D6</td><td>Column Address Order</td><td></td><td>B6</td></tr>
<tr><td>D5</td><td>Page/column Order</td><td></td><td>B5</td></tr>
<tr><td>D4</td><td>Line Address Order</td><td></td><td>B4</td></tr>
<tr><td>D3</td><td>RGB/BGR Order</td><td>Set to “0”</td><td></td></tr>
<tr><td>D2</td><td>Display Data Latch Order</td><td>Set to “0”</td><td></td></tr>
<tr><td>D1</td><td>Reserved</td><td>Set to “0”</td><td></td></tr>
<tr><td>D0</td><td>Switching between Common outputs and Frame Memory</td><td></td><td>B0</td></tr>
</table>

Bit D7 - Page Address Order

‘0’ = Top to Bottom (When set_address_mode D7 = ’0’)
‘1’ = Bottom to Top (When set_address_mode D7 = ‘1’)

Bit D6 – Column Address Order

‘0’ = Left to Right (When set_address_mode D6 = ‘0’)
‘1’ = Right to Left (When set_address_mode D6 = ‘1’)

Bit D5 – Page/column Order

‘0’ = Normal Mode (When set_address_mode D5 = ‘0’)
‘1’ = Reverse Mode (When set_address_mode D5 = ‘1’)
Note: See “Host Processor to Memory Write/Read Directuin” and “Memory Access Control” for D7 to D5 bits.

Bit D4 – Line Address Order

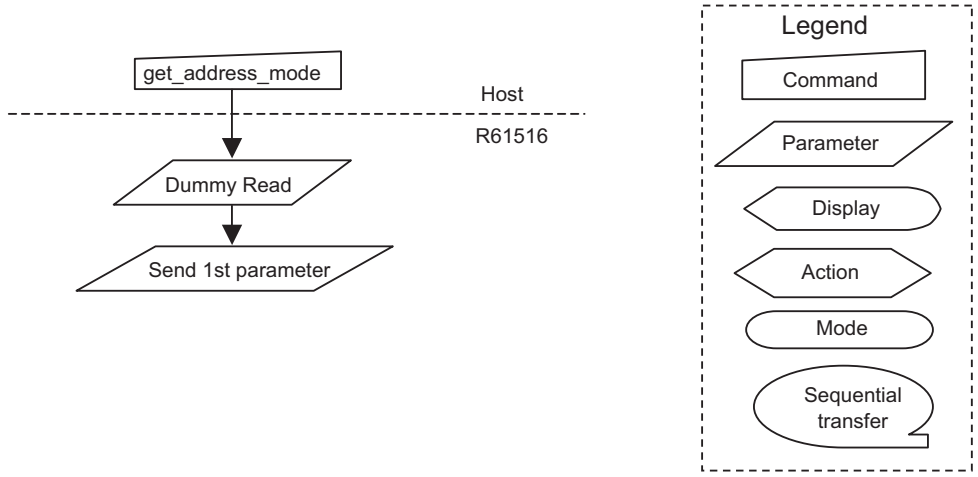
‘0’ = LCD Refresh Top to Bottom (When set_address_mode = ‘0’ (D4))
‘1’ = LCD Refresh Bottom to Top (When set_address_mode = ‘1’ (D4))
Note: See “Memory Access Control (36h)” for D4 bit.

Bit D3 – RGB/BGR Order

This bit is not applicable. Set to “0” (Not supported).

Bit D2 – Display Data latch Data Order

This bit is not applicable. Set to “0” (Not supported).</td></tr>
</table>

0Bh	get_address_mode
Description	• Bit D1 – Not Defined This bit is not applicable. Set to “0” (Not supported). • Bit D0 – Switching between Common outputs and FrameMemory ‘0’ = Reading direction from FrameMemory to Common Outputs is identical with writing direction. ‘1’ = Reading direction from FrameMemory to Common Outputs is reverse of writing direction. X = Don’t care.
Restriction	-
Flow Chart	

Note: See “”State Transition Diagram” for display mode transition.

get_pixel_format: 0Ch

0Ch	get_pixel_format												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	0	1	1	0	0	0Ch
1st parameter	1	↑	1	x	0	D6	D5	D4	0	D2	D1	D0	xxh

Description

This command indicates the current status of the display as described in the table below. This command setting depends on set_pixel_format (3Ah).

Bit	Description	Comment
D7	DPI Pixel format	Set to "0"
D6	(RGB Interface Colour Format)	D6
D5		D5
D4		D4
D3	DBI Pixel Format	Set to "0"
D2	(Control Interface Colour Format)	D2
D1		D1
D0		D0

- Bit D[6:4] – DPI Pixel Format (RGB Interface Color Format Selection)
- Bit D[2:0] – DBI Pixel Format (Control Interface Colour Format Selection)
- Bit D7 and D3 - These bits are not applicable to this project, so they are set to "0". See description of command set_pixel_format (3Ah).

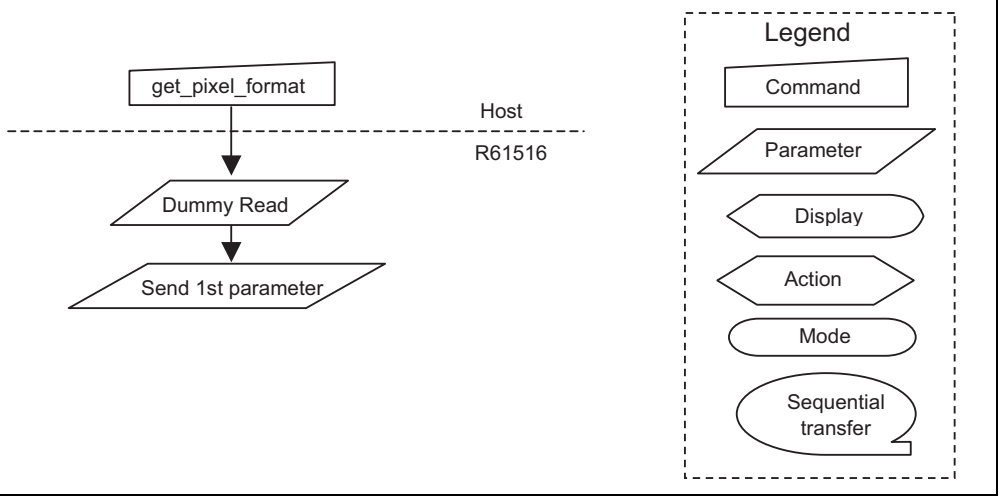
Control Interface Colour Format	D6/D2	D5/D1	D4/D0
Setting disasbled	0	0	0
3bit/pixel (8 colors)	0	0	1
Setting disasbled	0	1	0
Setting disasbled	0	1	1
Setting disasbled	1	0	0
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,1444 colors)	1	1	0
Setting disabled	1	1	1

x = Don't care

Note) In DPI operation, set D bit as following combination with RIM bit in 5th parameter of Frame Mmoery Access and Interface Setting (B3h). No other setting is inhibited.

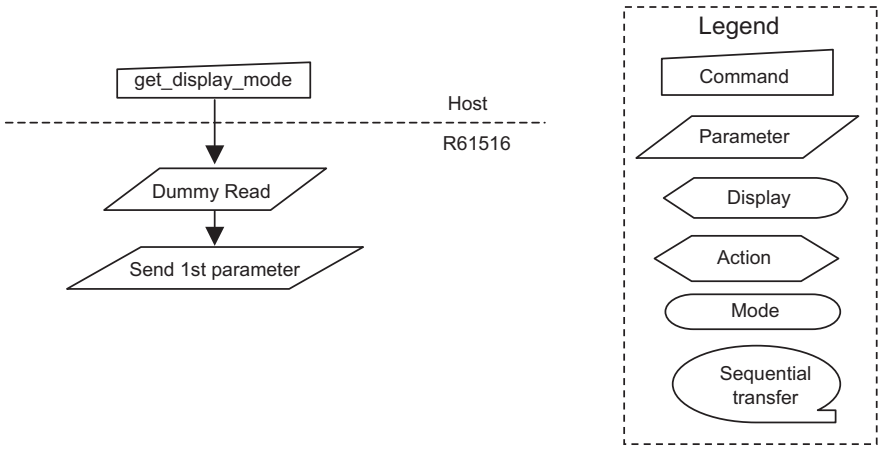
RIM=2'h1 (16 bit color format) D [6:4]=3'h5

RIM=2'h2 (18 bit color format) D [6:4]=3'h6

0Ch	get_pixel_format
Flow chart	

get_display_mode: 0Dh

<table>
<tr><td>0Dh</td><td colspan="13">get_display_mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB17-8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0Dh</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>VSSON</td><td>0</td><td>DSPINVON</td><td>0</td><td>0</td><td>0</td><td>0</td><td>x</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="13">The display module returns the current status of the display as described in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Command list symbol</th></tr>
<tr><td>D7</td><td>Vertical Scrolling Status</td><td></td><td>VSSON</td></tr>
<tr><td>D6</td><td>Reserved</td><td>Set to “0”</td><td></td></tr>
<tr><td>D5</td><td>Inversion ON/OFF</td><td></td><td>DSPINVON</td></tr>
<tr><td>D4</td><td>Reserved</td><td>Set to “0”</td><td></td></tr>
<tr><td>D3</td><td>Reserved</td><td>Set to “0”</td><td></td></tr>
<tr><td>D2</td><td>Gamma Curve Selection</td><td>Set to “0”</td><td></td></tr>
<tr><td>D1</td><td>Gamma Curve Selection</td><td>Set to “0”</td><td></td></tr>
<tr><td>D0</td><td>Gamma Curve Selection</td><td>Set to “0”</td><td></td></tr>
</table>
• Bit D7 –Vertical Scrolling On/Off
‘0’ = Vertical Scrolling is Off
‘1’ = Vertical Scrolling is On
• Bit D6 – Reserved
This bit is not applicable. Set to “0”.
• Bit D5 – Inversion On/Off
‘0’ = Inversion is Off
‘1’ = Inversion is On
• Bit D4, D3 – Reserved
This bit is not applicable. Set to “0”.
• Bit D2, D1, D0 – Gamma Curve Selection
This bit is not applicable. Set to “0”.
x = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
</table>

0Dh	get_display_mode
Flow Chart	

get_signal_mode: 0Eh

0Eh	get_signal_mode												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	0	1	1	1	0	0Eh
1st parameter	1	↑	1	x	TEON	TELOM	0	0	0	0	0	0	xx

Description: The display module returns the Display Signal Mode as described in the table below.

Bit	Description	Comment	Command list symbol
D7	Tearing Effect line ON/OFF		TEON
D6	Tearing Effect line Output Mode		TELOM
D5	Reserved	Set to "0"	-
D4	Reserved	Set to "0"	-
D3	Reserved	Set to "0"	-
D2	Reserved	Set to "0"	-
D1	Reserved	Set to "0"	-
D0	Reserved	Set to "0"	-

- Bit D7 – Tearing Effect Line On/Off

  '0' = Tearing Effect Line Off
  '1' = Tearing Effect On

- Bit D6 – Tearing Effect Line Output Mode (See "set_tear_on: 35h).

  '0' = Mode1
  '1' = Mode2

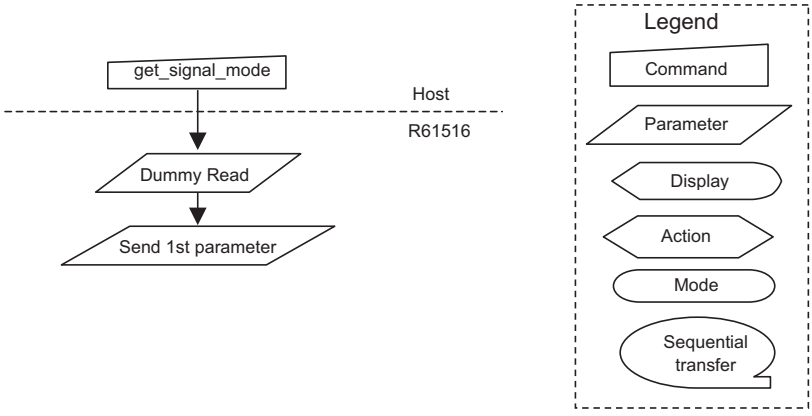
- Bit D5-D0 – Reserved

  These bits are not applicable. Set to "0".

X = Don't care

Restriction: -

Flow Chart



get_diagnostic_result:0Fh

0Fh	get_diagnostic_result												
	D/CX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	0	1	1	1	1	0Fh
1st Parameter	0	↑	1	x	SDR	FUNCD	0	0	0	0	0	0	xx

Description

Bit	Description	Comment	Command List Symbol
D7	Register Loading Detection		SDR
D6	Functionality Detection		FUNCD
D5	Chip Attachment Detection	Read 0	-
D4	Display Glass Break Detection	Read 0	-
D3	Not used	Read 0	-
D2	Not used	Read 0	-
D1	Not used	Read 0	-
D0	Not used	Read 0	-

The display module returns the self-diagnostic results following a Sleep Out command as shown in the table above.

・Bit D7 – Register Loading Detection

・Bit D6 – Functionality Detection

Note: See Self Diagnostic Function for D7 and D6.

・ Bit D5 – Chip Attachment Detection

This bit is not applicable. Set to “0”.

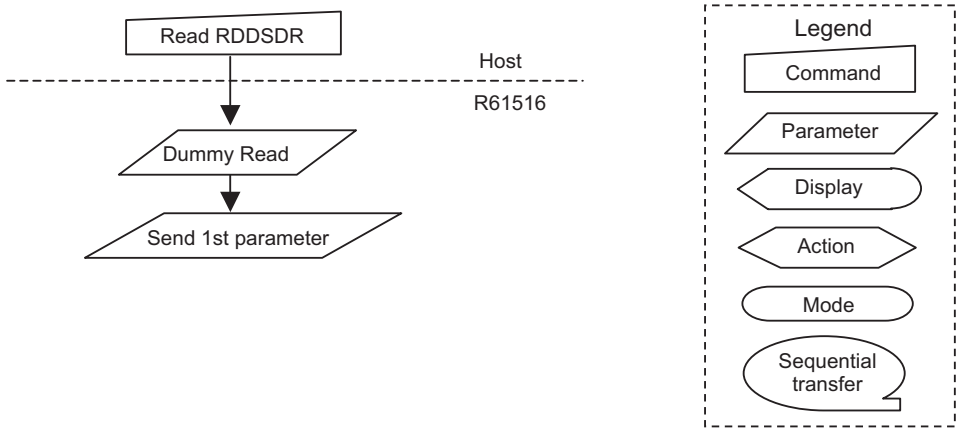
・Bit D4 –Display Glass Break Detection

This bit is not applicable. Set to “0”.

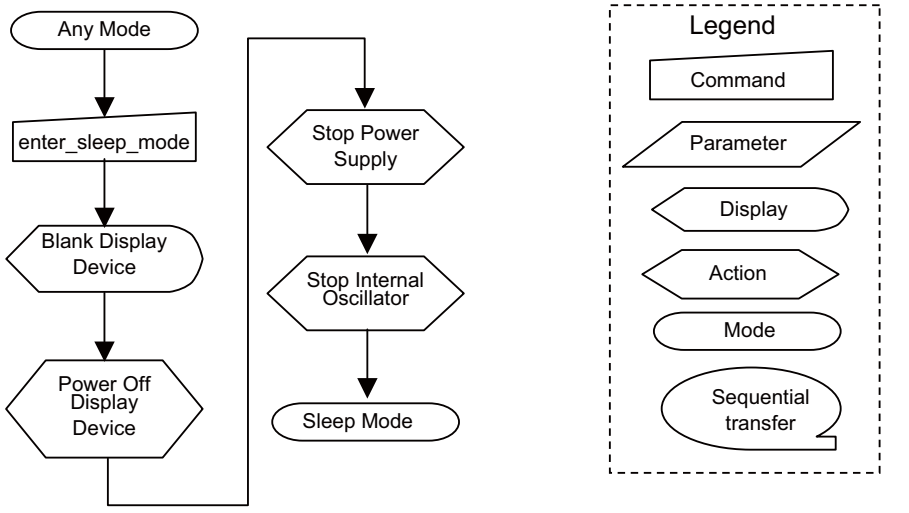
・Bit D3, D2, D1, D0 – Reserverd. Set to 0.

X = Don’t care

Restriction: -

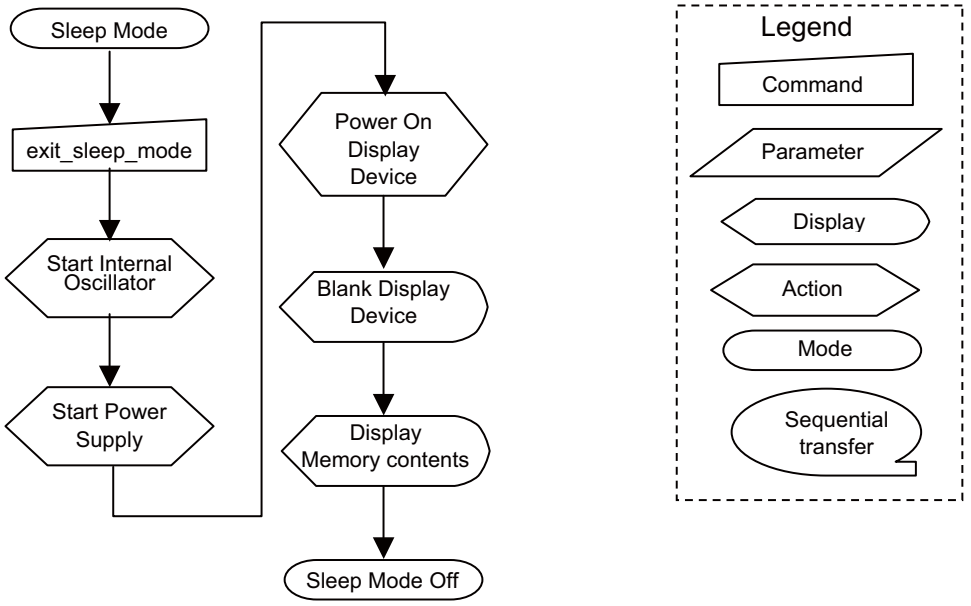
0Fh	get_diagnostic_result
Flow Chart	

enter_sleep_mode: 10h

10h	enter_sleep_mode												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	1	0	0	0	0	10h
Parameter	None												
Description	This command causes the LCD module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop. See “State & Command sequence” for Sleep In sequence. DBI remains operational and the memory maintains its contents. See State Transition Diagram for each stage of transition. X = Don’t care												
Restriction	This command has no effect when the module is already in Sleep mode. Sleep mode can be exited only when the exit_sleep_mode (11h) is transmitted. Sending a new command is prohibited while the R61516 performs either power supply OFF sequencer or blank scan.												
Flow Chart													

exit_sleep_mode: 11h

11h	exit_sleep_mode												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	1	0	0	0	1	11h
Parameter	None												
Description	This command causes the display module to exit Sleep mode. DC/DC converter, internal oscillation and panel scanning start. See “State & Command sequence” for exit_sleep_mode. See State Transition Diagram for each stage of transition. X = Don’t care												
Restriction	This command shall not cause any visual effect on display device when the display module is not in Sleep mode. No new command setting is allowed during EEPROM data load operation and power supply ON sequence. Operation may continue for more than 120msec duie to power supply ON sequence setting. Do not send any command also in this case. The host processor must waitn 120 milliseconds after sending an enter_sleep_mode command before sending an exit_sleep_mode command . External EEPROM is read again when exit_sleep_mode command is written during Sleep Mode. When this operation is completed and sleep mode is already exited, there is no undesireble image on the panel if registers set to the default value at the shipment from the plant. The display runs the self-diagnostic function after this command is received.												

11h	exit_sleep_mode
Flow Chart	

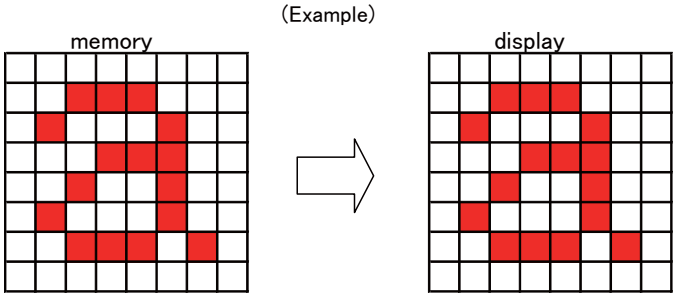
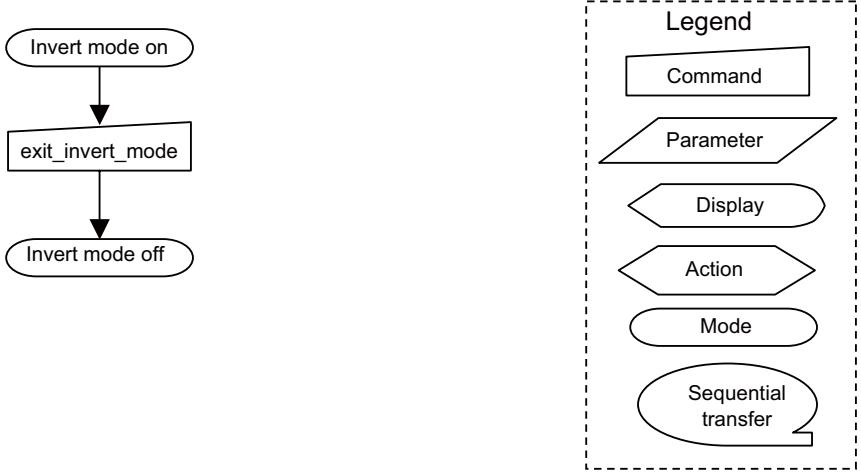
enter_partial_mode: 12h

12h	enter_partial_mode: 12h												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	1	0	0	1	0	12h
Parameter	None												
Description	This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the set_partial_area command (30h). To leave Partial Display Mode, the enter_normal_mode (13h) should be written. X=Don't care Note: When a command breaks in the middle of frame period in Normal mode, the command is enabled from the next frame period.												
Restriction	This command has no effect when the module is already in Partial mode. This command causes scrolling function disabled.												
Flow Chart	See set_partial_area (30h).												

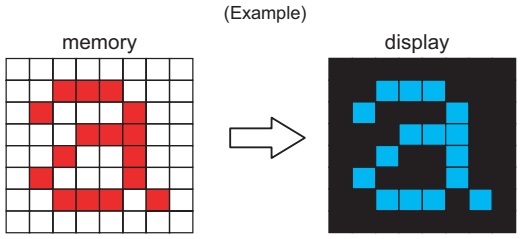
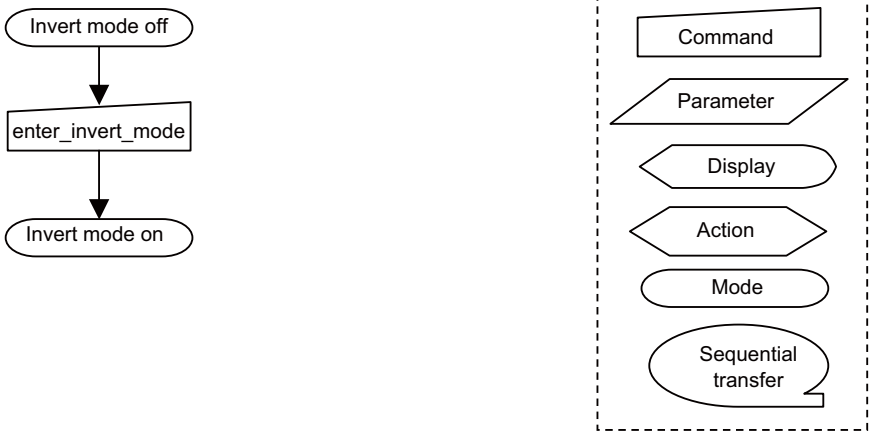
enter_normal_mode: 13h

13h	enter_normal_mode												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	1	0	0	1	1	13h
Parameter	None												
Description	This command causes the display module to enter the Normal mode. Normal Mode is defined as Partial mode and Scroll mode are off. X = Don't care Note: When a command breaks in the middle of frame period in Partial mode, that command becomes valid from the next frame period.												
Restriction	This command has no effect when Normal Display mode is already active.												
Flow Chart	See the descriptions of commands set_partial_area (30h) and set_scroll_area (33h) when using this command.												

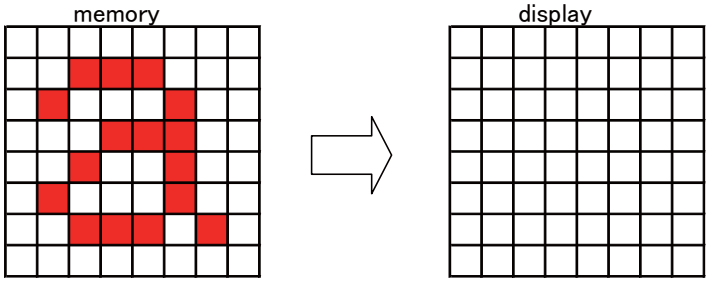
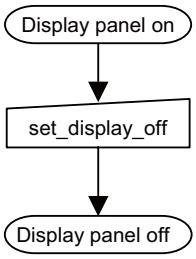
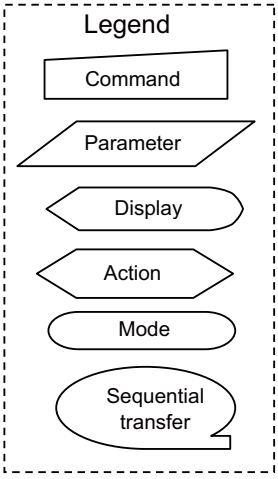
exit_invert_mode: 20h

20h	exit_invert_mode												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	0	0	0	0	0	20h
Parameter	None												
Description	This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. (Example) memory display  X = Don't care												
Restriction	This command has no effect when the module is already in Inversion is off.												
Flow Chart													

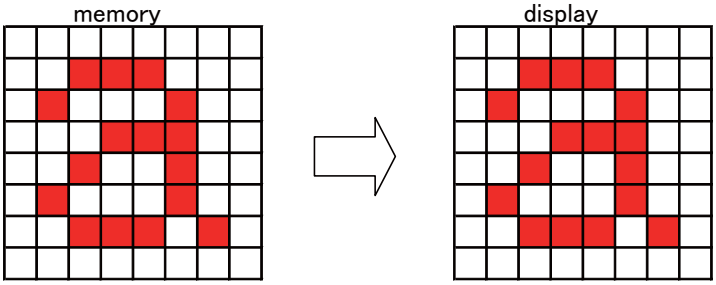
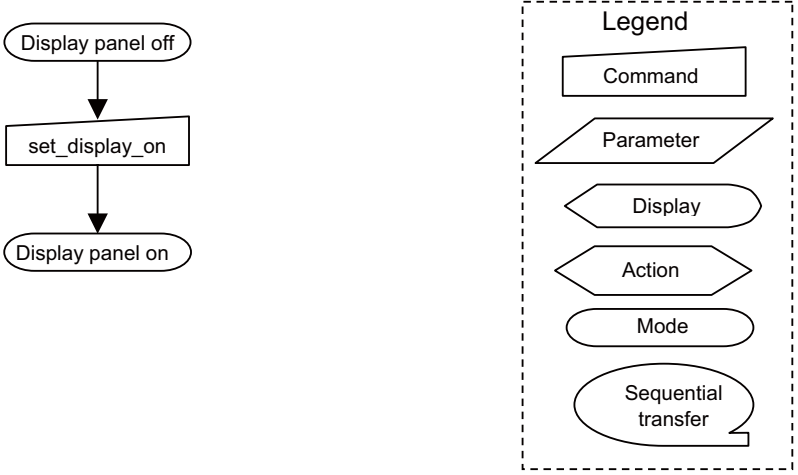
enter_invert_mode: 21h

21h	enter_invert_mode												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	0	0	0	0	1	21h
Parameter	None												
Description	This command causes the display module to invert the image data only on the display device. The frame memory contents remain unchanged. All bits send from the frame memory to the display invert. No status bits are changed.  X = Don't care												
Restriction	This command has no effect when the display module is already inverting the display image.												
Flow Chart	 												

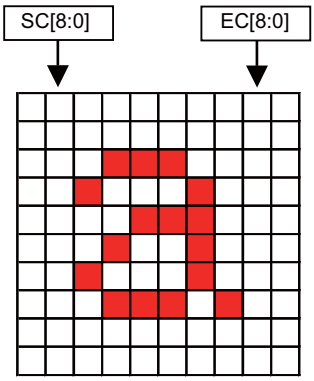
set_display_off: 28h

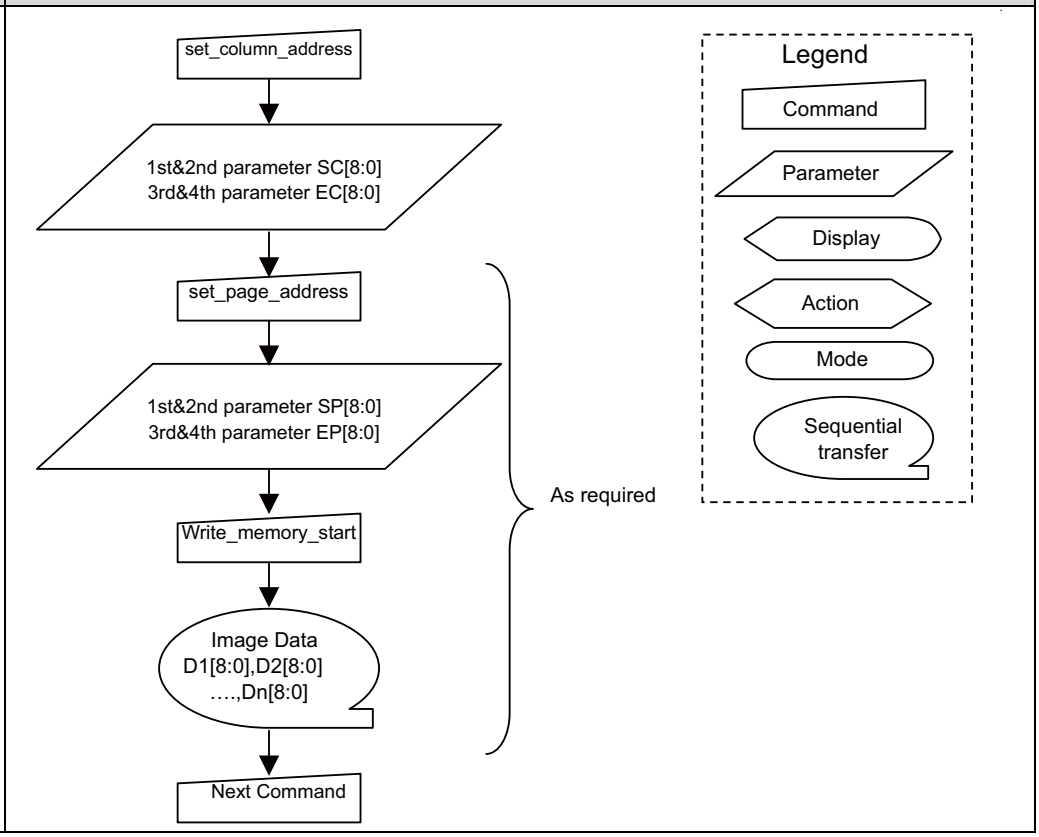
28h	set_display_off												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	0	1	0	0	0	28h
Parameter	None												
Description	This command causes the display module to stop displaying the imag edata on the display device. The frame memory contents remain unchanged. No status bits are changed. (Example) memory display  See PTS bit table in C0h description. X = Don't care												
Restriction	This command has no effect when the display panel is already off.												
Flow Chart	  												

set_display_on: 29h

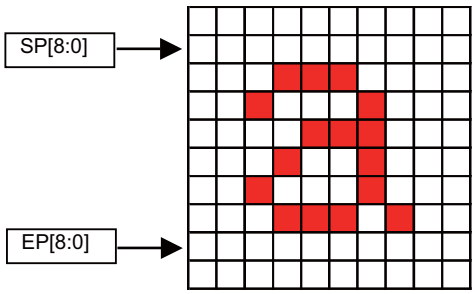
29h	**set_display_on**												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	1	0	1	0	0	1	29h
Parameter	None												
Description	This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. (Example) memory display  X = Don't care												
Restriction	This command has no effect when the display panel is already on.												
Flow Chart													

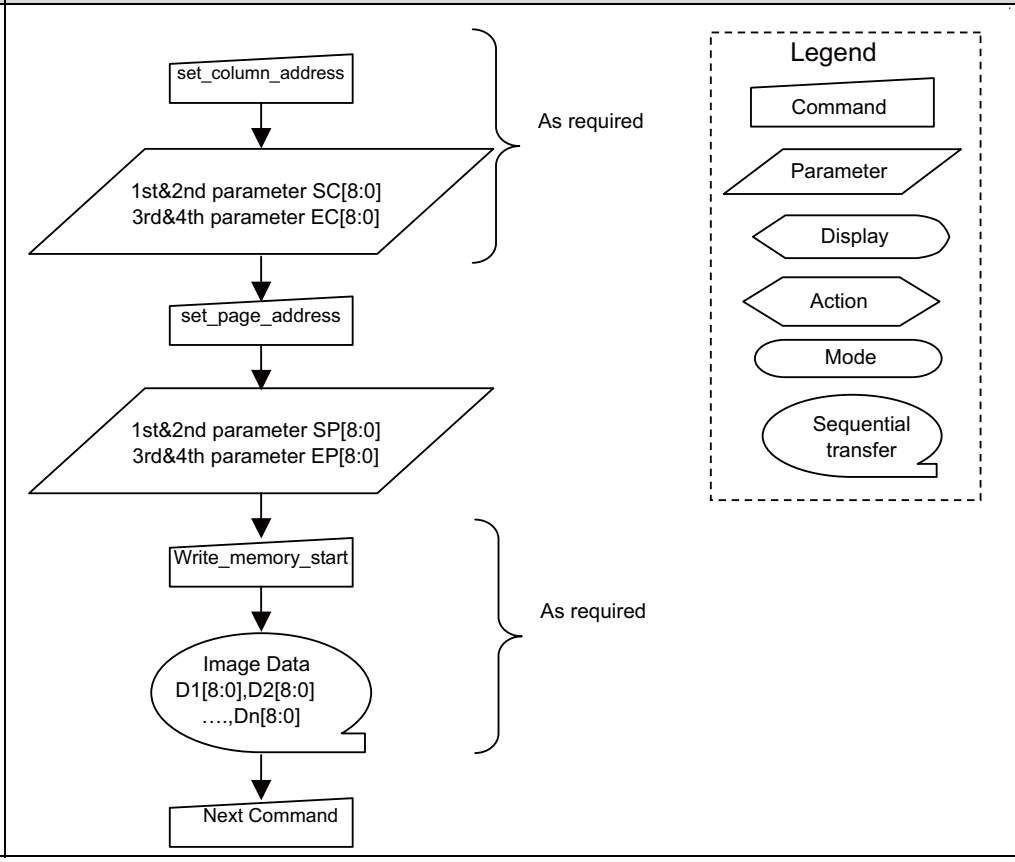
set_column_address: 2Ah

2Ah	set_column_address												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	0	1	0	1	0	2Ah
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	SC[8]	-
2nd parameter	1	1	↑	x	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]	-
3rd parameter	1	1	↑	x	0	0	0	0	0	0	0	EC[8]	-
4th parameter	1	1	↑	x	EC[7]	EC[6]	EC[5]	EC[4]	EC[3]	EC[2]	EC[1]	EC[0]	-
Description	This command defines the column extent of the frame memory accessed by the host processor. The values of SC[8:0] and EC[8:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. No status bits are changed. Example  X=Don't care.												
Restriction	SC [8:0] must be equal to or less than EC[8:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in following cases. • If set_address_mode B5 = 0: SC[7:0] or EC[7:0] > 0EFh • If set_address_mode B5 = 1: SC[8:0] or EC[8:0] > 13Fh												

2Ah	set_column_address
Flow Chart	

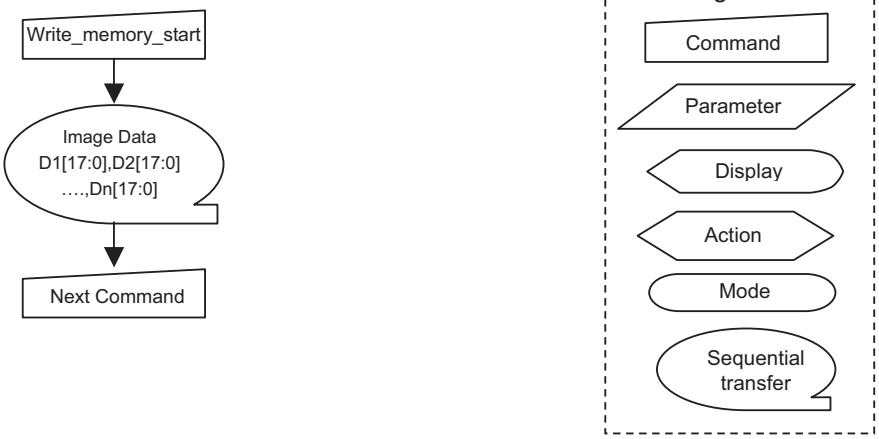
set_page_address: 2Bh

2Bh	set_page_address												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	0	1	0	1	1	2Bh
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	SP[8]	-
2nd parameter	1	1	↑	x	SP[7]	SP[6]	SP[5]	SP[4]	SP[3]	SP[2]	SP[1]	SP[0]	-
3rd parameter	1	1	↑	x	0	0	0	0	0	0	0	EP[8]	-
4th parameter	1	1	↑	x	EP[7]	EP[6]	EP[5]	EP[4]	EP[3]	EP[2]	EP[1]	EP[0]	-
Description	This command defines the page extent of the frame memory accessed by the host processor. No status bits are changed. The values of SP[8:0] and EP[8:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. Example  X=Don't care												
Restriction	SP[8:0] must always be equal to or less than EP[8:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in following cases. • If set_address_mode B5 = 0: SP[8:0] or EP[8:0] > 13Fh • If set_address_mode B5 = 1: SP[7:0] or EP[7:0] > 0EFh												

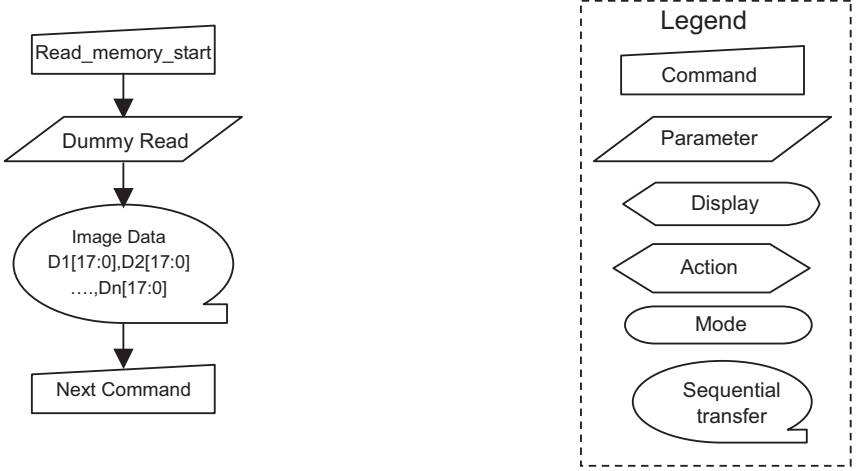
2Bh	set_page_address
Flow Chart	

write_memory_start: 2Ch

2Ch	write_memory_start												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	0	1	1	0	0	2Ch
1st parameter	1	1	↑	D1 [17:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000… 3FF
: :	1	1	↑	Dx [17:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000… 3FF
Nth parameter	1	1	↑	Dn [17:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000… 3FF
Description	This command transfers image data from the host processor to the display module's frame memory. No status bits are changed. If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively. After pixel data I is stored in frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction". If Frame Memory Access and Interface setting (B3h) WEMODE = 0: If the number of pixels in transfer data exceeds (EC-SC+1)*(EP-SP+1), the extra pixels are ignored. If Frame Memory Access and Interface setting (B3h) WEMODE = 1 When the number of pixels in transfer data exceeds (EC-SC+1)*(EP-SP+1), the column register and the page register are set to the Start Column and Start Page respectively. Then subsequent data is written to the frame memory. Sending any other command will stop writing to the frame memory. See DBI Data Format and DPI Data Format for write data formats in DBI Type B 18-/ 16-/ 9- /8- bit bus interface, Type C serial interface, and DPI. X=Don't care.												
Restriction	In all color modes, there are no restrictions on the length of parameters.												

2Ch	write_memory_start
Flow Chart	

read_memory_start: 2Eh

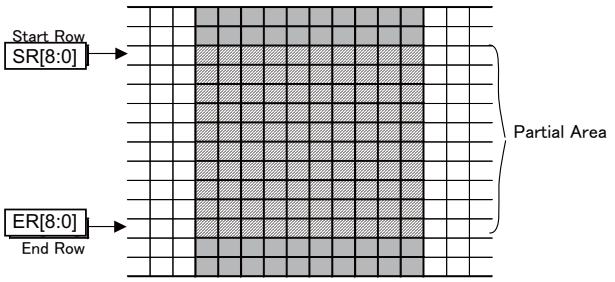
2Eh	**read_memory_start**												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	0	1	1	1	0	2Eh
1st parameter	1	↑	1	D1 [17:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000… 3FF
:	1	↑	1	Dx [17:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000… 3FF
Nth parameter	1	↑	1	Dn [17:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000… 3FF
Description	This command transfers image data from the frame memory to the host processor. No status bits are changed. If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively. After pixel data I is read from the frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction". If read operation continued after (EP, EC) data is read, the last data (EP, EC) continues to be read. Any other written command stops frame memory read. See DBI Data Format and DPI Data Format for write data formats in DBI Type B 18-/ 16-/ 9- /8- bit bus interface, Type C serial interface and DPI operations. X = Don't care.												
Restriction	In all color modes, the Frame read is always 18 bits so there is no restriction on the length of parameters.												
Flow Chart													

set_partial_area: 30h

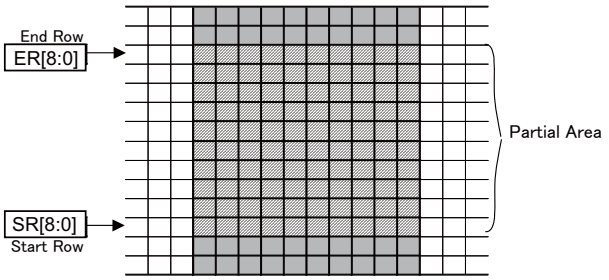
30h	set_partial_area												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	0	0	0	0	30h
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	SR[8]	000… 13F
2nd parameter	1	1	↑	x	SR[7]	SR[6]	SR[5]	SR[4]	SR[3]	SR[2]	SR[1]	SR[0]	
3rd parameter	1	1	↑	x	0	0	0	0	0	0	0	ER[8]	000… 13F
4th parameter	1	1	↑	x	ER[7]	ER[6]	ER[5]	ER[4]	ER[3]	ER[2]	ER[1]	ER[0]	

30h	set_partial_area
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

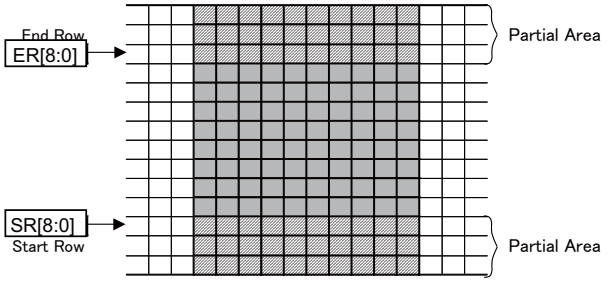
End Row > Start Row (set_address_mode(36h) B4=0)



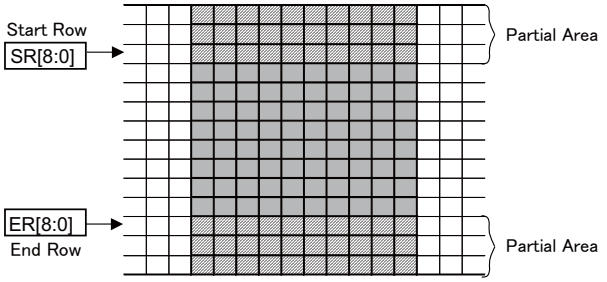
End Row > Start Row(set_address_mode(36h) B4=1)



End Row < Start Row (set_address_mode(36h) B4=0)

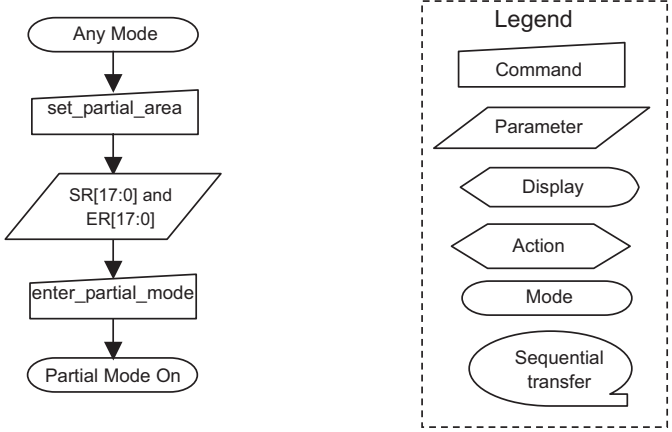
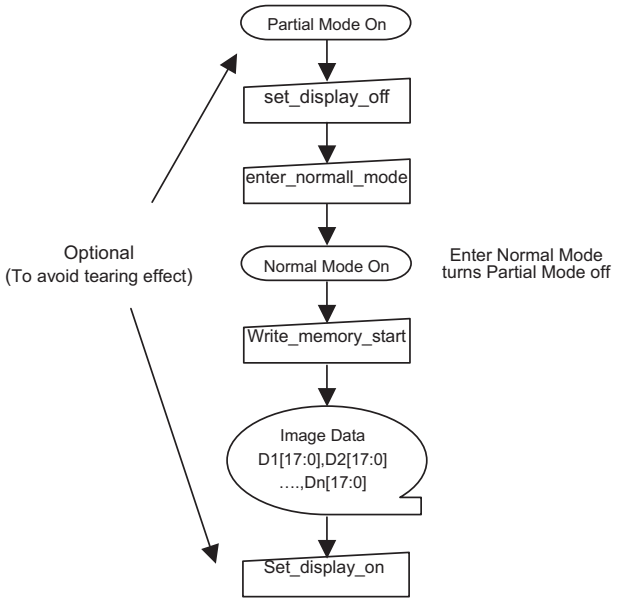


End Row < Start Row (set_address_mode(36h) B4=1)



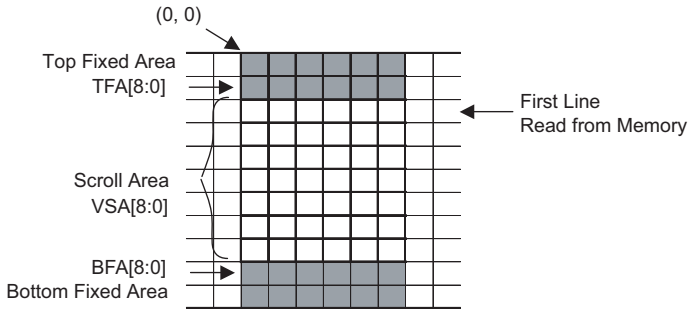
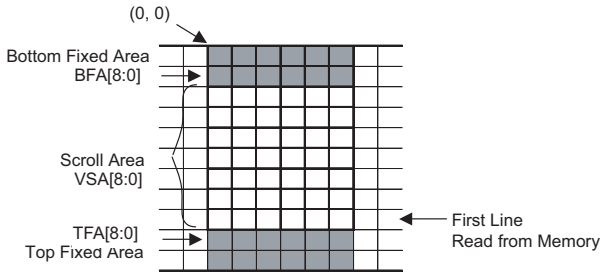
If End Row = Start Row, the partial area will be one row deep.

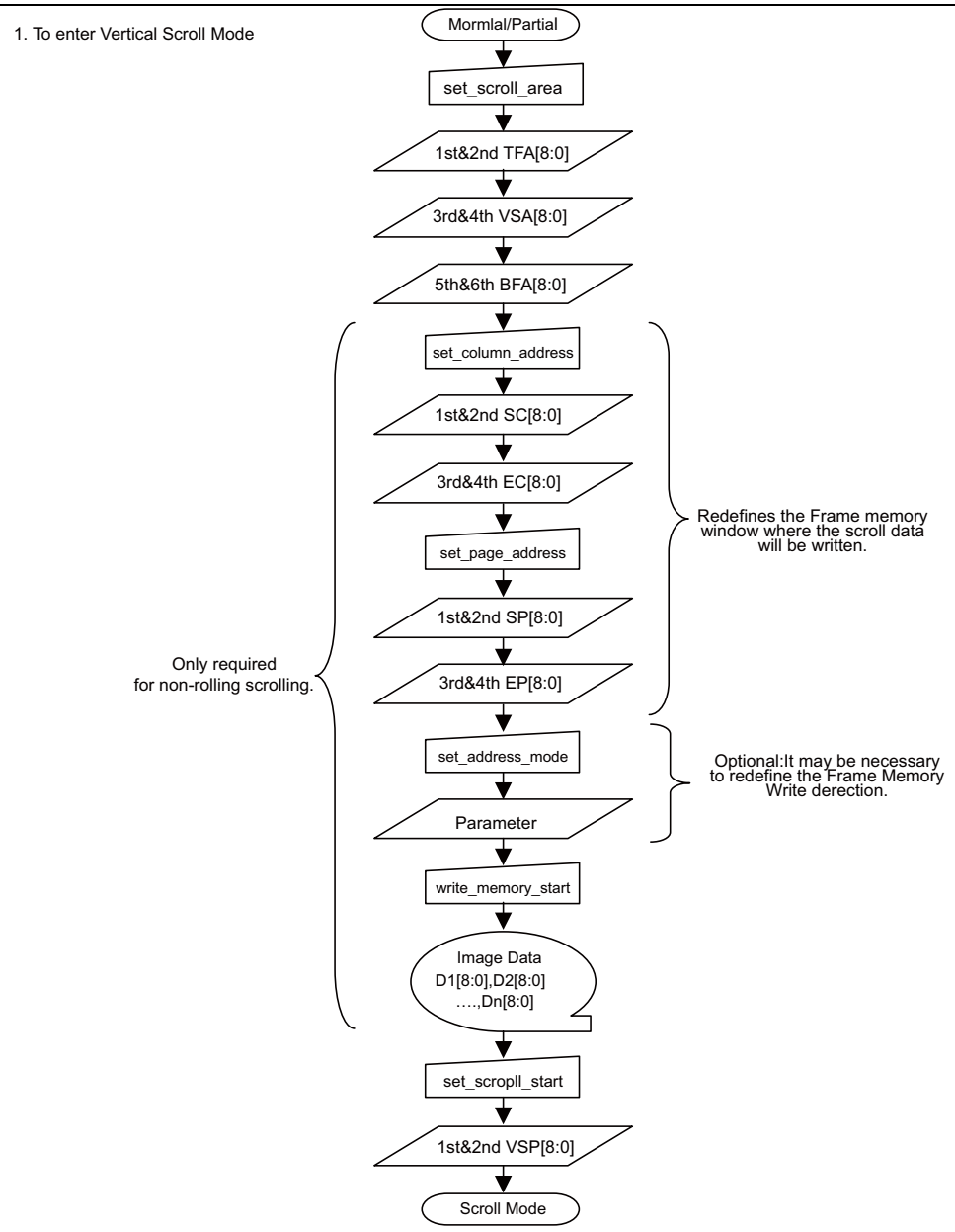
X = Don't care.

30h	set_partial_area
Restriction	SR[8:0] and ER[8:0] must not be greater than 13Fh. The bits other than SR[8:0] and ER[8:0] are “Don’t care”.
Flow Chart	1. To enter Partial mode  2.To exit Partial mode 

set_scroll_area: 33h

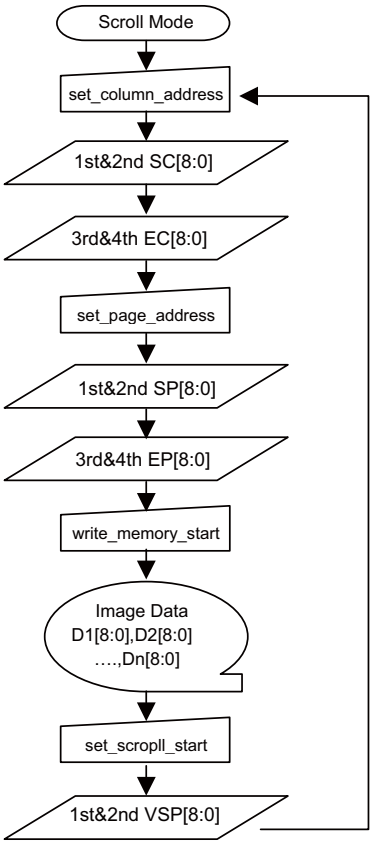
33h	set_scroll_area												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	0	0	1	1	33h
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	TFA [8]	000 … 140
2nd parameter	1	1	↑	x	TFA [7]	TFA [6]	TFA [5]	TFA [4]	TFA [3]	TFA [2]	TFA [1]	TFA [0]	
3rd parameter	1	1	↑	x	0	0	0	0	0	0	0	VSA [8]	000 … 140
4th parameter	1	1	↑	x	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]	
5th parameter	1	1	↑	x	0	0	0	0	0	0	0	BFA [8]	000 … 140
6th parameter	1	1	↑	x	BFA [7]	BFA [6]	BFA [5]	BFA [4]	BFA [3]	BFA [2]	BFA [1]	BFA [0]	

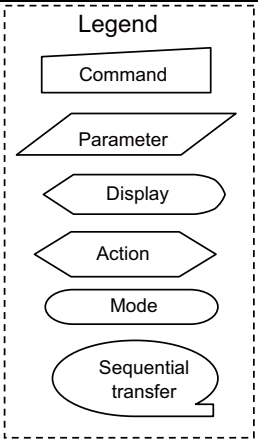
33h	set_scroll_area
Description	This command defines the display module's Vertical Scrolling Area. If set_address_mode (36h) B4 = 0: The 1st and 2nd parameters TFA[8:0] describe the Top Fixed Area in number of lines from the top of the frame memory. The 3rd and 4th parameters VSA[8:0] describe the hight of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of Vertical Scrolling Area starts immediately after theTop Fixed Area. The last line of the Vertical Scrolling Area ends immediately the top most line of the Bottom Fixed Area. The 5th and 6th parameters BFA[8:0] describe the Bottom Fixed Area in number of lines from the top of the frame memory. Set the number of lines from the bottom of the frame memory. TFA, VSA and BFA refer to the frame memory line pointer.  If set_address_mode (36h) B4 = 1: The 1st and 2nd parameters TFA[8:0] describe the Top Fixed Area in number of lines from the top of the frame memory. The 3rd and 4th parameters VSA[8:0] describe the hight of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of Vertical Scrolling Area starts immediately after theTop Fixed Area. The last line of the Vertical Scrolling Area ends immediately the top most line of the Bottom Fixed Area. The 5th and 6th parameters BFA[8:0] describe the Bottom Fixed Area in number of lines from the top of the frame memory. Set the number of lines from the bottom of the frame memory. TFA, VSA and BFA refer to the frame memory line pointer.  TFA, VSA and BFA refer to the frame memory line pointer.

33h	set_scroll_area
Restriction	The sum of TFA, VSA and BFA must equal the number of the display device's horizontal lines (pages). In Vertical Scroll Mode, set_address_mode B5 should be set to '0' and this only affects the Frame Memory Write.
Flow Chart	

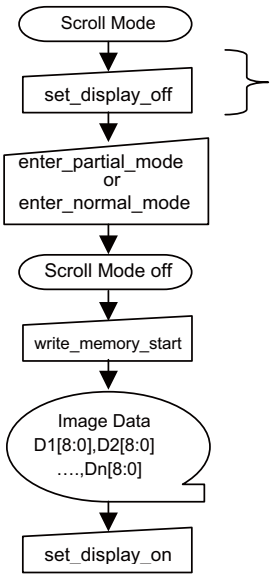
Since the value of the Vertical Scrolling Start Address is absolute with reference to the Frame Memory, it must not enter the fixed areas, otherwise an undesirable image may be shown on the Display Panel.

33h	set_scroll_area
Flow Chart	2. Continuous Scroll



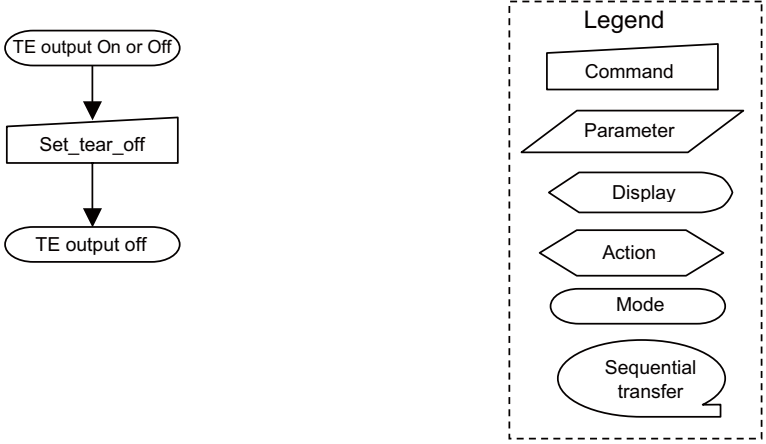


3. To exit Vertical Scroll Mode

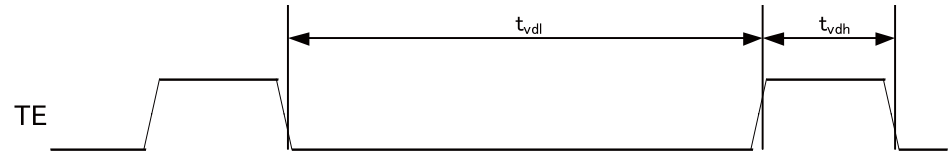
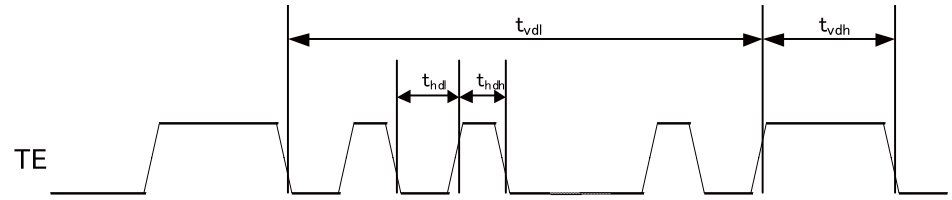


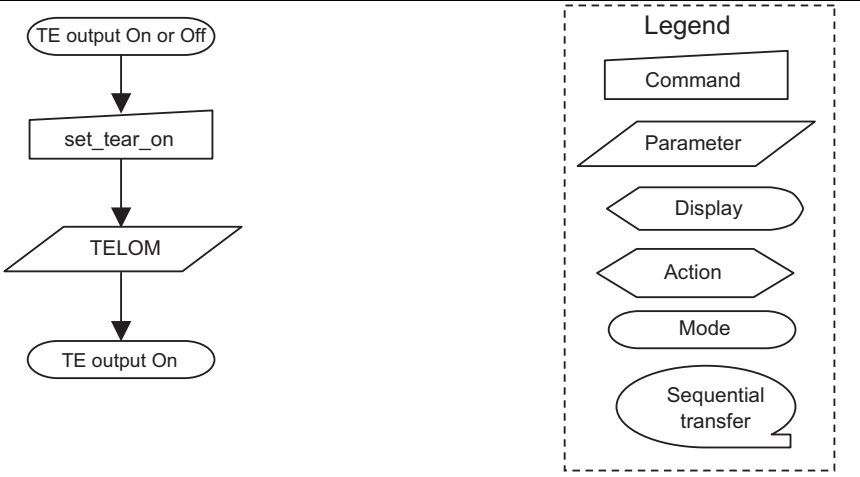
Optional:To prevent Tearing Effect Image displayed.

set_tear_off: 34h

34h	set_tear_off												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	0	1	0	0	34h
Parameter	None												
Description	This command turns off the Tearing Effect output signal from the TE signal line. X = Don't care												
Restriction	This command has no effect when Tearing Effect output is already off.												
Flow Chart													

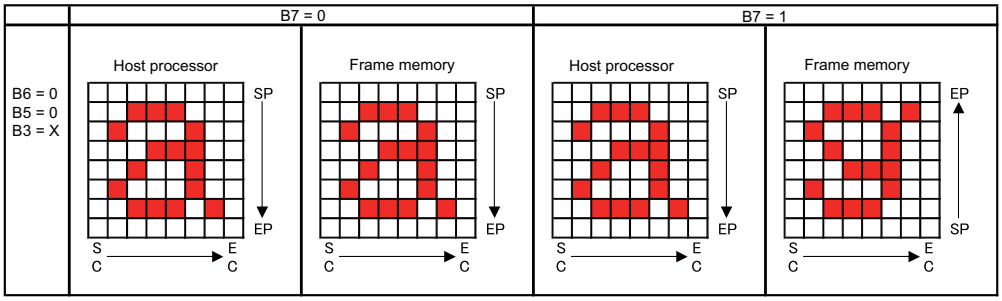
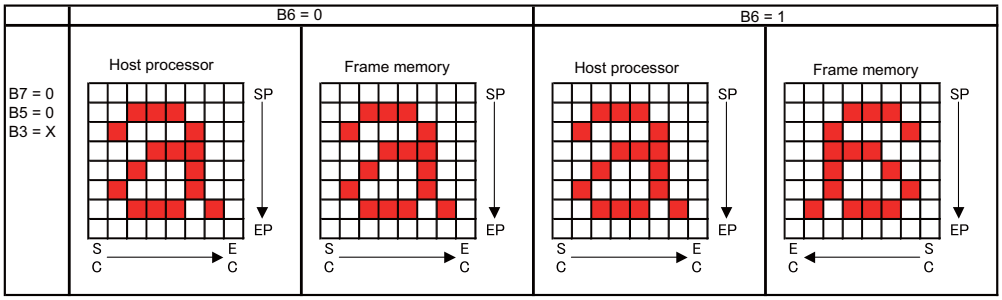
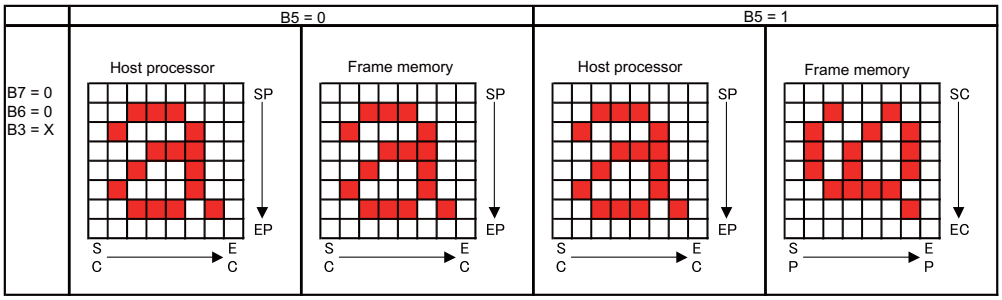
set_tear_on: 35h

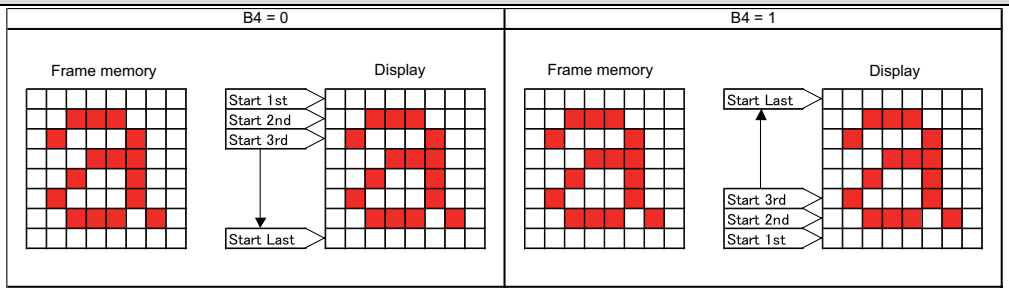
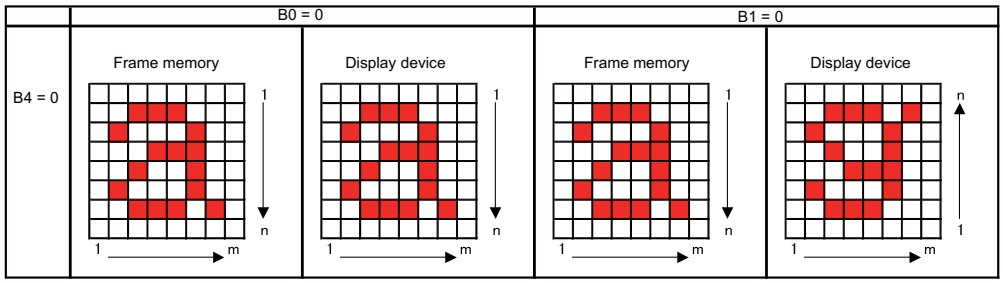
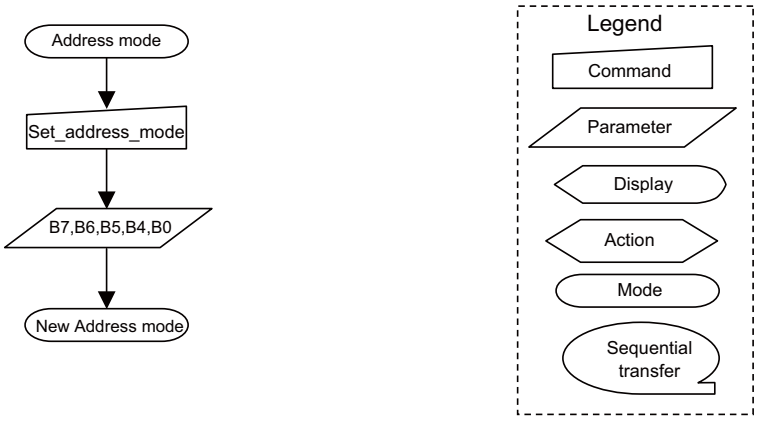
35h	set_tear_on												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	0	1	0	1	35h
Parameter	1	1	↑	x	x	x	x	x	x	x	x	TELOM	XXh
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line. The TE signal is not affected by changing set_address_mode (36h) bit B4 (Line Address order). The Tearing Effect Line On has one parameter, TELON, that describes the Tearing Effect Output Line mode. See TE Pin Output Signal" for detail. TELOM = 0: The Tearing Effect Output line consists of V-Blanking information only. The Tearing Effect Output line shall be high during vertical blanking period.  TELOM = 1: The tearing Effect Output line consists of both V-blanking and H-blanking information.  Vertical blanking period: Non-lit display period in (back porch + front porch + partial mode) Note: The Tearing Effect Output line shall be active low when the display module is in Sleep mode. X = Don't care												
Restriction	This command has no effect when Tearing Effect output is already ON. Changes in parameter TELOM is enabled from the next frame period.												

35h	set_tear_on
Flow Chart	

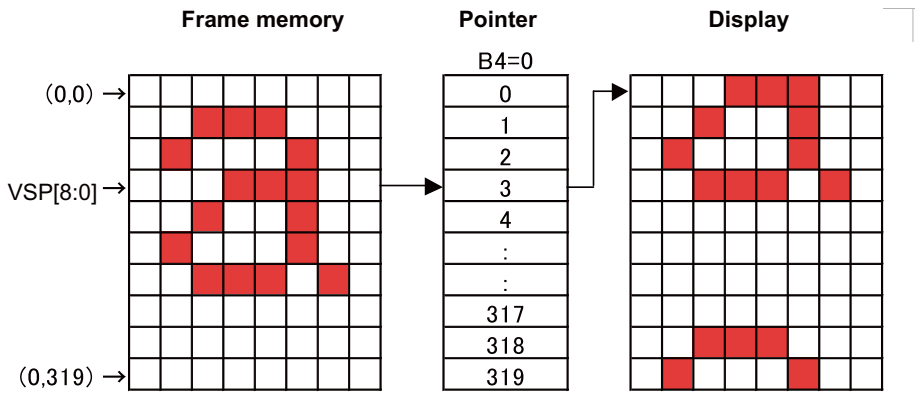
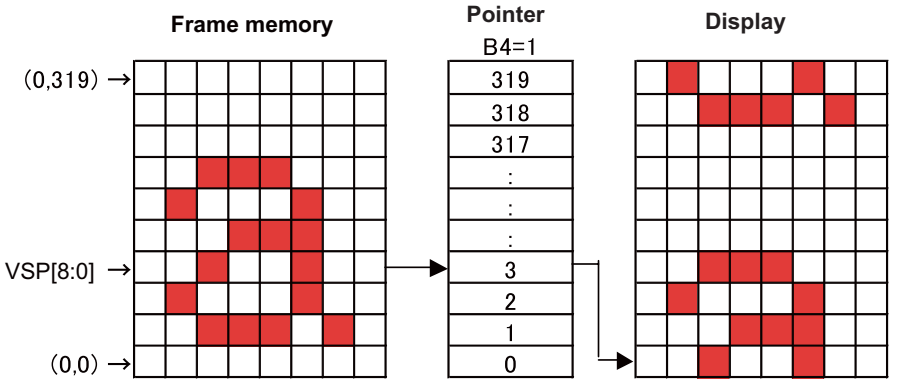
set_address_mode: 36h

<table>
<tr><td>36h</td><td colspan="13">set_address_mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB17-8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36h</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>x</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>0</td><td>0</td><td>0</td><td>B0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">This command sets read/write scanning direction of frame memory. No status bits are changed.
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th><th>Symbol</th></tr>
<tr><td>D7</td><td>Page Address Order</td><td></td><td>B7</td></tr>
<tr><td>D6</td><td>Column Address Order</td><td></td><td>B6</td></tr>
<tr><td>D5</td><td>Page/Column Addreeing Order</td><td></td><td>B5</td></tr>
<tr><td>D4</td><td>Display Device Line Refresh Order</td><td></td><td>B4</td></tr>
<tr><td>D3</td><td>RGB/BGR Order</td><td>Don’t care</td><td>-</td></tr>
<tr><td>D2</td><td>Display Data +atch Data Order</td><td>Don’t care</td><td>-</td></tr>
<tr><td>D1</td><td>Flip Horizontal</td><td>Don’t care</td><td>-</td></tr>
<tr><td>D0</td><td>Flip Vertical</td><td></td><td>B0</td></tr>
</table></td></tr>
</table>

36h	set_address_mode
Description	• Bit B7 - Page Address Order '0' = Top to Bottom '1' = Bottom to Top (When B7='1')  • Bit B6 - Column Address Order '0' = Left to Right '1' = Right to Left  • Bit B5 – Page/Column Addressing Order '0' = Normal mode '1' = Reverse Mode  See "Writing image and writing direction from the host to the frame memory" in chapter Frame Memory. • Bit B4 – Display Device Line Refresh Order '0' = LCD refresh Top to Bottom '1' = LCD refresh Bottom to Top (Memory reading and gate scanning directions invert simultaneously)

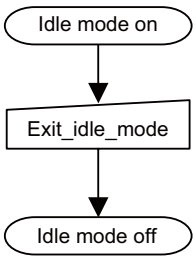
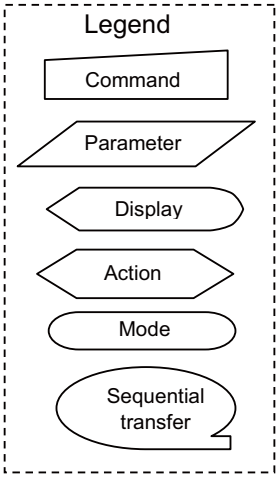
36h	set_address_mode
Description	 • Bit B3 – RGB/BGR order This bit is not applicable. Set to “0”. (not supported). • Bit B2 – Display Data Latch Data Order This bit is not applicable. Set to “0”. (not supported). • Bit B1 – Flip Horizontal This bit is not applicable. Set to “0”. (not supported). • Bit B0 – Flip Vertical ‘0’ = Normal ‘1’ = Flipped  x = Don’t care
Restriction	-
Flow Chart	

set_scroll_start: 37h

37h	set_scroll_start												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	0	1	1	1	37h
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	VSP [8]	000 … 13F
2nd parameter	1	1	↑	x	VSP [7]	VSP [6]	VSP [5]	VSP [4]	VSP [3]	VSP [2]	VSP [1]	VSP [0]	
Description	This command is used together with set_scroll_area (33h). The set_scroll_start command has one parameter, VSP (Vertical Scroll Pointer). VSP defines the line in the frame memory that is written to the display device as the first line of the vertical scroll area as illustrated below: set_address_mode (36h) B4 = 0 Example Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP = 3  set_address_mode (36h) B4 = 1 Example Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP = 3  Note: When a new pointer position and picture data are sent, the result on the display will happen at the next panel scan to avoid tearing effect. X = Don't care												

37h	set_scroll_start
Restriction	Since the value of the Vertical Scrolling Pointer is absolute with reference to the Frame Memory, it must not enter the fixed area (defined by set_scroll_area (33h). Otherwise, an undesirable image will be displayed on the panel although the command will be accepted.
Flow Chart	See set_scroll_area (33h) description.

exit_idle_mode: 38h

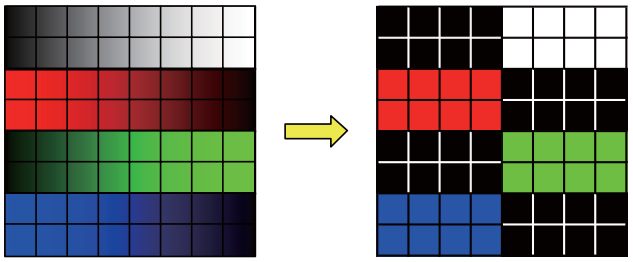
38h	exit_idle_mode												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	1	0	0	0	38h
Parameter	None												
Description	This command causes the display module to exit Idle mode. LCD can display up to maximum 262,144 colors. If the operation of the R61516 is in synchronization with internal oscillation clock (DM=0), the frame rate and liquid crystal alternating cicle can be adjusted for every display mode (Normal, Partial, Normal+Idle, Partial+Idle modes). See description of the manufacturer commands C0h-C2h's 1st to 3rd parameters for detail. If the operation of the R61516 is in synchronization with internal oscillation clock (DM=0), the current in amplifier and step-up clock cycle can be adjusted for different display modes (Normal, Partial, Normal+Idle, Partial+Idle modes). See description of the manufacturer commands D2-D4h's 1st and 2nd parameters for detail. X = Don't care												
Restriction	This command has no effect when the display module is not in Idle mode.												
Flow Chart	 												

enter_idle_mode: 39h

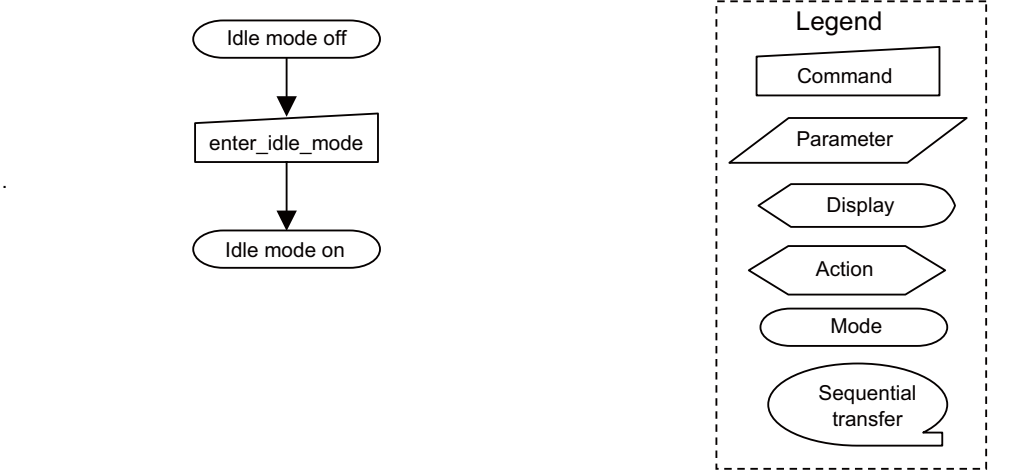
<table>
<tr><td>39h</td><td colspan="13">enter_idle_mode</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB17-8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39h</td></tr>
<tr><td>Parameter</td><td colspan="13">None</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the display module to enter Idle mode. In Idle mode, color expression is reduced. Eight color depth data is displayed using MSB of each R, G and B color components in the Frame Memory.

If the operation of the R61516 is in synchronization with internal oscillation clock (DM=0), the frame rate and liquid crystal alternating cicle can be adjusted for every display mode (Normal, Partial, Normal+Idle, Partial+Idle modes). See description of the manufacturer commands C0h-C2h's 1st - 3rd parameters for detail.

If the operation of the R61516 is in synchronization with internal oscillation clock (DM=0), the current in amplifier and step-up clock cycle can be adjusted for different display modes (Normal, Partial, Normal+Idle, Partial+Idle modes). See description of the manufacturer commands D2-D4h's 1st and 2nd parameters for detail.

Memory Display Panel
 

Memory contents vs Display Colour
<table><tr><td></td><td>R5 R4 R3 R2 R1 R0</td><td>G5 G4 G3 G2 G1 G0</td><td>B5 B4 B3 B2 B1 B0</td></tr><tr><td>Black</td><td>0 X X X X X</td><td>0 X X X X X</td><td>0 X X X X X</td></tr><tr><td>Blue</td><td>0 X X X X X</td><td>0 X X X X X</td><td>1 X X X X X</td></tr><tr><td>Red</td><td>1 X X X X X</td><td>0 X X X X X</td><td>0 X X X X X</td></tr><tr><td>Magenta</td><td>1 X X X X X</td><td>0 X X X X X</td><td>1 X X X X X</td></tr><tr><td>Green</td><td>0 X X X X X</td><td>1 X X X X X</td><td>0 X X X X X</td></tr><tr><td>Cyan</td><td>0 X X X X X</td><td>1 X X X X X</td><td>1 X X X X X</td></tr><tr><td>Yellow</td><td>1 X X X X X</td><td>1 X X X X X</td><td>0 X X X X X</td></tr><tr><td>White</td><td>1 X X X X X</td><td>1 X X X X X</td><td>1 X X X X X</td></tr></table>
X = Don't care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in Idle mode.</td></tr>
</table>

39h	enter_idle_mode
Flow Chart	

set_pixel_format: 3Ah

3Ah	set_pixel_format												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	1	0	1	0	3Ah
1st parameter	1	1	↑	x	0	D6	D5	D4	0	D2	D1	D0	XXh

Description

This command is used to define the format of RGB picture data, which is to be transferred via the DBI/DPI. The formats are shown in the following table:

Bit D[6:4] – DPI Pixel Format (RGB Interface Color Format Selection)

Bit D[2:0] – DBI Pixel Format (Control Interface Colour Format Selection)

Bit D7 and D3 – These bits are not applicable. Set to "0".

Control Interface Colour Format	D6/D2	D5/D1	D4/D0
Setting disabled	0	0	0
3bit/pixel (8 colors)	0	0	1
Setting disabled	0	1	0
Setting disabled	0	1	1
Setting disabled	1	0	0
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,1444 colors)	1	1	0
Setting disabled	1	1	1

See "Data Format List" for each type of interfaces.

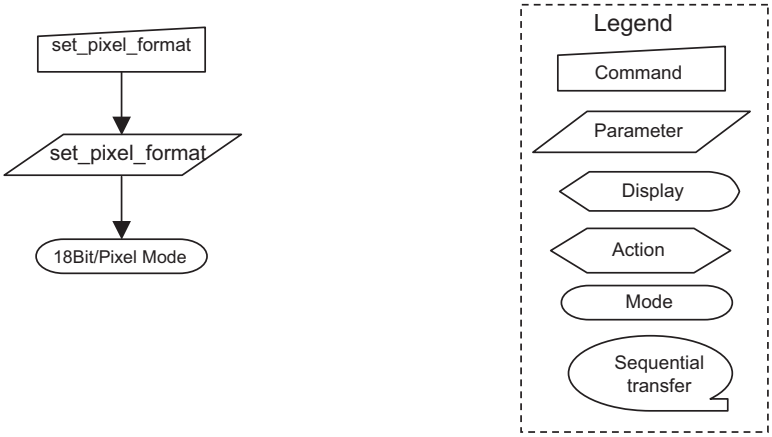
Note 1: When the setting disabled bits are set, undesirable image will be displayed on the panel.

Note 2: Other setting than D[2:0] =1 (3 bpp) and 6 (18 bpp) is disabled in DBI Type C serial interface operation.

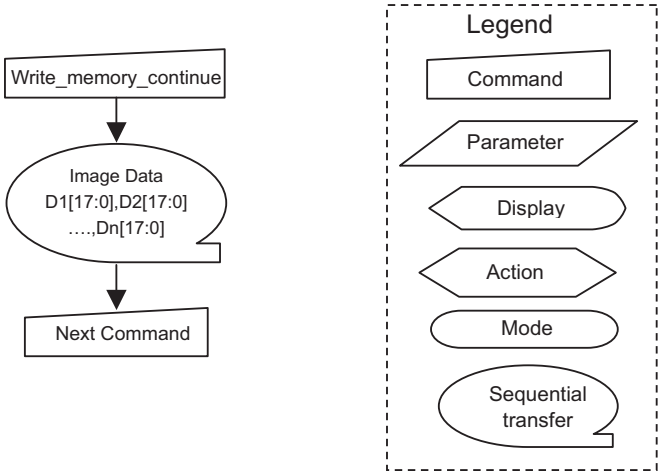
X = Don't care

Restriction: There is no visible effect until the frame memory is written.

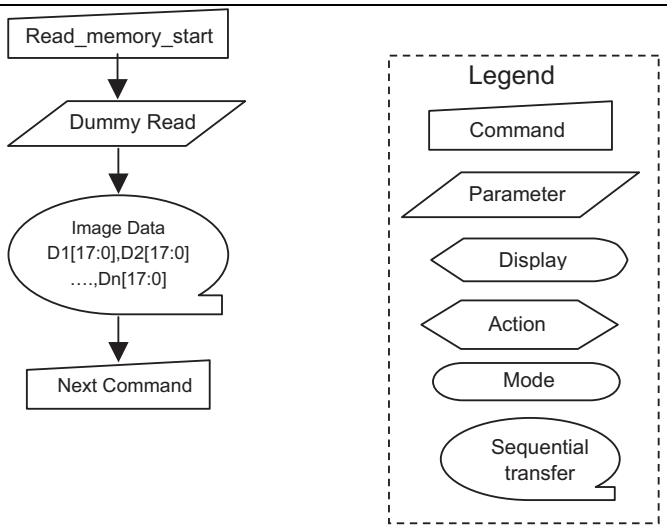
Flow Chart



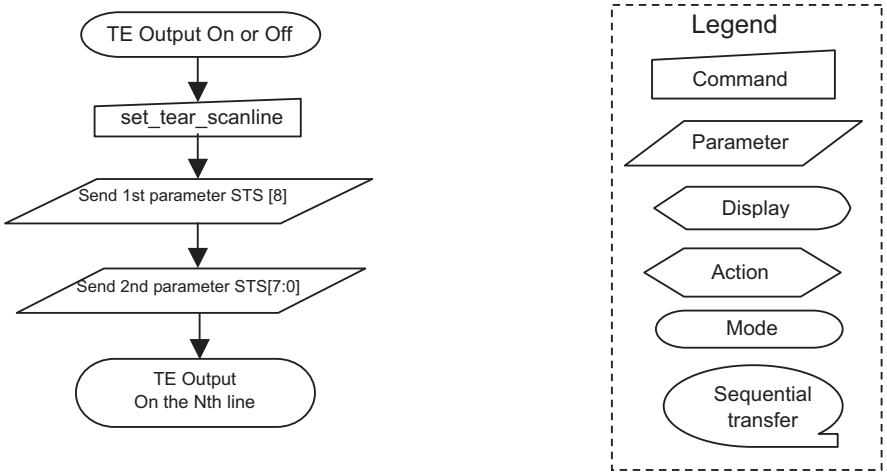
write_memory_continue: 3Ch

3Ch	write_memory_continue												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	1	1	0	0	3Ch
1st parameter	1	1	↑	D1 [17:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000… 3FF
:	1	1	↑	Dx [17:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000… 3FF
Nth parameter	1	1	↑	Dn [17:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000… 3FF
Description	This command transfers image data from the host processor to the display module's frame memory coutinuing from the pixel location following the previous write_memory_continue or write_memory_start command. Frame Memory Access and Interface setting (B3h): WEMODE = 0 If the number of pixels in the transfer data exceeds (EC-SC+1)*(EP-SP+1), the extra pixels are ignored. Frame Memory Access and Interface setting (B3h): WEMODE = 1 When the number of pixels in the transfer data exceeds (EC-SC+1)*(EP-SP+1), the column register and the page register are reset to the Start Column/Start Page positions, and the subsequent data is written to the frame memory. X=Don't care												
Restriction	If write_memory_continue command is executed without setting set_column_address (2Ah), set_page_address (2Bh), and set_address_mode (36h), there is no guarantee that data is correctly written to the frame memory.												
Flow Chart													

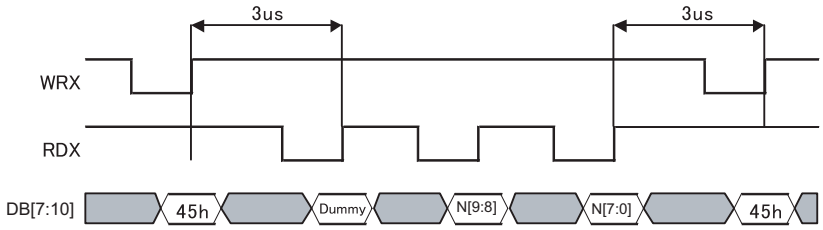
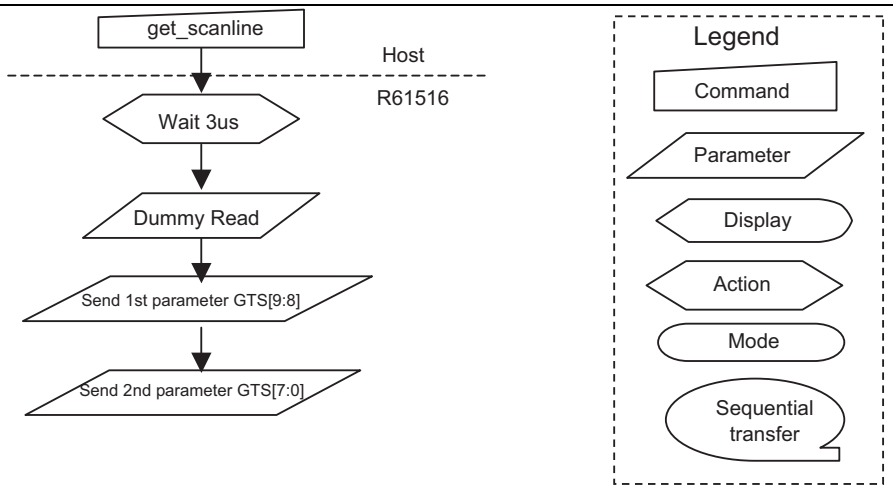
read_memory_continue:3Eh

3Eh	read_memory_continue												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	1	1	1	0	3Eh
1st Pixel data	1	↑	1	D1 [17:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000… 3FF
:	1	↑	1	Dx [17:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000… 3FF
Nth Pixel data	1	↑	1	Dn [17:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000… 3FF
Description	This command transfers image data from the diplay module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command. If read operation is executed after (EP. EC) is read, the last data (EP, EC) continues to output. After pixel data 1 is written frame memory (SC, SP), address counter's direction differs depending on setting of set_address_mode (36h)'s Bits 5, 6, 7. See "Host Processor to Memory Write/Read Direction". X = Don't care												
Restriction	In any color mode, format returned by read_memory_continue is always 18 bit so there is no restriction on the length of parameter.												
Flow Chart													

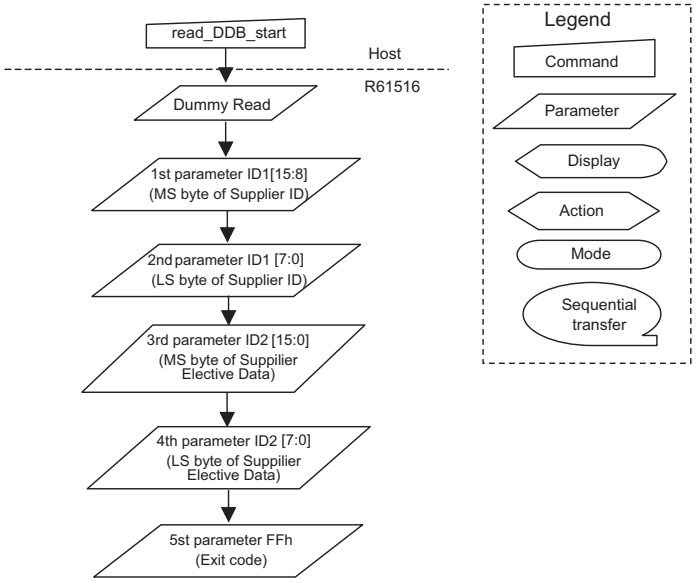
set_tear_scanline:44h

45h	set_tear_scanline												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	0	0	1	0	0	44h
1st Parametre	1	1	↑	X	X	X	X	X	X	X	0	STS [8]	0Xh
2nd Parameter	1	1	↑	X	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	XXh
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N defined by STS [8:0]. TE line is unaffected by change in B4 bit of set_address_mode command. See figure in get_scanline (45h) Restriction. X=don't care.												
Restriction	The command takes affect on the frame following the current frame. Therefore, if the TE signal is already ON, TE signal is output according to the old set_tear_on and set_tear_scanline commands until the end of currently scanned frame. Setting is disabled when TELOM=1 of set_tear_on (35h). Make sure that STS [8:0] ≤ NL (number of line) + 1.												
Flow Chart													

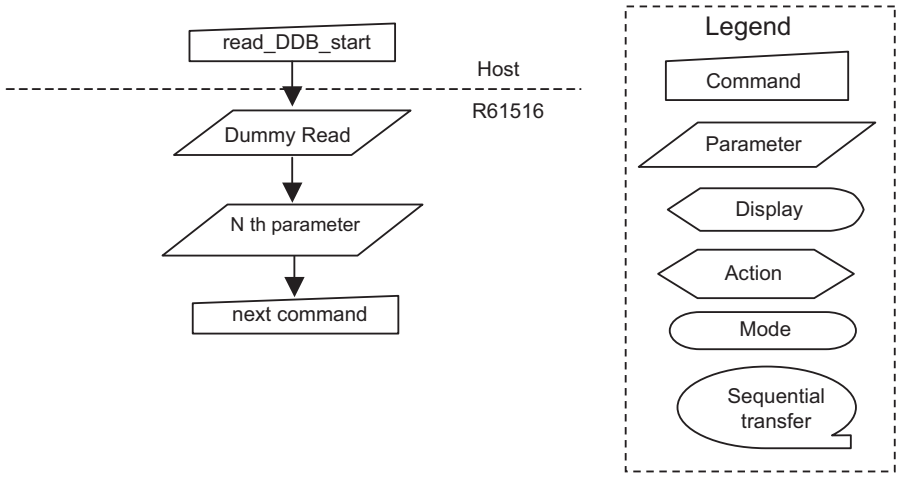
get_scanline: 45h

45h	get_scanline												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	0	0	1	0	1	45h
1st parameter	1	↑	1	X	X	X	X	X	X	X	GTS [9]	GTS [8]	0Xh
2nd parameter	1	↑	1	X	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	XXh
Description	The display module returns the current scan line. The total number of scan lines is defined as (BP + NL + FP). The first scan line of back porch period is defined as line 0. In sleep mode, the value returned by get_scanline is undefined. X = Don't care												
Restriction	After get_line command is input, it takes 3μs or more to read it. After parameters are read, wait 3μs or more to reinput this command. 												
Flow Chart													

read_DDB_start: A1h

45h	read_DDB_start												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	0	0	0	0	1	A1h
1st Parameter	1	↑	1	X	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
2nd Parameter	1	↑	1	X	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
3rd Parameter	1	↑	1	X	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
4th Parameter	1	↑	1	X	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
5th Parameter	1	↑	1	X	1	1	1	1	1	1	1	1	FFh
Description	The command returns information from the display module as follows: 1st parameter: upper byte (ID1[15:8]) of Supplier ID 2nd parameter: lower byte (ID1[7:0]) of Supplier ID 3rd parameter: Supplier Elective Data (ID2[15:8]) 4th parameter: Supplier Elective Data (ID2[7:0]) 5th parameter: Exit Code (FFh) EEPROME=1: Supplier ID and Supplier Elective Data are read when external EEPROM is used. EEPROME=0: Supplier ID amd Supplier Elective Data stored in internal NVM are read when external EEPROM is not used. X=don't care												
Restriction	-												
Flow Chart													

read_DDB_continue: A8h

A1h	read_DDB_continue												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	0	1	0	0	0	A8h
1st Parameter	1	↑	1	X	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
2nd Parameter	1	↑	1	X	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
3rd Parameter	1	↑	1	X	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
4th Parameter	1	↑	1	X	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
5th Parameter	1	↑	1	X	1	1	1	1	1	1	1	1	FFh
Description	This command continues to read from the location that follows suspended read_DDB_continue or read_DDB_start. See read_DDB_start (A1h) for description on data to be read. X=don't care												
Restriction	A read_DDB_start command and parameter read should be executed at least once respectively before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.												
Flow Chart													

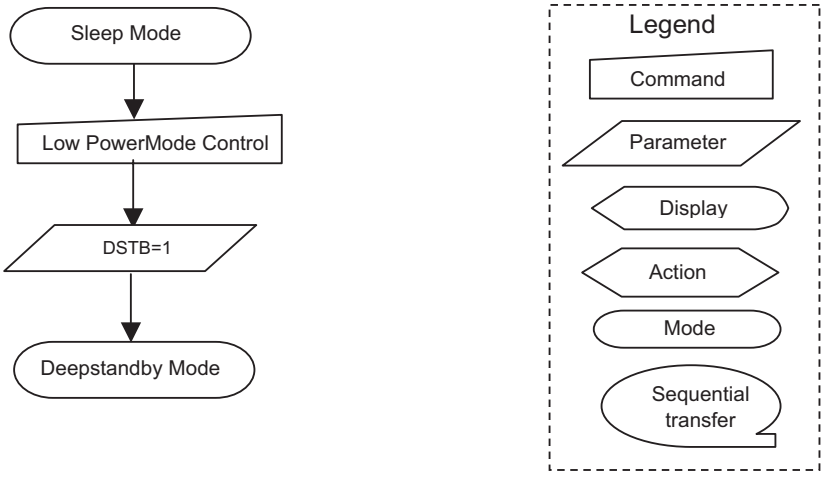
Manufacturer Command

Additional User Command:

MCAP: Manufacturer Command Access Protect (B0h)

<table>
<tr><td>B0h</td><td colspan="13">MCAP (Manufacturer Command Access Protect)</td></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>DB17-8</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td><td>Hex</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>X</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0h</td></tr>
<tr><td>1st parameter</td><td>1</td><td>#A</td><td>#B</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>MCAP [1]</td><td>MCAP [0]</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="13">Write #A=”1” #B=”↑”
Read #A=”↑” #B=” 1” & Insert dummy read
MCAP[1:0]
The R61516 is required to release Access Protect before inputting a Manufacturer Command. This command releases parameters so that Manufacturer Command inputs are enabled. When the conditions to release Protect, as shown in the table below, are met, Manufacturer Command inputs are enabled.
<table>
<tr><th rowspan="2">MCAP [1]</th><th rowspan="2">MCAP [0]</th><th>User Command</th><th colspan="3">Manufacturer Command</th></tr>
<tr><th>00h-0Fh</th><th>B0h</th><th>B1-BFh</th><th>C0h-FFh</th></tr>
<tr><td>0</td><td>0</td><td>Yes</td><td>Yes</td><td>Yes</td><td>Yes</td></tr>
<tr><td>0</td><td>1</td><td colspan="4">Setting Inhibitted</td></tr>
<tr><td>1</td><td>0</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td></tr>
<tr><td>1</td><td>1</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
</table>
Yes:Accessing is enabled (Protect Off)
No : Accessing is disabled (Protect On)
Once the R61516 enables Manufacturer Command inputs, it keeps the state until MCAP[1:0] is written so that the R61516 to enters Protect ON state again.</td></tr>
<tr><td>Restriction</td><td colspan="13">After H/W Reset or exiting Deep Standby Mode, accessing a Manufacturer Command is restricted so that Manufacture Commands B1h~BFh inputs are identified as nop command.</td></tr>
</table>

Low Power Mode Control (B1h)

B1h	Low power Mode Control												
	D/CX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	0	0	0	1	B1h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	DSTB	XX
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read This command is used to enter the Deep Standby Mode. **DSTB** The driver enters the Deep Standby Mode when DSTB=1. Internal logic power supply cirucuit (VDD) is turned down enabling low power consumption. In the Deep Standby mode, data stored in the Frame Memory and the Instructions are not retained. Rewrite them after the Deep Standby mode is exited. See Deep Standby Mode IN/EXIT Sequence in "State and Command Sequence".												
Restriction	-												
Flow Chart													

Frame Memory Access and Interface Setting (B3h)

B3h	Frame Memory Access and Interface Setting												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	1	1	B3h
1st Parameter	1	#A	#B	X	0	0	0	0	0	0	WEMODE	HWM	XX
2nd Parameter	1	#A	#B	X	0	0	0	0	0	TEI [2]	TEI [1]	TEI [0]	XX
3rd Parameter	1	#A	#B	X	0	0	0	0	0	DENC [2]	DENC [1]	DENC [0]	XX
4th Parameter	1	#A	#B	X	0	0	EPF [1]	EPF [0]	0	0	0	DFM	XX
5th Parameter	1	#A	#B	X	0	0	0	0	0	0	RIM [1]	RIM [0]	XX

Description

Write #A="1" #B="↑"

Read #A="↑" #B=" 1" & Insert dummy read

WEMODE

After frame memory write operation reaches to the end of winfow address area, the next write start position is selected.

WEMODE = 0: The write start position is not reset to the start of window address, and the subsequent data is disregarded. (Default)
WEMODE = 1: The write statrt position is reset to the start of window addres area to overwrite the subsequent data to the previous data.

HWM

HWM = 0: Normal write mode (Default)
HWM = 1: High-speed write mode

When HWM = "1", the R61516 writes data in the frame memory in high speed with low power consumption. In this write operation, the R61516 latches the data in the line buffer in units of horizontal lines of window address area and writes the data line by line at a time in the window address area minimizing the number of frame memory access and thereby reducing power consumption. When HWM = "1", make sure the data is written to the end of the line within the window address area in each farme memory write operation by setting set_address_mode: 36h's B5 to 0. If not, the frame memory write operation on that line will fail.

Note 1: The data in the line buffer is cleared when terminating the frame memory write operation in the middle of horizontal line and other instruction writes. When switching from high-speed frame memory write operation to command write operation, wait at least 2 normal-mode write cycle periods (tcycw) after writing data to the frame memory.

Note 2: To read the frame memory, make sure that HWM=0.

Description

TEI [2:0]
The bit is used to define interval between output of TE signal. Set in accordance with update cycle and transfer rate of the display data.

TEI[2]	TEI[1]	TEI[0]	Interval
0	0	0	Every frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other setting			Setting disabled

DENC [2:0]

The bit is used to define Frame Memory write cycle in DPI operation. Set in accordance with update cycle of the display data.

DENC [2]	DENC [1]	DENC [0]	Frame Memory Write Cycle
0	0	0	Every frame
0	0	1	1 frame
0	1	0	2 frames
0	1	1	3 frames
1	0	0	4 frames
1	0	1	5 frames
1	1	0	6 frames
1	1	1	7 frames

EPF[1:0]

This bit is used to set data format when 16bpp (R,G,B) data is converted to 18bpp (r,g,b) and stored in internal frame memory (18bpp).

EPF is enabled when one of

1 DBI TypeB 16 bit interface (set_pixel_format (3Ah) D[2:0]=3'h5)
2 DBI TypeB 8 bit interface (set_pixel_format (3Ah) D[2:0]=3'h5)
3 DPI 16 bit interface (RIM=2'h1, set_pixel_format (3Ah) D[6:4]=3'h5)

is selected. EPF is disabled in other interface operation.

Description

EPF[1:0]	Expand 16bpp(R, G, B) to 18bpp(r, g, b)
2'h0	"0" is written to LSB r[5:0]={ R[4:0], 1'h0 } g[5:0]={ G[5:0] } b[5:0]={ B[4:0], 1'h0 } Note that data is converted as follows: R[4:0], B[4:0]=5'h1F → r, b[5:0]=6'h3F G[5:0]=6'h3F → g[5:0]=6'h3F
2'h1	"1" is written to LSB r[5:0]={ R[4:0], 1'h1 } g[5:0]={ G[5:0] } b[5:0]={ B[4:0], 1'h1 } Note that data is converted as follows: R[4:0], B[4:0]=5'h0 → r, b[5:0]=6'h00 G[5:0]=6'h0 → g[5:0]=6'h00
2'h2	MSB value is written to LSB r[5:0]={ R[4:0], R[4] } g[5:0]={ G[5:0] } b[5:0]={ B[4:0], B[4] }
2'h3	Setting disabled

DFM

The bit is used to define image data write/read format to the Frame Memory in DBI TypeB (16bit bus interface) and DBI TypeC serial interface operation. See DBI Data Format for details.

RIM [1:0]

The bit is used to define bus width in DPI operation. Do not change the RIM setting during display operation.

RIM[1]	RIM[0]	Bus width	Colors	Pins
0	0	Setting disabled	-	-
0	1	16-bit	65,536	DB[15:0]
1	0	18-bit	262,144	DB[17:0]
1	1	Setting disabled	-	-

Display Mode and Frame Memory Write Mode setting (B4h)

B4h	Frame Memory Access and Interface setting												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	1	0	0	B4h
1st Parameter	1	#A	#B	X	0	0	0	RM	0	0	DM[1]	DM[0]	XX
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read												

RM

The bit is used to select a interface for the Frame Memory access operation. The Frame Memory is accessed only via the interface defined by RM bit. Because the interface can be selected separately from display operation mode, writing data to the Frame Memory is possible via system interface when RM = 0, even in the DPI display operation . RM setting is enabled from the next frame. Wait 1 frame to transfer data after setting RM.

RM	Interface to access Frame Memory
0	DBI
1	DPI

See "Display Pixel Interface" for the sequence.

DM[1:0]

The bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, or DIP signal. Note that switching between VSYNC and DPI operation is prohibited.

DM[1]	DM[0]	Display mode
0	0	Internal oscillation clock
0	1	DPI signal
1	0	VSYNC signal
1	1	Setting disabled

Device Code Read:(BFh)

A1h	Device Code Read												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	1	1	1	1	BFh
1st Parameter	1	↑	1	X	0	0	0	0	0	0	0	1	01h
2nd Parameter	1	↑	1	X	0	0	1	0	0	0	1	0	22h
3rd Parameter	1	↑	1	X	0	0	0	1	0	1	0	1	15h
4th Parameter	1	↑	1	X	0	0	0	1	0	1	1	0	16h
Description	The parameters are used to read the information as follows. 1st parameter: Returns the upper byte "01h" of Renesas Technology's Supplier ID decided by MIPI Alliance. 2nd parameter: Returns the lower byte "22h" of Renesas Technology's Supplier ID decided by MIPI Alliance. 3rd parameter: Returns the upper byte "15h" of product code of this LSI. 4th parameter: Returns the lower byte "16h" of product code of this LSI. 5th parameter: Returns Exit Code (FFh). X = Don't care												
Restriction	-												

Panel Control

Panel Driving setting (C0h)

C0h	Panel Driving setting												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	0	0	C0h
1st parameter	1	#A	#B	X	0	0	0	REV	SM	GS	BGR	SS	XX
2nd parameter	1	#A	#B	X	0	NL [6]	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	XX
3rd parameter	1	#A	#B	X	0	SCN [6]	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	XX
4th parameter	1	#A	#B	X	0	0	0	0	0	0	0	NW [0]	XX
5th parameter	1	#A	#B	X	0	0	0	0	0	0	BLV	PTV	XX
6th parameter	1	#A	#B	X	0	0	BLS	NDL	0	PTS [2]	PTS [1]	PTS [0]	XX
7th parameter	1	#A	#B	X	0	0	0	PTG	ISC [3]	ISC [2]	ISC [1]	ISC [0]	XX
8th parameter	1	#A	#B	X	0	PC DIV H [2]	PC DIV H [1]	PC DIVH [0]	0	PC DIV H [2]	PC DIV H [1]	PC DIV H [0]	XX
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read												

Description

REV

The grayscale ie reversed by setting REV = 0. This enables the R61516 to display the same image from the same set of data on both normally white and black panels. The source output level during the retrace period and non-lit display period is determined by register settings, BLS and NDL, respectively.

REV	Frame Memory data	Source output level in display area	
		Positive polarity	Negative polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

SM

SM=0: Left/right interchanging scan
SM=1: Left/right one-side scan

GS

GS=0: Forward scan
GS=1: Reverse scan

The R61516 allows changing gate driver assignment and the scan mode by combination of SM and GS bits. Set these bits in accordance with the configuration of the module. For details, see "Scan Mode Setting".

BGR

The bit is used to reverse 18-bit write data in the Frame Memory from RGB to BGR. Set in accordance with arrangement of color filters.

BGR=0: Data is written to the Frame Memory in the order of RGB. (Default)
BGR=1: Data is written to the Frame Memory in the order of BGR.

SS

The bit is used to select the shifting direction of the source driver output. Set in accordance with mounting position of the R61516 to the panel.

SS=0: S1 to S720 (Default)
SS=1 S720 to S1

To change the RGB order, set SS and BGR bit.

SS=0, BGR=0: RGB
SS=1, BGR=1: BGR

Description

NL[6:0]

These bits set the number of lines to drive the LCD at 4 line intervals. The frame memory address mapping is not affected by the number of NL[6:0]. The number of lines should be set according to the panel size.

NL[6:0]	No. of Line
7'h00	Setting disabled
7'h01	Setting disabled
7'h02	Setting disabled
7'h03	Setting disabled
7'h04	Setting disabled
7'h05	Setting disabled
7'h06	Setting disabled
7'h07	Setting disabled
7'h08	Setting disabled
7'h09	Setting disabled
7'h0A	Setting disabled
7'h0B	Setting disabled
7'h0C	Setting disabled
7'h0D	Setting disabled
7'h0E	Setting disabled
7'h0F	Setting disabled
7'h10	Setting disabled
7'h11	Setting disabled
7'h12	Setting disabled
7'h13	Setting disabled
7'h14	Setting disabled
7'h15	Setting disabled
7'h16	Setting disabled
7'h17	Setting disabled
7'h18	Setting disabled
7'h19	Setting disabled
7'h1A	Setting disabled
7'h1B	Setting disabled
7'h1C	Setting disabled
7'h1D	Setting disabled
7'h1E	Setting disabled
7'h1F	Setting disabled

NL[6:0]	No. of Line
7'h20	Setting disabled
7'h21	Setting disabled
7'h22	Setting disabled
7'h23	Setting disabled
7'h24	Setting disabled
7'h25	Setting disabled
7'h26	Setting disabled
7'h27	Setting disabled
7'h28	Setting disabled
7'h29	Setting disabled
7'h2A	Setting disabled
7'h2B	Setting disabled
7'h2C	Setting disabled
7'h2D	Setting disabled
7'h2E	Setting disabled
7'h2F	Setting disabled
7'h30	Setting disabled
7'h31	Setting disabled
7'h32	Setting disabled
7'h33	Setting disabled
7'h34	Setting disabled
7'h35	Setting disabled
7'h36	Setting disabled
7'h37	Setting disabled
7'h38	Setting disabled
7'h39	Setting disabled
7'h3A	Setting disabled
7'h3B	240 lines
7'h3C	244 lines
7'h3D	248 lines
7'h3E	252 lines
7'h3F	256 lines

NL[6:0]	No. of Line
7'h40	260 lines
7'h41	264 lines
7'h42	268 lines
7'h43	272 lines
7'h44	276 lines
7'h45	280 lines
7'h46	284 lines
7'h47	288 lines
7'h48	292 lines
7'h49	296 lines
7'h4A	300 lines
7'h4B	304 lines
7'h4C	308 lines
7'h4D	312 lines
7'h4E	316 lines
7'h4F	320 lines
7'h50-7'h7F	Setting disabled

Description

SCN[6:0]

The bit is used to set scanning start position.

SCN[6:0]	Scan start position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
7'h00	G1	G(N)	G1	G(N)
7'h01	G5	G(N+4)	G9	G(N+8)
7'h02	G9	G(N+8)	G17	G(N+16)
7'h03	G13	G(N+12)	G25	G(N+24)
7'h04	G17	G(N+16)	G33	G(N+32)
7'h05	G21	G(N+20)	G41	G(N+40)
7'h06	G25	G(N+24)	G49	G(N+48)
7'h07	G29	G(N+28)	G57	G(N+56)
7'h08	G33	G(N+32)	G65	G(N+64)
7'h09	G37	G(N+36)	G73	G(N+72)
7'h0A	G41	G(N+40)	G81	G(N+80)
7'h0B	G45	G(N+44)	Setting disabled	Setting disabled
7'h0C	G49	G(N+48)	Setting disabled	Setting disabled
7'h0D	G53	G(N+52)	Setting disabled	Setting disabled
7'h0E	G57	G(N+56)	Setting disabled	Setting disabled
7'h0F	G61	G(N+60)	Setting disabled	Setting disabled
7'h10	G65	G(N+64)	Setting disabled	Setting disabled
7'h11	G69	G(N+68)	Setting disabled	Setting disabled
7'h12	G73	G(N+72)	Setting disabled	Setting disabled
7'h13	G77	G(N+76)	Setting disabled	Setting disabled
7'h14	G81	G(N+80)	Setting disabled	Setting disabled
7'h15-7'h27	Setting disabled	Setting disabled	Setting disabled	Setting disabled
7'h28	G161	G(N+160)	G2	G(N+1)
7'h29	G165	G(N+164)	G10	G(N+9)
7'h2A	G169	G(N+168)	G18	G(N+17)
7'h2B	G173	G(N+172)	G26	G(N+25)
7'h2C	G177	G(N+176)	G34	G(N+33)
7'h2D	G181	G(N+180)	G42	G(N+41)
7'h2E	G185	G(N+184)	G50	G(N+49)
7'h2F	G189	G(N+188)	G58	G(N+57)
7'h30	G193	G(N+192)	G66	G(N+65)
7'h31	G197	G(N+196)	G74	G(N+73)
7'h20-7'hFF	Setting disabled	Setting disabled	Setting disabled	Setting disabled

N: Number of line(s) defined by NL[6:0].

Make sure that gate scanning end position (= gate scanning start position + Number of drive line defined by NL bit) does not exceed 320.

NW[0]

This bit sets the number of lines for inversion liquid crystal drive by line inversion waveform (BCn=1, Display Timing Setting 1-3 (C1h-C3h)). The polarity of waveform inverts in every 1 or 2 line(s).

NW[0]	Number of line(s)
0	1 line
1	2 lines

BLV

The bit selects line or frame inversion during the retrace period.

BLV=0: line inversion is selected for the retrace period when line inversion is selected by BCn=1, C1h~C3h.

BLV=1: Frame inversion is selected for the retrace period.

BCn	BLV	Retrace period
0	-	Frame inversion
1	0	Line inversion
	1	Frame inversion

PTV

The bit is used to define inversion in the non-lit display area.

PTV=1: frame inversion is selected for the non-lit display area when line inversion is selected (BCn=1).

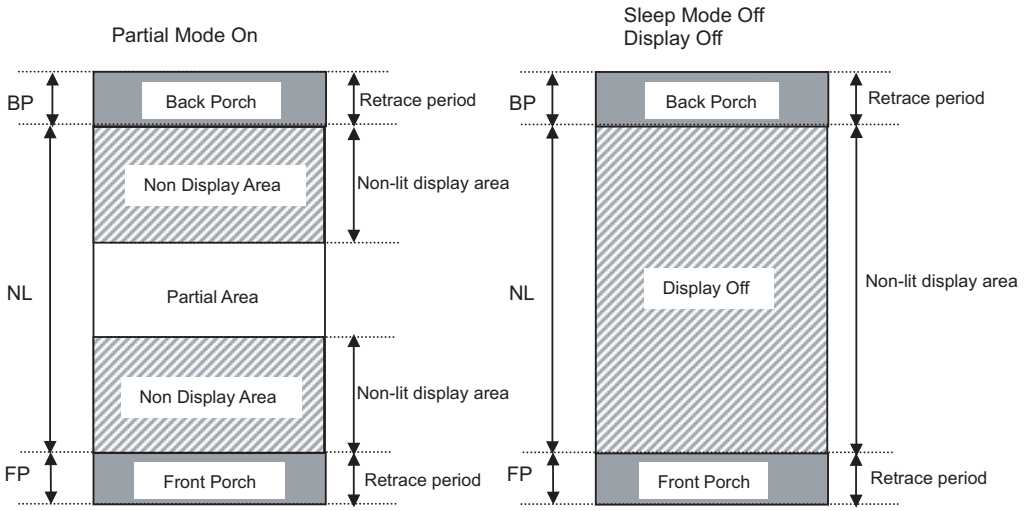
BCn	**PTV**	**Inversion in non-lit display area**
0	*	Frame inversion
1	0	Line inversion
	1	Frame inversion

“Retrace period” means back and front porches.

“Non-lit display area” means:

Non-display area other than the Partial Area defined by SR[8:0] and ER[8:0].
Display area when Sleep mode is off and the display operation is off.

Description



BLS

The bit is used to source output level in the Retrace Period. The polarity of grayscale voltage in the Retrace period is inverted.

	Retrace Period	
BLS	**Posotive polarity**	**Negative polarity**
0	V63	V0
1	V0	V63

NDL

The bit is used to define source output level in the non-lit display area. The polarity of graycscale voltage is inverted.

	Non-lit display area	
NDL	**Positive polarity**	**Negative polarity**
0	V63	V0
1	V0	V63

PTS[2:0]

The bit is used to define low-power consumption operation. PTS[1:0] defines output level in the retrace period and the non-lit display area. PTS[2] defines the operation of the grayscale amplifier and the step-up clock frequency.

Description

PTS[2]	PTS[1:0]	Source output lebel in non-lit display area (Note)		Grayscale amplifier in non-lit display area	Step-up clock frequency in non-lit display area
		Positive polarity	Negative polarity		
0	00	V63	V0	V0 to V63	DC0n, DC1n setting
	01	(setting disabled)	(setting disabled)	(setting disabled)	(setting disabled)
	10	GND	GND	V0 to V63	DC0n, DC1n setting
	11	Hi-z	Hi-z	V0 to V63	DC0n, DC1n setting
1	00	V63	V0	V0,V63	DC0n setting x 1/2
	01	(setting disabled)	(setting disabled)	(setting disabled)	(setting disabled)
	10	GND	GND	V0,V63	DC0n setting x 1/2
	11	Hi-z	Hi-z	V0,V63	DC0n setting x 1/2

Note: The polarity of the source output level in non-lit display period is set by NDL (C0h). The polarity of the source output level during the retrace period is defined by BLS (C0h). If PTS[2]=1, step-up operation may not be executed properly depending on CD0h and RTNn values.

PTG

The bit is used to select gate scan mode in non-lit display area.

PTG	Gate output in non-lit display area
0	Normal scan
1	Interval scan

Note: Set BCn=0 and select frame inversion in interval scan operation.

Descriotion

ISC[3:0]

The bit is used to set gate interval scan when PTG bit sets interval scan in non-lit display area. The scan interval is always of odd number. The polarity of liquid crystal drive waveform is inverted in the same timing as the interval scan.

ISC[3:0]	Scan interval	ISC[3:0]	Scan interval
4'h0	Setting disabled	4'h8	17 frames
4'h1	3 frames	4'h9	19 frames
4'h2	5 frames	4'hA	21 frames
4'h3	7 frames	4'hB	23 frames
4'h4	9 frames	4'hC	25 frames
4'h5	11 frames	4'hD	27 frames
4'h6	13 frames	4'hE	29 frames
4'h7	15 frames	4'hF	31 frames

PCDIVH[2:0]/PCDIVL[2:0]

When the R61516's display operation is synchronized with PCLK (DM=1, DPI), internal clock for display operation switches from internal oscillation clock to PCLKD. The bits are used to define the division ratio of PCLKD to PCLK.

PCDIVH defines the number of PCLK in PCLKD=High period in units of 1 clock.
PCDIVL defines the number of PCLK in PCLKD=Low period in units of 1 clock.

Set PCDIVL=PCDIVH or PCDIVH-1.

Also, set PCDIVH and PCDIVL so that PCLKD frequency becomes the closest to internal oscillation clock frequency 678KHz.

See "Display Pixel Interface" for details in setting the bits.

Display Timing Setting for Normal Mode (C1h), Display Timing Setting for Partial Mode (C2h), Display Timing Setting for Idle Mode (C3h)

C1h	Display Timing Setting for Normal Mode												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	0	1	C1h
1st Parameter	1	#A	#B	X	0	0	0	0	0	0	0	BC0	XX
2nd Parameter	1	#A	#B	X	0	0	0	0	0	0	DIV0 [1]	DIV 0[0]	XX
3rd Parameter	1	#A	#B	X	0	0	0	RTN 0[4]	RTN 0 [3]	RTN 0[2]	RTN 0[1]	RTN 0[0]	XX
4th Parameter	1	#A	#B	X	BP0 [7]	BP0 [6]	BP0 [5]	BP0 [4]	BP0 [3]	BP0 [2]	BP0 [1]	BP0 [0]	XX
5th Parameter	1	#A	#B	X	FP0 [7]	FP0 [6]	FP0 [5]	FP0 [4]	FP0 [3]	FP0 [2]	FP0 [1]	FP0 [0]	XX
C2h	**Display Timing Setting for Partial Mode**												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	1	0	C2h
1st Parameter	1	#A	#B	X	0	0	0	0	0	0	0	BC1	XX
2nd Parameter	1	#A	#B	X	0	0	0	0	0	0	DIV1 [1]	DIV1 [0]	XX
3rd Parameter	1	#A	#B	X	0	0	0	RTN 1[4]	RTN 1[3]	RTN 1[2]	RTN 1[1]	RTN 1[0]	XX
4th Parameter	1	#A	#B	X	BP1 [7]	BP1 [6]	BP1 [5]	BP1 [4]	BP1 [3]	BP1 [2]	BP1 [1]	BP1 [0]	XX
5th Parameter	1	#A	#B	X	FP1 [7]	FP1 [6]	FP1 [5]	FP1 [4]	FP1 [3]	FP1 [2]	FP1 [1]	FP1 [0]	XX
C3h	**Display Timing Setting for Idle Mode**												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	1	1	C3h
1st Parameter	1	#A	#B	X	0	0	0	0	0	0	0	BC2	XX
2nd Parameter	1	#A	#B	X	0	0	0	0	0	0	DIV2 [1]	DIV2 [0]	XX
3rd Parameter	1	#A	#B	X	0	0	0]	RTN 2[4]	RTN 2[3]	RTN 2[2]	RTN 2[1]	RTN 2[0]	XX
4th Parameter	1	#A	#B	X	BP2 [7]	BP2 [6]	BP2 [5]	BP2 [4]	BP2 [3]	BP2 [2]	BP2 [1]	BP2 [0]	XX
5th Parameter	1	#A	#B	X	FP2 [7]	FP2 [6]	FP2 [5]	FP2 [4]	FP2 [3]	FP2 [2]	FP2 [1]	FP2 [0]	XX

Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read Timigs can be defined separately for different modes. C1h: Enabled when Normal Mode On, Idle Mode Off C2h: Enabled when Partial Mode On, Idle Mode Off C3h: Enabled when Normal Mode On, Idle Mode On and Partial Mode On, Idle Mode On **BC0, BC1, BC2** These bits define liquid crystal drive waveform inversion. BC = 0: Frame inversion waveform is selected. BC = 1: Line inversion wave form is selected. For details, see "Line Inversion AC Drive". **DIV0[1:0], DIV1[1:0], DIV2[1:0]** These bits set the division ratio of the internal clock frequency (DIVn). The frame frequency can be changed by DIV bit and RTNn (defining the number of clocks in 1H period). The R61516's internal operation is synchronized with the clock devided by the division ratio set by DIV bits. Also, reference clock width in the source delay time, VCOM invetsion point gate non-overlap period settings and so on changes in accordance with DIVn setting. For details, see "Frame Frequency Adjustment Function".

DIVn[1:0]	Division ratio of internal operation clock
2'h0	1/1
2'h1	1/2
2'h2	1/4
2'h3	1/8

Frame frequency calculation

Frame frequency (f_{FRM}) = {fosc / (Clock per line × division ratio × (Line + FP + BP))} [Hz]

Fosc: Internal clock frequency (678 kHz)
Clocks per line: RTNn bit
Division ratio: DIVn bit
Line: Number of drive line(s) on the panel (NL)
Front porch (FP): FPn bit
Back porch (BP): BPn bit

Description

RTN0[4:0], RTN1[4:0], RTN2[4:0]

These bits set 1H line period.

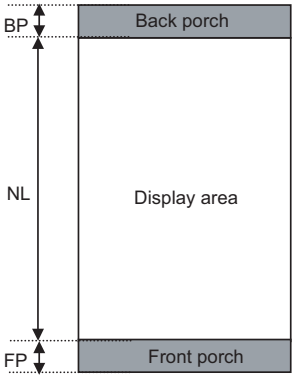
RTNn [4:0]	Clocks per line	RTNn [4:0]	Clocks per line	RTNn [4:0]	Clocks per line
5'h00-5'h0F	Setting inhibited	5'h15	21 clocks	5'h1B	27 clocks
5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks
5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks
5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks
5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks
5'h14	20 clocks	5'h1A	26 clocks		

Description

FP0[7:0], FP1[7:0], FP2[7:0]
BP0[7:0], BP1[7:0], BP2[7:0]

These parameters define the retrace period (i.e. front and back porches) which appears before and after the display area. DPn bits define number of front porch lines while BPn bits define number of back porch lines.

FPn[7:0], BPn[7:0]	Number of front porch lines	Number of back porch lines
8'h00	Setting disabled	Setting disabled
8'h01	Setting disabled	Setting disabled
8'h02	Setting disabled	2 lines
8'h03	3 lines	3 lines
8'h04	4 lines	4 lines
8'h05	5 lines	5 lines
8'h06	6 lines	6 lines
8'h07	7 lines	7 lines
8'h08	8 lines	8 lines
8'h09	9 lines	9 lines
8'h0A	10 lines	10 lines
8'h0B	11 lines	11 lines
8'h0C	12 lines	12 lines
8'h0D	13 lines	13 lines
8'h0E	14 lines	14 lines
8'h0F	15 lines	15 lines
:	:	:
8'h7F	127 lines	127 lines
8'h80	128 lines	128 lines
8'h81	Setting disabled	Setting disabled
:	:	:
8'hFF	Setting disabled	Setting disabled



Restriction	Set the BP and FP bits as follows.		
	BP ≥ 2 lines	FP ≥ 3 lines	FP + BP ≤ 256 lines

Display_Setting commands (C0h, C1h, and Ch2) can be set according to display mode.

Table 20 Display Mode and Valid Register Setting

Display mode	Operation clock (DIV)	Clocks per line (RTN)	Back Porch (BP)	Front Porch (FP)	VCOM inversion cycle (BC)
Normal mode + Idle mode off	C1h: DIV0	C1h: RTN0	C1h: BP0	C1h: FP0	C1h: BC0
Partial mode + Idle mode off	C2h: DIV1	C2h: RTN1	C2h: BP1	C2h: FP1	C2h: BC1
Idle mode on + (Normal/Partial mode)	C3h: DIV2	C3h: RTN2	C3h: BP2	C3h: FP2	C3h: BC2

Source/VCOM/Gate Driving Timing Setting (C4h)

C4h	Source/VCOM/Gate Driving Timing Setting												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	1	0	0	C4h
1st Parameter	1	#A	#B	X	0	SDT [2]	SDT [1]	SDT [0]	0	NOW [2]	NOW [1]	NOW [0]	XX
2nd Parameter	1	#A	#B	X	0	0	0	0	0	MCP [2]	MCP [1]	MCP [0]	XX
3rd Parameter	1	#A	#B	X	0	VEQW [2]	VEQW [1]	VEQW [0]	0	0	VEM [1]	VEM [2]	XX
4th Parameter	1	#A	#B	X	0	0	0	0	0	SPCW [2]	SPCW [1]	SPCW [0]	XX

Description

Write #A="1" #B="↑"

Read #A="↑" #B="1" & Insert dummy read

SDT [2:0]

The bit is used to set the source output alternating position in 1H period.

SDT[2:0]	Source output alternating position	SDT[2:0]	Source output alternating position
3'h0	Setting disabled	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h, C2h, and C3h).

NOW[2:0]

These bits set the gate output start position (non-overlap period).

NOW[2:0]	Gate output start position	NOW[2:0]	Gate output start position
3'h0	Setting disabled	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The unit clock here is specified according to the division ratio set by DIVn (C1h, C2h, and C3h).

Description

MCP [2:0]

The bit is used to set the VCOM output alternating position in 1H period.

MCP[2:0]	VCOM alternating position	MCP[2:0]	VCOM alternating position
3'h0	Setting disabled	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h, C2h, and C3h).

VEQW[2:0]

These bits define VCOM equalize period.

VEQW[2:0]	VCOM equalize period
3'h0	0 clocks
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn.

VEM[1:0]

VEM[0]: VCOMH equalize switch
VEM[0] = 1: When VCOMH level falls from VCOMH to VCOML level, the level first falls to the GND level and then to the VCOML level.

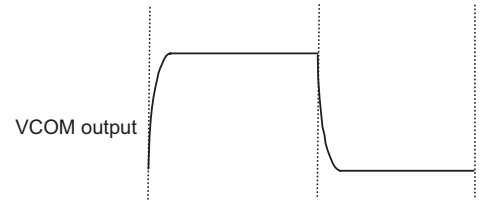
VEM[1]: VCOML equalize switch
VEM[1] = 1: When VCOMH level rises from VCOML level to VCOMH level, the level first goes up to the GND level and then to the VCOMH level.

These bits reduce power consumption during VCOM drive period. In using this function, make sure VCI < VCOMH, GND > VCOML.

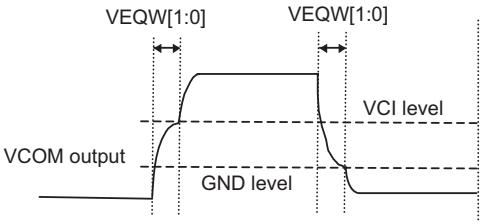
VEM[1:0]	Operation
2'h0	Normal VCOM drive (No equalize)
2'h1	VCOMH equalize
2'h2	VCOML equalize
2'h3	VCOMH/VCOML equalize

When enabling VCOM function to reduce power consumption, check the display quality on the panel and effectiveness of power saving.

Description



1. VEQW[1:0] = 0h



2. VEQW[1:0] is not 0h, VEM[1:0] = 3h

SPCW[2:0]

The bit is used to set source pre-charge period in 1H period. Pre-charge period is set by SPCW[2:0] starting from the source output alternating position defined by SDT [2:0]. Source output is precharged only on the line where liquid crystal waveform inverts.

This function realizes power consumption reduction depending on image data. Check actual image quality and effect on the panel.

SPCW[2:0]	Source precharge position
3'h0	Setting disabled
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h, C2h, and C3h).

Gamma Control

Gamma Set A

C8h	Gamma set A												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	1	0	0	0	C8h
1st parameter	1	1	↑	X	0	0	0	PR0P 00[4]	PR0P 00[3]	PR0P 00[2]	PR0P 00[1]]	PR0P 00[0]	XX
2nd parameter	1	1	↑	X	0	0	0	PR0P 01[4]	PR0P 01[3]	PR0P 01[2]	PR0P 01[1]]	PR0P 01[0]	XX
3rd parameter	1	1	↑	X	0	0	0	PR0P 02[4]	PR0P 02[3]	PR0P 02[2]	PR0P 02[1]	PR0P 02[0]	XX
4th parameter	1	1	↑	X	PR0P 04[3]	PR0P 04[2]	PR0P 04[1]	PR0P 04[0]	PR0P 03[3]	PR0P 03[2]	PR0P 03[1]	PR0P 03[0]	XX
5th parameter	1	1	↑	X	0	0	0	0	PR0P 05[3]	PR0P 05[2]	PR0P 05[1]	PR0P 05[0]	XX
6th parameter	1	1	↑	X	0	0	0	PR0P 06[4]	PR0P 06[3]	PR0P 06[2]	PR0P 06[1]	PR0P 06[0]	XX
7th parameter	1	1	↑	X	0	0	0	PR0P 07[4]	PR0P 07[3]	PR0P 07[2]	PR0P 07[1]	PR0P 07[0]	XX
8th parameter	1	1	↑	X	0	0	0	PR0P 08[4]	PR0P 08[3]	PR0P 08[2]	PR0P 08[1]	PR0P 08[0]	XX
9th parameter	1	1	↑	X	0	0	PIR0P 1[1]	PIR0P 1[0]	0	0	PIR0P 0[1]	PIR0P 0[0]	XX
10th parameter	1	1	↑	X	0	0	PIR0P 3[1]	PIR0P 3[0]	0	0	PIR0P 2[1]	PIR0P 2[0]	XX
11th parameter	1	1	↑	X	0	0	0	PR0N 00[4]	PR0N 00[3]	PR0N 00[2]	PR0N 00[1]	PR0N 00[0]	XX
12th parameter	1	1	↑	X	0	0	0	PR0N 01[4]	PR0N 01[3]	PR0N 01[2]	PR0N 01[1]	PR0N 01[0]	XX
13th parameter	1	1	↑	X	0	0	0	PR0N 02[4]	PR0N 02[3]	PR0N 02[2]	PR0N 02[1]	PR0N 02[0]	XX
14th parameter	1	1	↑	X	PR0N 04[3]	PR0N 04[2]	PR0N 04[1]	PR0N 04[0]	PR0N 03[3]	PR0N 03[2]	PR0N 03[1]	PR0N 03[0]	XX
15th parameter	1	1	↑	X	0	0	0	0	PR0N 05[3]	PR0N 05[2]	PR0N 05[1]	PR0N 05[0]	XX
16th parameter	1	1	↑	X	0	0	0	PR0N 06[4]	PR0N 06[3]	PR0N 06[2]	PR0N 06[1]	PR0N 06[0]	XX
17th parameter	1	1	↑	X	0	0	0	PR0N 07[4]	PR0N 07[3]	PR0N 07[2]	PR0N 07[1]	PR0N 07[0]	XX
18th parameter	1	1	↑	X	0	0	0	PR0N 08[4]	PR0N 08[3]	PR0N 08[2]	PR0N 08[1]	PR0N 08[0]	XX

19th parameter	1	1	↑	X	0	0	PIR0 N1[1]	PIR0 N1[0]	0	0	PIR0 N0[1]	PIR0 N0[0]	XX
20th parameter	1	1	↑	X	0	0	PIR0 N3[1]	PIR0 N3[0]	0	0	PIR0 N2[1]	PIR0 N2[0]	XX
Description	Gamma Set A registers are applied to source pins numbered Sn + 1 (n=1, 2, ..., 239). Gamma Set A registers are applied to all source pins in the Idle Mode. See “Gamma Correction Function” for detailed description of the parameters.												

Gamma Set B (C9h)

C9h	Gamma set B												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	1	0	0	1	C9h
1st parameter	1	1	↑	X	0	0	0	PR1P 00[4]	PR1P 00[3]	PR1P 00[2]	PR1P 00[1]]	PR1P 00[0]	XX
2nd parameter	1	1	↑	X	0	0	0	PR1P 01[4]	PR1P 01[3]	PR1P 01[2]	PR1P 01[1]]	PR1P 01[0]	XX
3rd parameter	1	1	↑	X	0	0	0	PR1P 02[4]	PR1P 02[3]	PR1P 02[2]	PR1P 02[1]	PR1P 02[0]	XX
4th parameter	1	1	↑	X	PR1P 04[3]	PR1P 04[2]	PR1P 04[1]	PR1P 04[0]	PR1P 03[3]	PR1P 03[2]	PR1P 03[1]	PR1P 03[0]	XX
5th parameter	1	1	↑	X	0	0	0	0	PR1P 05[3]	PR1P 05[2]	PR1P 05[1]	PR1P 05[0]	XX
6th parameter	1	1	↑	X	0	0	0	PR1P 06[4]	PR1P 06[3]	PR1P 06[2]	PR1P 06[1]	PR1P 06[0]	XX
7th parameter	1	1	↑	X	0	0	0	PR1P 07[4]	PR1P 07[3]	PR1P 07[2]	PR1P 07[1]	PR1P 07[0]	XX
8th parameter	1	1	↑	X	0	0	0	PR1P 08[4]	PR1P 08[3]	PR1P 08[2]	PR1P 08[1]	PR1P 08[0]	XX
9th parameter	1	1	↑	X	0	0	PIR1P 1[1]	PIR1P 1[0]	0	0	PIR1P 0[1]	PIR1P 0[0]	XX
10th parameter	1	1	↑	X	0	0	PIR1P 3[1]	PIR1P 3[0]	0	0	PIR1P 2[1]	PIR1P 2[0]	XX
11th parameter	1	1	↑	X	0	0	0	PR1N 00[4]	PR1N 00[3]	PR1N 00[2]	PR1N 00[1]	PR1N 00[0]	XX
12th parameter	1	1	↑	X	0	0	0	PR1N 01[4]	PR1N 01[3]	PR1N 01[2]	PR1N 01[1]	PR1N 01[0]	XX
13th parameter	1	1	↑	X	0	0	0	PR1N 02[4]	PR1N 02[3]	PR1N 02[2]	PR1N 02[1]	PR1N 02[0]	XX
14th parameter	1	1	↑	X	PR1N 04[3]	PR1N 04[2]	PR1N 04[1]	PR1N 04[0]	PR1N 03[3]	PR1N 03[2]	PR1N 03[1]	PR1N 03[0]	XX
15th parameter	1	1	↑	X	0	0	0	0	PR1N 05[3]	PR1N 05[2]	PR1N 05[1]	PR1N 05[0]	XX
16th parameter	1	1	↑	X	0	0	0	PR1N 06[4]	PR1N 06[3]	PR1N 06[2]	PR1N 06[1]	PR1N 06[0]	XX
17th parameter	1	1	↑	X	0	0	0	PR1N 07[4]	PR1N 07[3]	PR1N 07[2]	PR1N 07[1]	PR1N 07[0]	XX
18th parameter	1	1	↑	X	0	0	0	PR1N 08[4]	PR1N 08[3]	PR1N 08[2]	PR1N 08[1]	PR1N 08[0]	XX

19th parameter	1	1	↑	X	0	0	PIR1 N1[1]	PIR1 N1[0]	0	0	PIR1 N0[1]	PIR1 N0[0]	XX
20th parameter	1	1	↑	X	0	0	PIR1 N3[1]	PIR1 N3[0]	0	0	PIR1 N2[1]	PIR1 N2[0]	XX
Description	Gamma Set B registers are applied to source pins numbered Sn + 2 (n=1, 2, ..., 239). However, Gamma Set A registers are applied to all source pins in the Idle Mode. See “Gamma Correction Function” for detailed description of the parameters.												

Gamma Set C (CAh)

CAh	Gamma set C												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	1	0	1	0	CAh
1st parameter	1	1	↑	X	0	0	0	PR2P 00[4]	PR2P 00[3]	PR2P 00[2]	PR2P 00[1]]	PR2P 00[0]	XX
2nd parameter	1	1	↑	X	0	0	0	PR2P 01[4]	PR2P 01[3]	PR2P 01[2]	PR2P 01[1]]	PR2P 01[0]	XX
3rd parameter	1	1	↑	X	0	0	0	PR2P 02[4]	PR2P 02[3]	PR2P 02[2]	PR2P 02[1]	PR2P 02[0]	XX
4th parameter	1	1	↑	X	PR2P 04[3]	PR2P 04[2]	PR2P 04[1]	PR2P 04[0]	PR2P 03[3]	PR2P 03[2]	PR2P 03[1]	PR2P 03[0]	XX
5th parameter	1	1	↑	X	0	0	0	0	PR2P 05[3]	PR2P 05[2]	PR2P 05[1]	PR2P 05[0]	XX
6th parameter	1	1	↑	X	0	0	0	PR2P 06[4]	PR2P 06[3]	PR2P 06[2]	PR2P 06[1]	PR2P 06[0]	XX
7th parameter	1	1	↑	X	0	0	0	PR2P 07[43]	PR2P 07[3]	PR2P 07[2]	PR2P 07[1]	PR2P 07[0]	XX
8th parameter	1	1	↑	X	0	0	0	PR2P 08[4]	PR2P 08[3]	PR2P 08[2]	PR2P 08[1]	PR2P 08[0]	XX
9th parameter	1	1	↑	X	0	0	PIR2P 1[1]	PIR2P 1[0]	0	0	PIR2P 0[1]	PIR2P 0[0]	XX
10th parameter	1	1	↑	X	0	0	PIR2P 3[1]	PIR2P 3[0]	0	0	PIR2P 2[1]	PIR2P 2[0]	XX
11th parameter	1	1	↑	X	0	0	0	PR2N 00[4]	PR2N 00[3]	PR2N 00[2]	PR2N 00[1]	PR2N 00[0]	XX
12th parameter	1	1	↑	X	0	0	0	PR2N 01[4]	PR2N 01[3]	PR2N 01[2]	PR2N 01[1]	PR2N 01[0]	XX
13th parameter	1	1	↑	X	0	0	0	PR2N 02[4]	PR2N 02[3]	PR2N 02[2]	PR2N 02[1]	PR2N 02[0]	XX
14th parameter	1	1	↑	X	PR2N 04[3]	PR2N 04[2]	PR2N 04[1]	PR2N 04[0]	PR2N 03[3]	PR2N 03[2]	PR2N 03[1]	PR2N 03[0]	XX
15th parameter	1	1	↑	X	0	0	0	0	PR2N 05[3]	PR2N 05[2]	PR2N 05[1]	PR2N 05[0]	XX
16th parameter	1	1	↑	X	0	0	0	PR2N 06[4]	PR2N 06[3]	PR2N 06[2]	PR2N 06[1]	PR2N 06[0]	XX
17th parameter	1	1	↑	X	0	0	0	PR2N 07[4]	PR2N 07[3]	PR2N 07[2]	PR2N 07[1]	PR2N 07[0]	XX
18th parameter	1	1	↑	X	0	0	0	PR2N 08[4]	PR2N 08[3]	PR2N 08[2]	PR2N 08[1]	PR2N 08[0]	XX

19th parameter	1	1	↑	X	0	0	PIR2 N1[1]	PIR2 N1[0]	0	0	PIR2 N0[1]	PIR2 N0[0]	XX
20th parameter	1	1	↑	X	0	0	PIR2 N3[1]	PIR2 N3[0]	0	0	PIR2 N2[1]	PIR2 N2[0]	XX
Description	Gamma Set C registers are applied to source pins numbered Sn + 3 (n=1, 2, ..., 239). However, Gamma Set A registers are applied to all source pins in the Idle Mode. See “Gamma Correction Function” for detailed description of the parameters.												

Power Control

Power Setting (Common Setting) (D0h)

D0h	Power Setting (Common Setting)												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	0	0	D0h
1st parameter	1	#A	#B	X	0	0	0	0	0	VC [2]	VC [1]	VC [0]	XX
2nd parameter	1	#A	#B	X	1	1	0	0	0	BT [2]	BT [1]	BT [0]	XX
3rd parameter	1	#A	#B	X	1	1	0	VRH [4]	VRH [3]	VRH [2]	VRH [1]	VRH [0]	XX

Description

Write #A="1" #B="↑"

Read #A="↑" #B="1" & Insert dummy read

VC[2:0]

The bit defines voltage level VCI1.

VC[2:0]	VCI1 (Step-up reference voltagae)
3'h0	Setting disabled
3'h1	0.94 x VCILVL
3'h2	0.89 x VCILVL
3'h3	Setting disabled
3'h4	Setting disabled
3'h5	0.76 x VCILVL
3'h6	Setting disabled
3'h7	1.00 x VCILVL

Description

BT[2:0]

The bit sets the voltage step-up factor according to selected voltage level. Smaller step-up factor leads to less power consumption.

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	Setting disabled			
3'h1				
3'h2				
3'h3	VCI1 x 2 [x 2]	-VCI1 [x -1]	DDVDH×3 [x 6]	-(VCI1+DDVDH×2) [x –5]
3'h4				-(DDVDH×2) [x –4]
3'h5				-(VCI1+DDVDH) [x –3]
3'h6			VCI1+DDVDH×2 [x 5]	-(VCI1+DDVDH×2) [x –5]
3'h7				-(DDVDH×2) [x -4]

Note 1: The step-up factors for VCI1 are shown in the brackets [].

Note 2: Set the following voltages within the respective voltage setting ranges: DDVDH=max.6.0V, VGH=max.18.0V, VGL=max. -13.5V, VCL=max.-3.0V.

VRH[4:0]

VRH[4:0]	VREG
5'h00	Halt (Hiz)
5'h01-5'h0F	Setting disabled
5'h10	VCIR x 1.600
5'h11	VCIR x 1.625
5'h12	VCIR x 1.650
5'h13	VCIR x 1.675
5'h14	VCIR x 1.700
5'h15	VCIR x 1.725
5'h16	VCIR x 1.750
5'h17	VCIR x 1.775
5'h18	VCIR x 1.800
5'h19	VCIR x 1.825
5'h1A	VCIR x 1.850
5'h1B	VCIR x 1.875
5'h1C	VCIR x 1.900
5'h1D	VCIR x 1.925
5'h1E	VCIR x 1.950
5'h1F	VCIR x 1.975

Note: Set the VC and VRH bits so that VREG ≤ DDVDH-0.5V.

VCOM Control (D1h)

D1h	VCOM Control												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	0	1	D1h
1st parameter	1	#A	#B	X	0	VCM [6]	VCM [5]	VCM [4]	VCM [3]	VCM [2]	VCM [1]	VCM [0]	XX
2nd parameter	1	#A	#B	X	0	0	0	VDV [4]	VDV [3]	VDV [2]	VDV [1]	VDV [0]	XX
3rd parameter	1	#A	#B	X	0	0	0	0	0	0	VCM R	SEL VCM	XX

Description

Write #A="1" #B="↑"

Read #A="↑" #B=" 1" & Insert dummy read

VCM[6:0]

The bit is used to set VCOMH voltage when VCOMR=1 within the range of VREG x 0.492 ~ 1.000. For details, see VCM setting table.

VDV[4:0]

The bit is used to set VCOM alternation amplitude within the range of VREG x 0.70 ~ 1.32. See VDV setting table.

VCMR

The bit is used to select how to set electrical potential VCOMH. The method to adjust the potential is to use either external variable resistance (VCOMR pin level) or internal electric volume.

VCMR=0: VCOMR pin level, external input to the driver

VCMR=1: Internal electric volume (defined by VCM [6:0])

SELVCM

SELVCM=0: VCM value written in internal NVM.
SELVCM=1: VCM value defined by D1h's 1st parameter (VCM[6:0]).

VCMR	**EEPROME pin**	**SELVCM**	**VCOMH level**
0	*	*	VCOMR pin level
1	GND	0	VCM value in internal NVM.
		1	VCM value defined by D1h's 1st parameter
	VCC	0	Setting disabled
		1	VCM value in external EEPROM

Description VCM setting table

VCM[6:0]	VCOMH
7'h 00	VREG X 0.492
7'h 01	VREG X 0.496
7'h 02	VREG X 0.500
7'h03	VREG X 0.504
7'h04	VREG X 0.508
7'h05	VREG X 0.512
7'h06	VREG X 0.516
7'h07	VREG X 0.520
7'h08	VREG X 0.524
7'h09	VREG X 0.528
7'h0A	VREG X 0.532
7'h0B	VREG X 0.536
7'h0C	VREG X 0.540
7'h0D	VREG X 0.544
7'h0E	VREG X 0.548
7'h0F	VREG X 0.552
7'h10	VREG X 0.556
7'h11	VREG X 0.560
7'h12	VREG X 0.564
7'h13	VREG X 0.568
7'h14	VREG X 0.572
7'h15	VREG X 0.576
7'h16	VREG X 0.580
7'h17	VREG X 0.584
7'h18	VREG X 0.588
7'h19	VREG X 0.592
7'h1A	VREG X 0.596
7'h1B	VREG X 0.600
7'h1C	VREG X 0.604
7'h1D	VREG X 0.608
7'h1E	VREG X 0.612
7'h1F	VREG X 0.616
7'h20	VREG X 0.620
7'h21	VREG X 0.624
7'h22	VREG X 0.628
7'h23	VREG X 0.632
7'h24	VREG X 0.636
7'h25	VREG X 0.640
7'h26	VREG X 0.644
7'h27	VREG X 0.648
7'h28	VREG X 0.652
7'h29	VREG X 0.656
7'h2A	VREG X 0.660
7'h2B	VREG X 0.664
7'h2C	VREG X 0.668
7'h2D	VREG X 0.672
7'h2E	VREG X 0.676
7'h2F	VREG X 0.680
7'h30	VREG X 0.684
7'h31	VREG X 0.688
7'h32	VREG X 0.692
7'h33	VREG X 0.696
7'h34	VREG X 0.700
7'h35	VREG X 0.704
7'h36	VREG X 0.708
7'h37	VREG X 0.712
7'h38	VREG X 0.716
7'h39	VREG X 0.720
7'h3A	VREG X 0.724
7'h3B	VREG X 0.728
7'h3C	VREG X 0.732
7'h3D	VREG X 0.736
7'h3E	VREG X 0.740
7'h3F	VREG X 0.744

VCM[6:0]	VCOMH
7'h40	VREG X 0.748
7'h41	VREG X 0.752
7'h42	VREG X 0.756
7'h43	VREG X 0.760
7'h44	VREG X 0.764
7'h45	VREG X 0.768
7'h46	VREG X 0.772
7'h47	VREG X 0.776
7'h48	VREG X 0.780
7'h49	VREG X 0.784
7'h4A	VREG X 0.788
7'h4B	VREG X 0.792
7'h4C	VREG X 0.796
7'h4D	VREG X 0.800
7'h4E	VREG X 0.804
7'h4F	VREG X 0.808
7'h50	VREG X 0.812
7'h51	VREG X 0.816
7'h52	VREG X 0.820
7'h53	VREG X 0.824
7'h54	VREG X 0.828
7'h55	VREG X 0.832
7'h56	VREG X 0.836
7'h57	VREG X 0.840
7'h58	VREG X 0.844
7'h59	VREG X 0.848
7'h5A	VREG X 0.852
7'h5B	VREG X 0.856
7'h5C	VREG X 0.860
7'h5D	VREG X 0.864
7'h5E	VREG X 0.868
7'h5F	VREG X 0.872
7'h60	VREG X 0.876
7'h61	VREG X 0.880
7'h62	VREG X 0.884
7'h63	VREG X 0.888
7'h64	VREG X 0.892
7'h65	VREG X 0.896
7'h66	VREG X 0.900
7'h67	VREG X 0.904
7'h68	VREG X 0.908
7'h69	VREG X 0.912
7'h6A	VREG X 0.916
7'h6B	VREG X 0.920
7'h6C	VREG X 0.924
7'h6D	VREG X 0.928
7'h6E	VREG X 0.932
7'h6F	VREG X 0.936
7'h70	VREG X 0.940
7'h71	VREG X 0.944
7'h72	VREG X 0.948
7'h73	VREG X 0.952
7'h74	VREG X 0.956
7'h75	VREG X 0.960
7'h76	VREG X 0.964
7'h77	VREG X 0.968
7'h78	VREG X 0.972
7'h79	VREG X 0.976
7'h7A	VREG X 0.980
7'h7B	VREG X 0.984
7'h7C	VREG X 0.988
7'h7D	VREG X 0.992
7'h7E	VREG X 0.996
7'h7F	VREG X 1.000

Description

VDV setting table

VDV[4:0]	VCOM amplitude
5'h00	VREG × 0.70
5'h01	VREG × 0.72
5'h02	VREG × 0.74
5'h03	VREG × 0.76
5'h04	VREG × 0.78
5'h05	VREG × 0.80
5'h06	VREG × 0.82
5'h07	VREG × 0.84
5'h08	VREG × 0.86
5'h09	VREG × 0.88
5'h0A	VREG × 0.90
5'h0B	VREG × 0.92
5'h0C	VREG × 0.94
5'h0D	VREG × 0.96
5'h0E	VREG × 0.98
5'h0F	VREG × 1.00

VDV[4:0]	VCOM amplitude
5'h10	VREG×1.02
5'h11	VREG×1.04
5'h12	VREG×1.06
5'h13	VREG×1.08
5'h14	VREG×1.10
5'h15	VREG×1.12
5'h16	VREG×1.14
5'h17	VREG×1.16
5'h18	VREG×1.18
5'h19	VREG×1.20
5'h1A	VREG×1.22
5'h1B	VREG×1.24
5'h1C	VREG×1.26
5'h1D	VREG×1.28
5'h1E	VREG×1.30
5'h1F	VREG×1.32

Note: Make sure that VCOM amplitude is 6.0V or smaller.

Power Setting for Normal Mode (D2h),
Power Setting for Partial Mode (D3h)
Power Setting for Idle Mode (D4h)

D2h	**Power Setting for Normal Mode**												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	1	0	D2h
1st parameter	1	#A	#B	X	0	1	1	0	0	0	AP0 [1]	AP0 [0]	XX
2nd parameter	1	#A	#B	X	0	DC10 [2]	DC10 [1]	DC10 [0]	0	DC00 [2]	DC00 [1]	DC00 [0]	XX
D3h	**Power Setting for Partial Mode**												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	1	1	D3h
1st parameter	1	#A	#B	X	0	1	1	0	0	0	AP1 [1]	AP1 [0]	XX
2nd parameter	1	#A	#B	X	0	DC11 [2]	DC11 [1]	DC11 [0]	0	DC01 [2]	DC01 [1]	DC01 [0]	XX
D4h	**Power Setting for Idle Mode**												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	1	0	0	D4h
1st parameter	1	#A	#B	X	0	1	1	0	0	0	AP2 [1]	AP2 [0]	XX
2nd parameter	1	#A	#B	X	0	DC12 [2]	DC12 [1]	DC12 [0]	0	DC02 [2]	DC02 [1]	DC02 [0]	XX
Description	Write #A="1" #B=" ↑ " Read #A=" ↑ " #B=" 1" & Insert dummy read Power control is defined for each mode. D2h is enabled when Normal Mode is On, Idle Mode is Off. D3h is enabled when Partial Mode is On, Idle Mode is Off D4h is inabled when Normal Mode is On, Idle Mode is On, and Partial Mode is On, Idle Mode is On.												

Description

AP0[1:0], AP1[1:0], AP2[1:0]

These bits adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current will enhance the drivability of the LCD, however more current willl be consumed. Adjust the constant current taking the trade-off between the display quality and the current consumption into account .

APn[1:0]	**Constant current in operational amplifier in LCD power supply circuit**
2'h0	Halt operational amplifier and step-up circuits
2'h1	0.5
2'h2	0.75
2'h3	1

The values represent the ratios of constant current in respective AP[1:0] settings to the constant current when APn[1:0] is set to 2'h3.

DC10[2:0], DC11[2:0], DC12[2:0]

These bits set the step-up clock frequency of the step-up circuit 2.

DC1n[2:0]	**Step-up circuit 2 Step-up clock frequency (f_{DCDC2})**
3'h0	Halt operatipn
3'h1	Setting disabled
3'h2	Line frequency / 4
3'h3	Line frequency / 8
3'h4	Line frequency / 16
3'h5	Setting disabled
3'h6	Setting disabled
3'h7	Setting disabled

Step-up clock frequency calculation of the step-up circuit 2

Step-up clock frequency (f_{DCDC2}) =
{Line frequency / 2^N} [Hz] =
{Internal clock frequency (f_{osc}) / Clocks per line x Division ratio x 2^N}

f_{osc}: Internal clock frequency
Clocks per line: RTNn[4:0]
Division ratio: DIVn[1:0]
N: DC1n[2:0]

Description

DC00[2:0], DC01[2:0], DC02[2:0]

These bits set the step-up clock frequency of the step-up circuit 1.

DC0n[2:0]	Step-up circuit 1 Step-up clock frequency (f_{DCDC1})
3'h0	Halt operation
3'h1	Setting disabled
3'h2	Setting disabled
3'h3	Setting disabled
3'h4	f_{osc} / 8
3'h5	f_{osc} / 16
3'h6	f_{osc} / 32
3'h7	Setting disabled

Note: Make sure $f_{DCDC1} \geq f_{DCDC2}$.

Step-up clock frequency calculation of the step-up circuit 1

Step-up clock frequency (f_{DCDC1}) =
{Reference clock frequency (f_{osc}) / 2^{N-1}} [Hz] = {Internal clock frequency (f_{osc}) / Division ratio x 2^{N-1}}

f_{osc}: Internal clock frequency
Division ratio: DIVn[1:0]
N: DC1n[2:0]

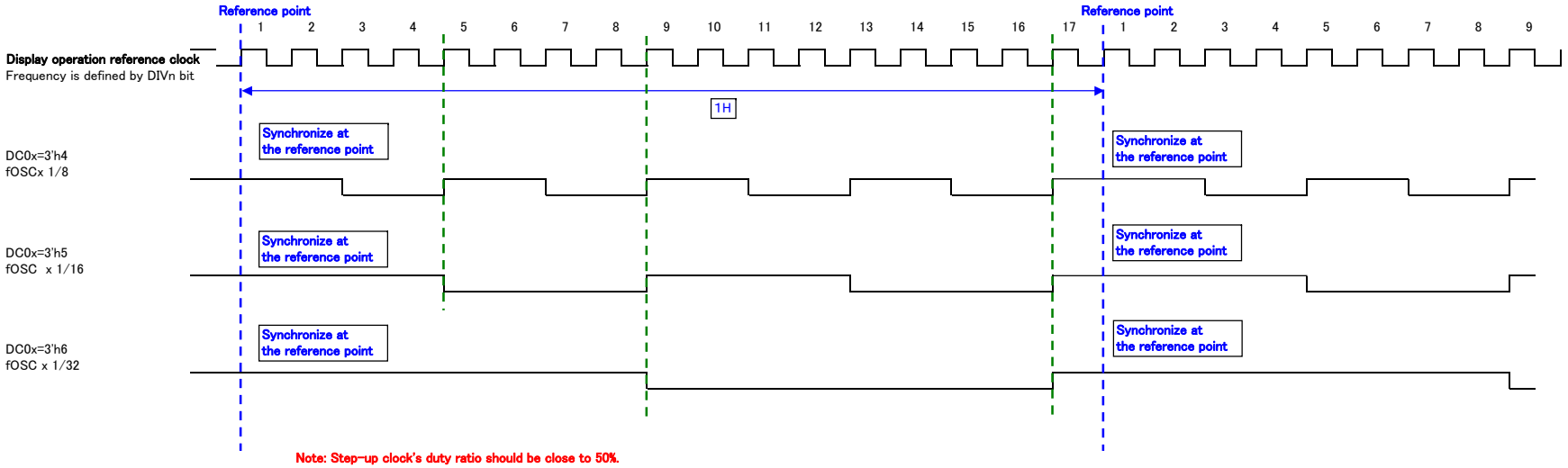
Step-up clock and display operation synchronize with each other. Frequency deviding clock's counter is reset at every 1H period's beginning.

Table 21 Display Mode and Valid Register Setting

Display Mode	Operationalamplifier constant current	Step-up circuit 1 Step-up clock frequency	Step-up circuit 2 Step-up clock frequency
Normal mode + Idle mode off	D2h:AP0	D2h:DC00	D2h:DC10
Partial mode + Idle mode off	D3h:AP1	D3h:DC01	D3h:DC11
Idle mode on + (Normal / Partial mode)	D4h:AP2	D4h:DC02	D4h:DC12

■DC0x value and clock signal waveform example

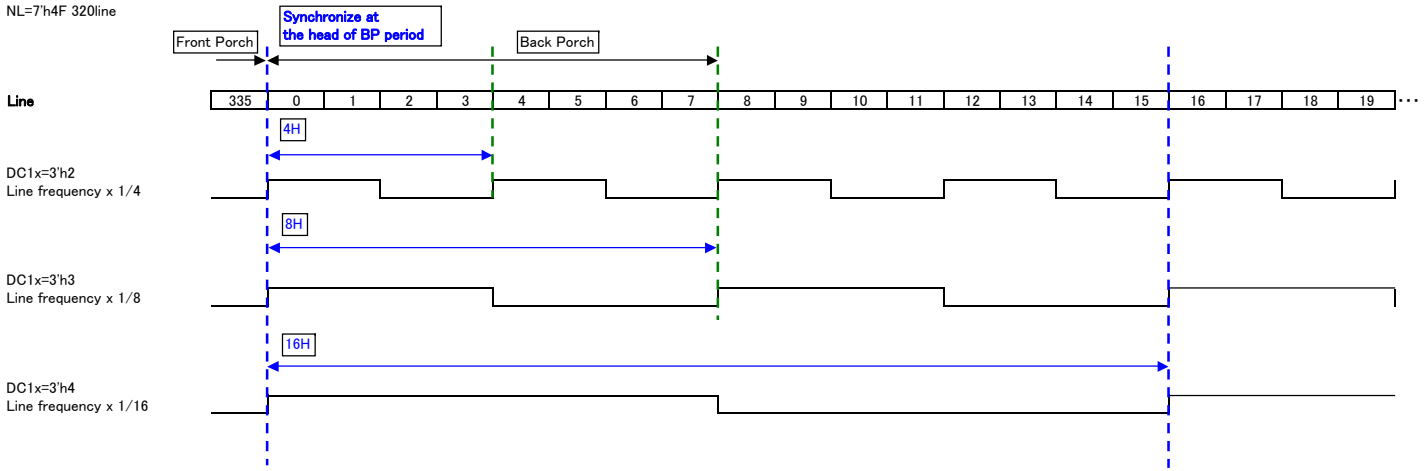
RTN=5'h10 1H=17CLK
DIVn=2'h1 (x 1/2)



Note: Step-up clock's duty ratio should be close to 50%.

■DC1x value and clock signal waveform example

BP=FP=8'h8
NL=7'h4F 320line



NVM Control

NVM Access Control (E0h)

E0h	NV Memory Access Control												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	0	0	0	0	E0h
1st parameter	1	#A	#B	X	FTT	CALB	OP [1]	OP [0]	0	NVAD [2]	NVAD [1]	NVAD [0]	XX
2nd parameter	1	#A	#B	X	0	0	0	0	0	0	0	NVV RF	XX

Description

Write #A="1" #B="↑"

Read #A="↑" #B="1" & Insert dummy read

FTT

NVM access enable bit. When FTT=1, access to the NVM is enabled.

CALB

When CALB=1, all data on the NVM is read to be updated onto the corresponding registers. CALB=0 is returned when loading is finished.

OP[1:0]

NVM control bit. The bit is used to control writing and rerasing.

OP[1:0]	Operation
2'h0	Halt
2'h1	Write
2'h2	Setting disabled
2'h3	Erase

NVAD

The bit specifies the NVM addresses to which data is written / from which data is erased. One address consists of 16 bits.

To write, set the write data to NVDAT (E1h) and command write operation using OP bit.

To erase, define the erase address and command erase operation using OP bit.

See "NVM Control Sequence" for detail.

Description

NVAD[1:0]	NVDAT [15]/[7]	NVDAT [14]/[6]	NVDAT [13]/[5]	NVDAT [12]/[4]	NVDAT [11]/[3]	NVDAT [10]/[2]	NVDAT [9]/[1]	NVDAT [8]/[0]
3'h0 (MS byte)	1	T_VCM [6]	T_VCM [5]	T_VCM [4]	T_VCM [3]	T_VCM [2]	T_VCM [1]	T_VCM [0]
3'h0 (LS byte)	1	1	1	1	1	1	1	1
3'h1 (MS byte)	T_ID1 [15]	T_ID1 [14]	T_ID1 [13]	T_ID1 [12]	T_ID1 [11]	T_ID1 [10]	T_ID1 [9]	T_ID1 [8]
3'h1 (LS byte)	T_ID1 [7]	T_ID1 [6]	T_ID1 [5]	T_ID1 [4]	T_ID1 [3]	T_ID1 [2]	T_ID1 [1]	T_ID1 [0]
3'h2 (MS byte)	T_ID2 [15]	T_ID2 [14]	T_ID2 [13]	T_ID2 [12]	T_ID2 [11]	T_ID2 [10]	T_ID2 [9]	T_ID2 [8]
3'h2 (LS byte)	T_ID2 [7]	T_ID2 [6]	T_ID2 [5]	T_ID2 [4]	T_ID2 [3]	T_ID2 [2]	T_ID2 [1]	T_ID2 [0]

MS byte: NVDAT[15:8]. LS byte: NVDAT[7:0].

T_VCM[6:0]: VCOMH level adjusting value when EEPROME=GND (external EEPROM is not used) and SELVCM=0.

T_ID1[15:0]: Supplier ID read by read_DDB_start (A1h) and read_DDB_continue (A8h) commands when EEPROME=GND (external EEPROM is unused).

T_ID2[15:0]: Supplier Elective Data read by read_DDB_start (A1h) and read_DDB_continue (A8h) commands when EEPROME=GND (external EEPROM is unused).

NVVRF

The bit is used to set erase verify mode to be used only in the NVM Erase Sequence.

See NVM Erase Sequence for detail.

NVM Write Data (E1h)

E1h	NV Memory Write Data												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	0	0	0	1	E1h
1st parameter	1	#A	#B	X	NVDAT [15]	NVDAT [14]	NVDAT [13]	NVDAT [12]	NVDAT [11]	NVDAT [10]	NVDAT [9]	NVDAT [8]	XX
2nd parameter	1	#A	#B	X	NVDAT [7]	NVDAT [6]	NVDAT [5]	NVDAT [4]	NVDAT [3]	NVDAT [2]	NVDAT [1]	NVDAT [0]	XX
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read **NVDAT[15:0]** The bit is used to specify data to be written to the NVM. See NVAD description for relationship between address and data.												

NVM Data Load Register (E2h)

E2h	NV Memory Data Load Register												
	DCX	RDX	WRX	DB17-8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	0	0	1	0	E2h
1st Parameter	1	#A	#B	X	1	T_VCM[6]	T_VCM[5]	T_VCM[4]	T_VCM[3]	T_VCM[2]	T_VCM[1]	T_VCM[0]	XX
2nd Parameter	1	#A	#B	X	1	1	1	1	1	1	1	1	XX
3rd Parameter	1	#A	#B	X	T_ID1 [15]	T_ID1 [14]	T_ID1 [13]	T_ID1 [12]	T_ID1 [11]	T_ID1 [10]	T_ID1 [9]	T_ID1 [8]	XX
4th Parameter	1	#A	#B	X	T_ID1 [7]	T_ID1 [6]	T_ID1 [5]	T_ID1 [4]	T_ID1 [3]	T_ID1 [2]	T_ID1 [1]	T_ID1 [0]	XX
5th Parameter	1	#A	#B	X	T_ID2 [15]	T_ID2 [14]	T_ID2 [13]	T_ID2 [12]	T_ID2 [11]	T_ID2 [10]	T_ID2 [9]	T_ID2 [8]	XX
6th Parameter	1	#A	#B	X	T_ID2 [7]	T_ID2 [6]	T_ID2 [5]	T_ID2 [4]	T_ID2 [3]	T_ID2 [2]	T_ID2 [1]	T_ID2 [0]	XX
Description	Data stored in the internal NVM is loaded so that data written to the NVM can be confirmed. Read #A=" ↑ " #B=" 1" & Insert dummy read 1st parameter : Returns T_VCM[6:0] 2nd parameter: Returns FFh 3rd parameter: Returns T_ID1[15:8] 4th parameter: Returns T_ID1[7:0] 5th parameter: Returns T_ID2[15:8] 6th parameter: Returns T_ID2[7:0] X = Don't care												

EEPROM Control

EEPROM Write Enable (E8h)

E8h	EEPROM Write Enable												
	DCX	RDX	WRX	DB17~8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	1	0	0	0	E8h
Parameter	None												
Description	This command is used to enable write to the EEPROM. This command does not need a parameter. After executing this command, 16 cycle or more of EEPROM serial clock (SCL) is required before writing next command. This command does not have any effect on register, display, host processor interface or power mode settings.												

EEPROM Write Disable (E9h)

E9h	ERWDS(EEPROM write disable)												
	DCX	RDX	WRX	DB17~8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	1	0	0	1	E9h
Parameter	None												
Description	This command is used to disable EEPROM write. This command does not need a parameter. After executing this command, 16 cycle or more of EEPROM serial clock (SCL) is required before writing next command. This command does not have any effect on register, display, host processor interface or power mode settings.												

EEPROM Word Write (EAh)

EAh	EEPROM Word write												
	DCX	RDX	WRX	DB17~8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	1	0	1	0	EAh
1st parameter	1	1	↑	X	DW [15]	DW [14]	DW [13]	DW [12]	DW [11]	DW [10]	DW [9]	DW [8]	XX
2nd parameter	1	1	↑	X	DW [7]	DW [6]	DW [5]	DW [4]	DW [3]	DW [2]	DW [1]	DW [0]	XX
Description	The parameters are write data for the EEPROM. The command needs 2 byte parameter DW[15:0]. Note 1: After executing this command (after writing the 2nd parameter), 30 cycle or more of EEPROM serial clock (SLC) is required before writing next command. Note 2: To specify start position of write operation, use EEPROM Address Set command (ECh). Note 3: Write address of the EEPROM is automatically incremented after executing this command. Input 1st Parameter-2nd Parameter (EAh) repeatedly to write to consecutive address. Note 4: Address must specified again by ECh command to write to inconsecutive address. This command does not have any effect on register, display, host processor interface or power mode settings.												

EEPROM Word Read (EBh)

EBh	EEPROM Word Read												
	DCX	RDX	WRX	DB17~8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	1	0	1	1	EBh
1st parameter	1	↑	1	X	D15	D14	D13	D12	D11	D10	D9	D8	XX
2nd parameter	1	↑	1	X	D7	D6	D5	D4	D3	D2	D1	D0	XX
Description	This command is used to read 1 word (2 byte) parameter data stored in the EEPROM. Note 1: After executing this command (after writing the 2nd parameter), 55 cycle or more of EEPROM serial clock (SLC) is required before writing next command. Note 2: To specify start position of write operation, use EEPROM Address Set command (ECh). Note 3 The first byte of the read data is undefined. The data is read from the EEOROM from the 2nd word onward. Note 4: Read address of the EEPROM is automatically incremented after executing this command. Input EBh repeatedly to write to consecutive address. Note 5: Address must specified again by ECh command to read inconsecutive address.												

EEPROM Address Set (ECh)

ECh	EEPROM Address Set												
	DCX	RDX	WRX	DB17~8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	1	1	0	0	ECh
1st parameter	1	#A	#B	X	A7	A6	A5	A4	A3	A2	A1	A0	XX
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read This command is used to define write, read and erase address of the EEPROM. The command needs 1 byte parameter. When 2K-bit EEPROM is used: A0 to A6 bits define the address. Write "0" to A7. When 4K-bit EEPROM is used: A0 to A6 bits define the address. This command does not have any effect on register, display, host processor interface or power mode settings. The addresses are automatically incremented after executing EAh and EBh commands.												

State Transition Diagram

State Transition Diagram

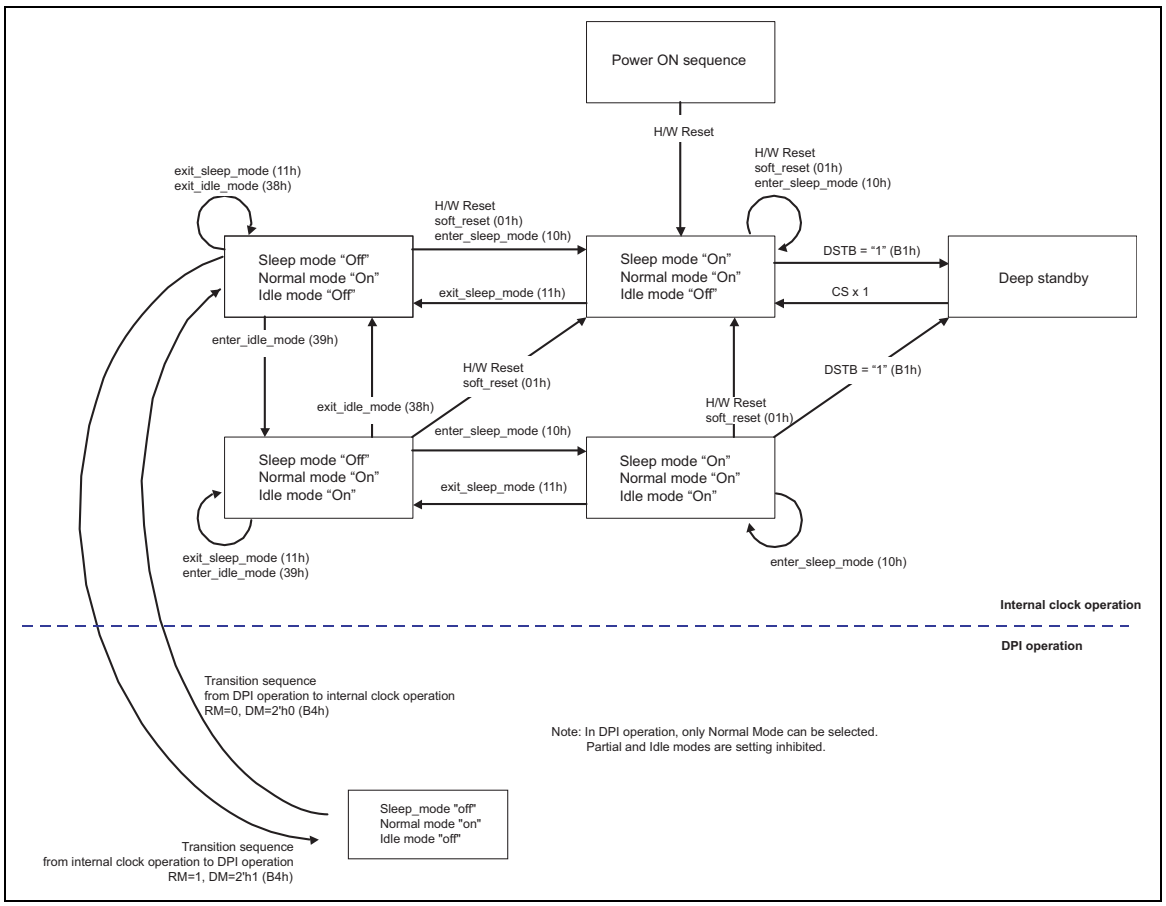


Figure 27

■ R61516 State & Command sequence

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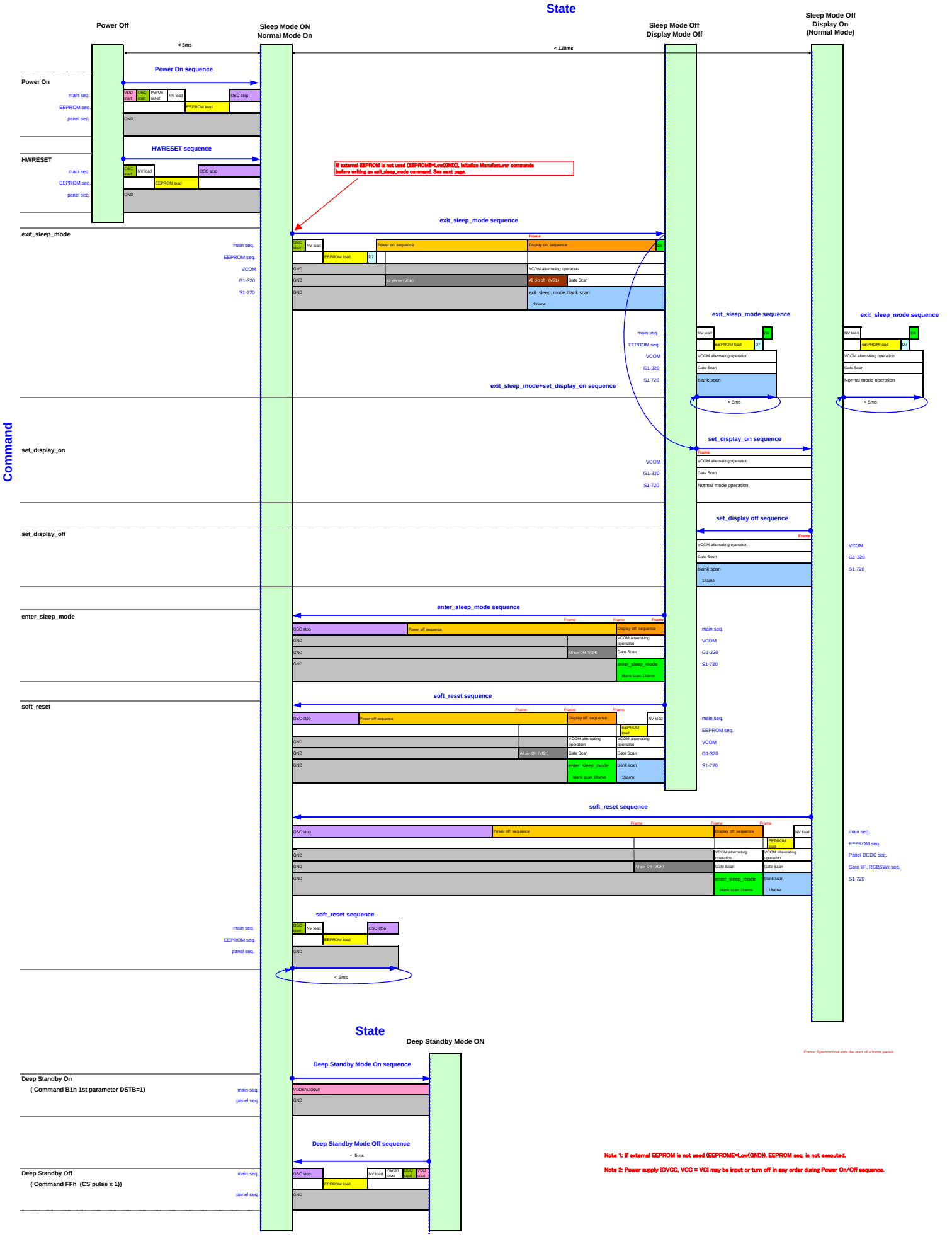
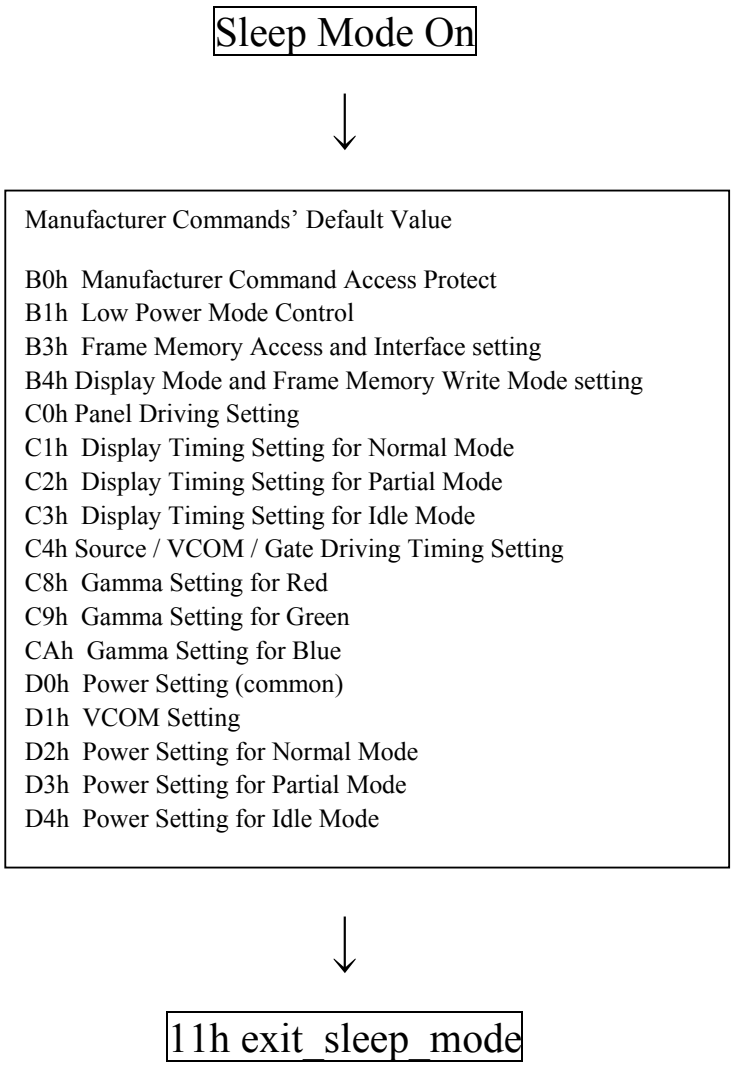


If EEPROM is not used:

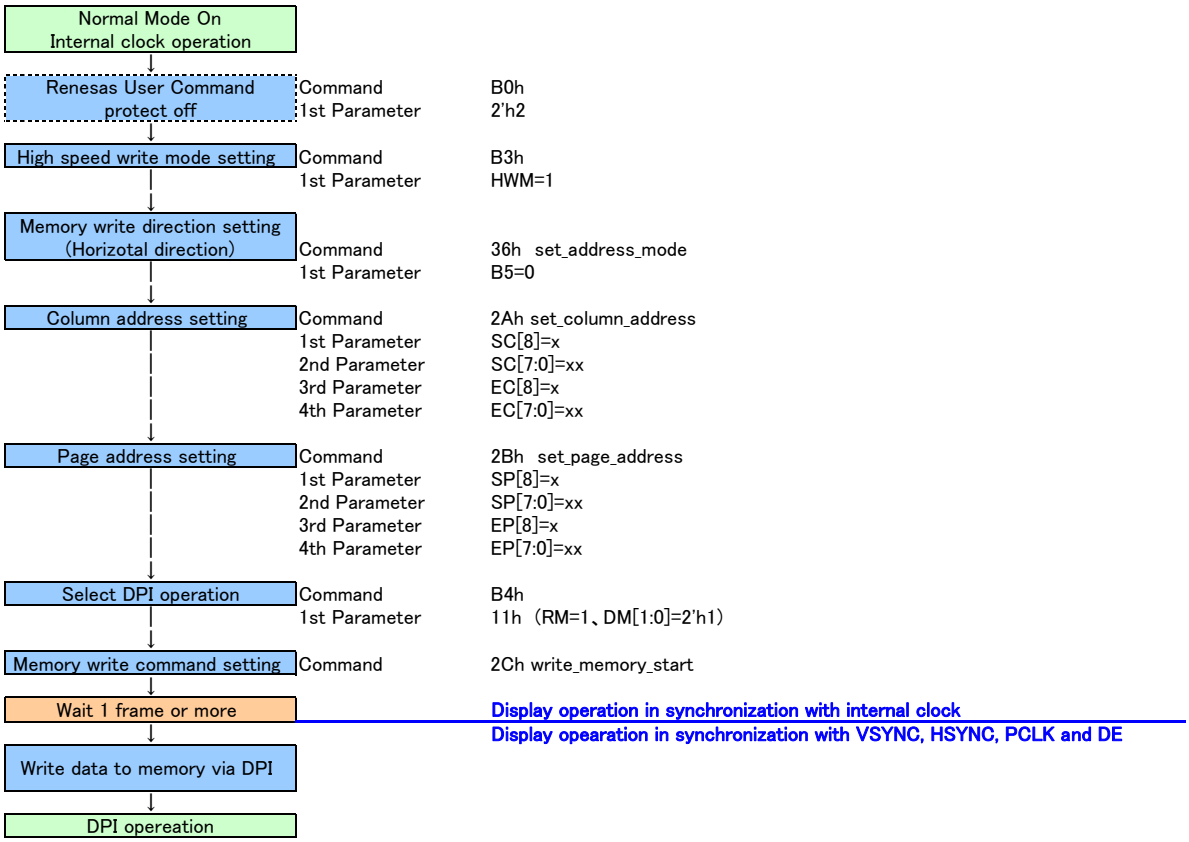
If EEPROM is not used, initialize following Manufacturer commands before writing an exit_sleep_mode command.



Internal Clock Operation

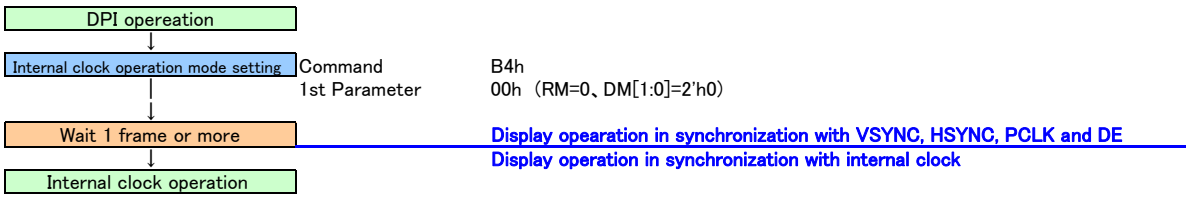
■Transition sequence

1.Transition sequence from internal clock operation to DPI operation



＊DPI signals (VSYNC, HSYNC, PCLK, DE, DB[17:0]) must be supplied before setting DM and RM.

2. Transition sequence from DPI operation to internal clock operation



＊DPI signals must be supplied for 2 frame period time after DM and RM are set.

Reset

The R61516's initial internal setting is done with a RESET input. During the RESET period, no access, whether it is command write or frame memory data write operation, is accepted. The source driver unit and the power supply circuit unit are also reset to the respective initial states when RESET signal is inputted to the R61516.

1. Initial state of command

   The initial state of command is shown in Default Modes and Values table in Command List. The command setting is initialized to the default value when executing a Hardware Reset.

2. Frame Memory data initial state

   The Franme Memory data is not automatically initialized by inputting RESET. It needs to be initialized by software during Display Off period.

3. Input/output pin initial state

Table 22 INPUT/OUTPUT Pin Initial State

Pin name	INPUT/OUTPUT Pin Initial State	Pin name	INPUT/OUTPUT Pin Initial State
DB[17:0]	Hi-Z	VREG	GND
DOUT	Hi-Z	VCOML	GND
TE	GND	VCOMH	VCI(DDVDH)
SCS	GND	VCL	GND
SCL	VCC	VGL	GND
SDO	GND	VLOUT3	GND
VDD	1.5V	VLOUT2	VCI
VCI1	Hi-Z	DDVDH	VCI
C11P/C11M	Hi-Z/Hi-Z	VLOUT1	VCI(DDVDH)
C12P/C12M	Hi-Z/Hi-Z	VCOM	GND
C13P/C13M	Hi-Z/GND	VCOMOL/VCOMOR	GND
C21P/C21M	VCI/GND	S1-720	GND
C22P/C22M	VCI/GND	G1-320	GND

EEPROM Serial Interface

The R61516 supports micro-wire based serial interface to access EEPROM. Given Manufacturer commands' default values are loaded from EEPROM via this interface. 2k bit or 4k bit EEPROM may be connected to the R61516.

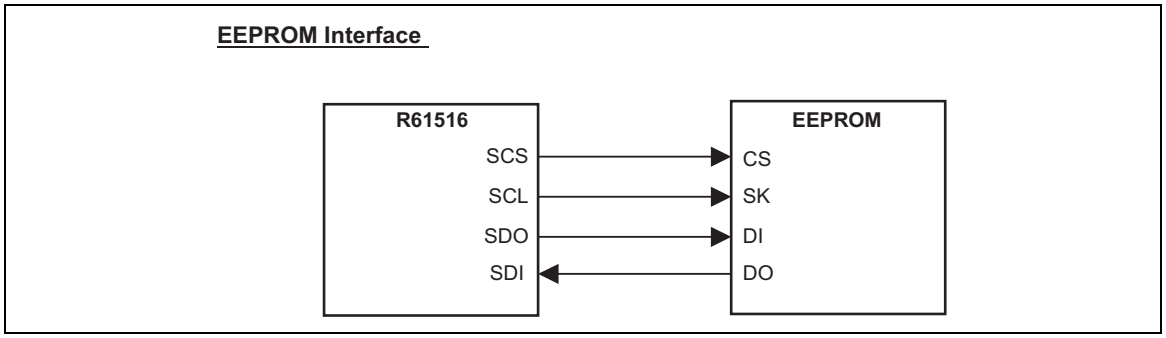


Figure 28 EEPROM Interface

Manufacturer Command – EEPROM Instruction set table

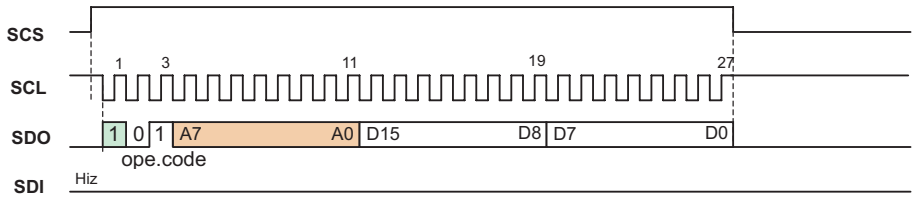
R61516 Manufacturer Command		EEPROM Instruction set	S	Ope. Code		Address								Date
			1	2	3	4	5	6	7	8	9	10	11	12~27
E8h	ERWEN	EWEN (Write enable)	1	0	0	1	1	x	x	x	x	x	x	-
E9h	ERWDS	EWDS (Write disable)	1	0	0	0	0	x	x	x	x	x	x	-
EAh	ERWR	WRITE (Data write)	1	0	1	(A7)/X	A6	A5	A4	A3	A2	A1	A0	Input D15-D0
EBh	ERRD	READ (Data read)	1	1	0	(A7)/X	A6	A5	A4	A3	A2	A1	A0	Input D15-D0
ECh	ERADR Note 1)	-	-	-	-	-	-	-	-	-	-	-	-	-

Note 1: ERADR (BEh) defines EEPROM address. No command is written to the EEPROM.

Note 2: If 4k bit EEPROM is connected, most significant address A7 is enabled. If 2k bit EEPROM is connected, most significant address is "don't care".

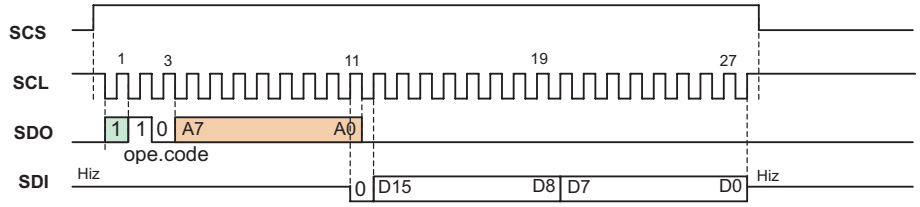
EEPROM Serial Interface Waveforms

1. E8h: ERWR (WRITE)



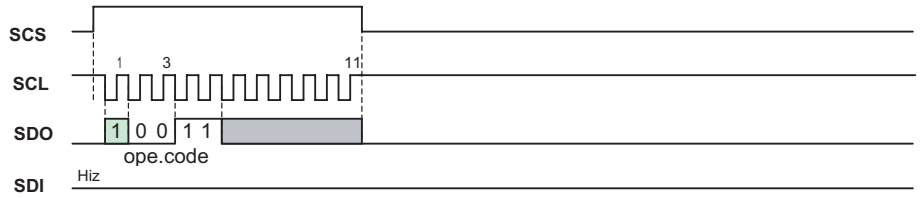
Note: If 2 k bit EEPROM is connected, A7 = Don't care.

2. E9h: ERRD (READ)



Note: If 2 k bit EEPROM is connected, A7 = Don't care.

3. EAh: ERWEN (EWEN)



4. EBh: ERWDS (EWDS)

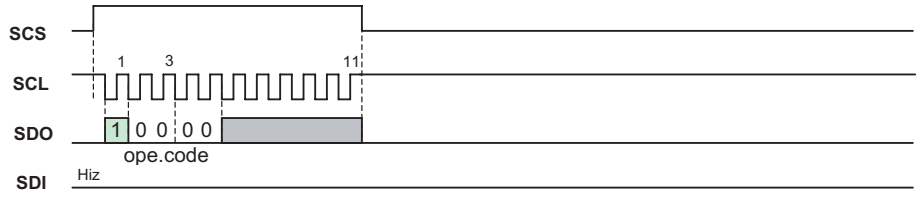
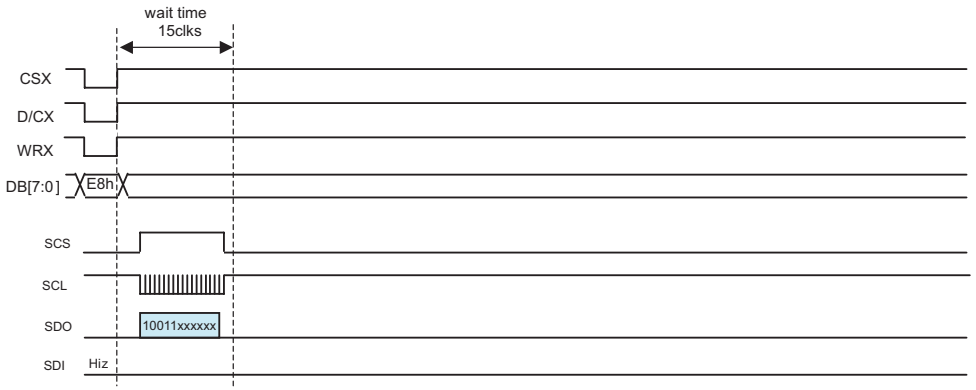


Figure 29

EEPROM Serial Interface Protocol (R61516-EEPROM)

Note: Number of clock decided as wait time refers to SCL cycle.

1) E8H: EEPROM WRITE ENABLE (ERWEN)



2) E9H: EEPROM WRITE DISABLE (ERWDS)

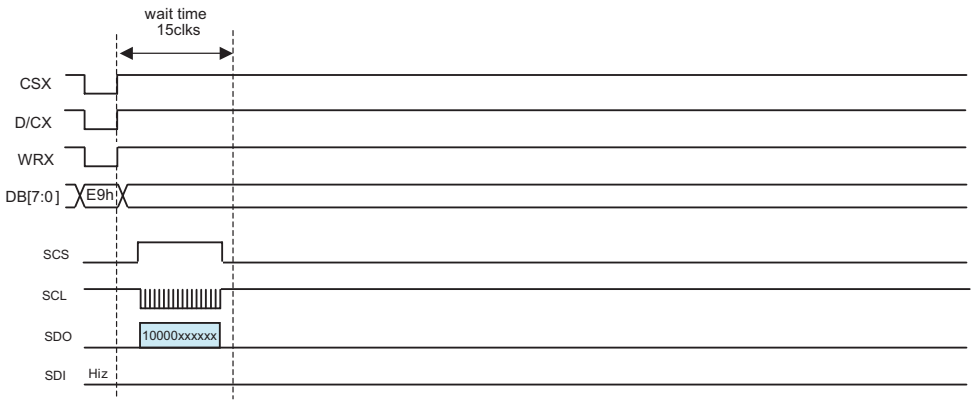
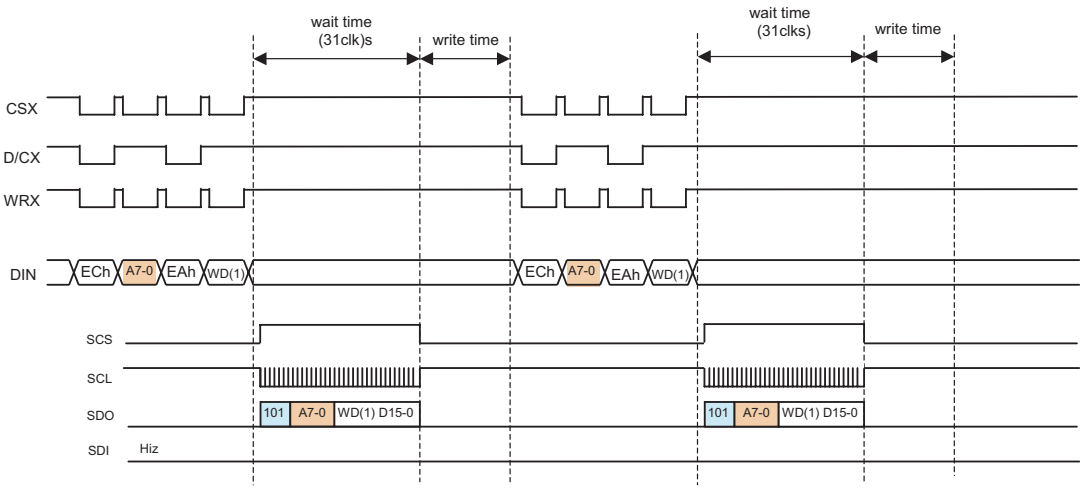


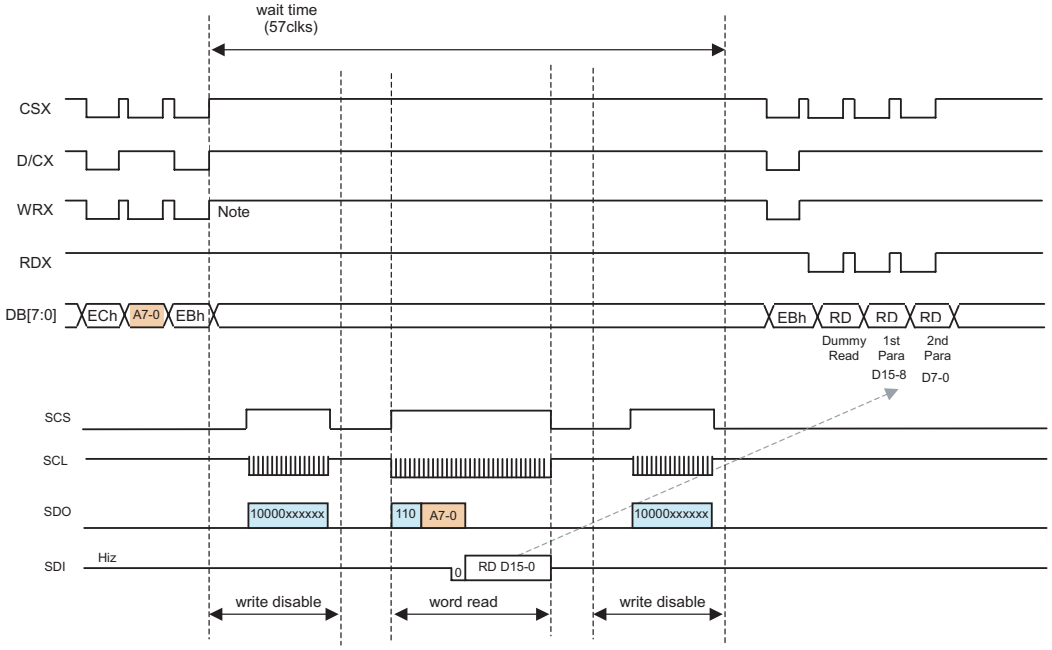
Figure 30

3) EAH: EEPROM WORD WRITE (ERWR)



Note: The R61516 does not support verify function. Write to EEPROM after given wait time.

4) EBH: EEPROM WORD READ (ERRD)

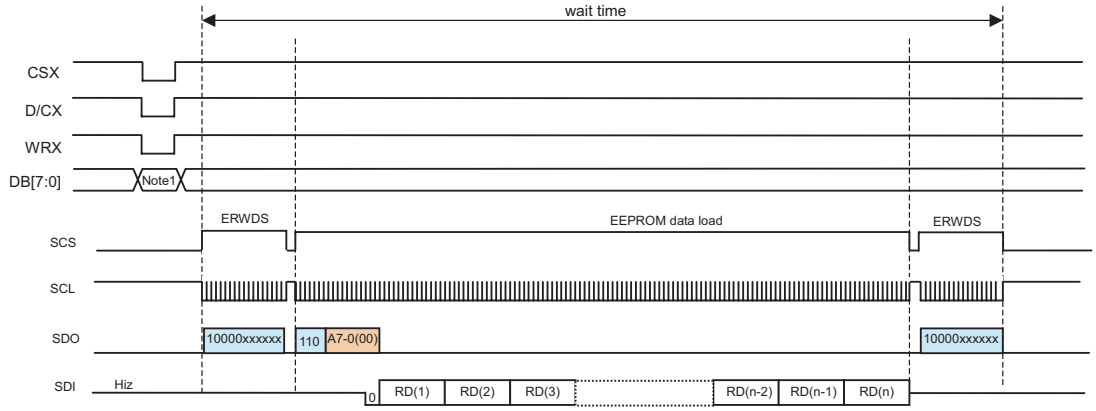


Note: After transferring EBh ERRD , wait 57 SCL clock cycle before reading the 1st parameter.

Figure 31

5) EEPROM LOAD (ERLOAD) **POWERON / HWRESET / EXIT_SLEEP_MODE / SWRESET SEQUENCE**

This operation is executed during Power On / HWRESET / Exit Sleep Mode / SWRESET sequence.
EEPROM data is loaded to User and Manufacturer's commands following bit allocation on EEPROM.



Note 1: This command is executed internally during Power On / HWRESET / Exit Sleep Mode / SWRESET sequence.
Note 2: EEPROM data read by an exit_sleep_mode command is compared to the R61516's command register values. (D7h Self-diagnostic Function)

Figure 32

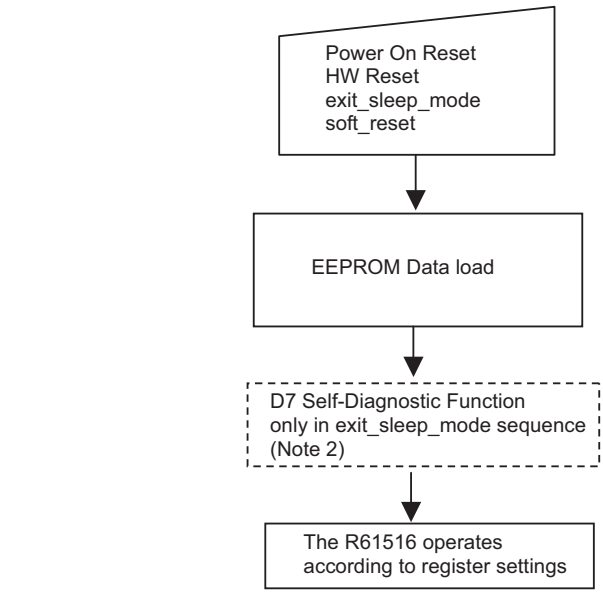
EEPROM Data Load Function

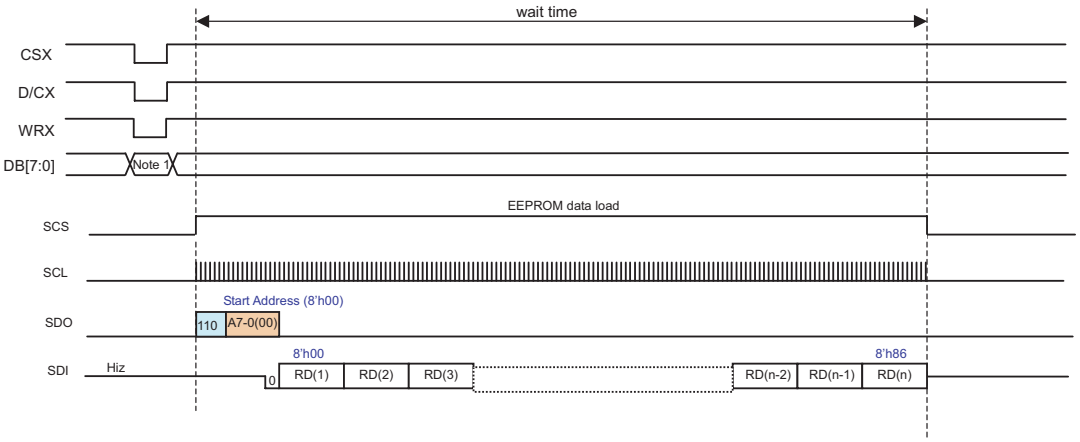
If EEPROME = High (VCC), the R61516 loads data stored in external EEPROM to User / Manufacturer command registers.

EEPROM Data Load Commands and Sequences

Sequences	Power On sequence
	HWRESET sequence
	exit_sleep_mode sequence (D7 Self Diagnostic Function is executed only during this sequence only)
	soft_reset sequence

EEPROM Data Load Sequence





Note 1: This command is executed internally during Power On / HWRESET / Exit Sleep Mode / SWRESET sequence when EEPROME = High (VCC) and external EEPROM is used.

Note 2: D7 Self-Diagnostic Function is executed only in exit_sleep_mode sequence.

Figure 33

■R61516 EEPROM Bit Allocation Table

EEPROM Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Command	ParamNo	ParamNo
0	0	0	0	1	0	1	0	1	0	0	0	1	0	1	1	0			
1	DDB0[7]	DDB0[6]	DDB0[5]	DDB0[4]	DDB0[3]	DDB0[2]	DDB0[1]	DDB0[0]	DDB1[7]	DDB1[6]	DDB1[5]	DDB1[4]	DDB1[3]	DDB1[2]	DDB1[1]	DDB1[0]	A1	1	2
2	DDB2[7]	DDB2[6]	DDB2[5]	DDB2[4]	DDB2[3]	DDB2[2]	DDB2[1]	DDB2[0]	DDB3[7]	DDB3[6]	DDB3[5]	DDB3[4]	DDB3[3]	DDB3[2]	DDB3[1]	DDB3[0]	A1	3	4
3	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	A1	5	6
4	0	0	0	0	0	0	MCAP[1]	MCAP[0]	0	0	0	0	0	0	0	0	B0	1	2
5	0	0	0	0	0	0	0	DSTB	0	0	0	0	0	0	0	0	B1	1	–
6	0	0	0	0	0	0	WEMODE	HWM	0	0	0	0	0	TEI[2]	TEI[1]	TEI[0]	B3	1	2
7	0	0	0	0	0	DENC[2]	DENC[1]	DENC[0]	0	0	EPF[1]	EPF[0]	0	0	0	DFM[0]	B3	3	4
8	0	0	0	0	0	0	RIM[1]	RIM[0]	0	0	0	0	0	0	0	0	B3	5	–
9	0	0	0	RM	0	0	DM[1]	DM[0]	0	0	0	0	0	0	0	0	B4	1	–
10	0	0	0	REV	SM	GS	BGR	SS	0	NL[6]	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	NL[0]	C0	1	2
11	0	SCN[6]	SCN[5]	SCN[4]	SCN[3]	SCN[2]	SCN[1]	SCN[0]	0	0	0	0	0	0	0	NW[0]	C0	3	4
12	0	0	0	0	0	0	BLV	PTV	0	0	BLS	NDL	0	PTS[2]	PTS[1]	PTS[0]	C0	5	6
13	0	0	0	PTG	ISC[3]	ISC[2]	ISC[1]	ISC[0]	PCDIVH[3]	PCDIVH[2]	PCDIVH[1]	PCDIVH[0]	PCDIVL[3]	PCDIVL[2]	PCDIVL[1]	PCDIVL[0]	C0	7	8
14	0	0	0	0	0	0	0	BCO	0	0	0	0	0	0	DIVO[1]	DIVO[0]	C1	1	2
15	0	0	RTNO[5]	RTNO[4]	RTNO[3]	RTNO[2]	RTNO[1]	RTNO[0]	BPO[7]	BPO[6]	BPO[5]	BPO[4]	BPO[3]	BPO[2]	BPO[1]	BPO[0]	C1	3	4
16	FPO[7]	FPO[6]	FPO[5]	FPO[4]	FPO[3]	FPO[2]	FPO[1]	FPO[0]	0	0	0	0	0	0	0	0	C1	5	–
17	0	0	0	0	0	0	0	BC1	0	0	0	0	0	0	DIV1[1]	DIV1[0]	C2	1	2
18	0	0	RTN1[5]	RTN1[4]	RTN1[3]	RTN1[2]	RTN1[1]	RTN1[0]	BP1[7]	BP1[6]	BP1[5]	BP1[4]	BP1[3]	BP1[2]	BP1[1]	BP1[0]	C2	3	4
19	FP1[7]	FP1[6]	FP1[5]	FP1[4]	FP1[3]	FP1[2]	FP1[1]	FP1[0]	0	0	0	0	0	0	0	0	C2	5	–
20	0	0	0	0	0	0	0	BC2	0	0	0	0	0	0	DIV2[1]	DIV2[0]	C3	1	2
21	0	0	RTN2[5]	RTN2[4]	RTN2[3]	RTN2[2]	RTN2[1]	RTN2[0]	BP2[7]	BP2[6]	BP2[5]	BP2[4]	BP2[3]	BP2[2]	BP2[1]	BP2[0]	C3	3	4
22	FP2[7]	FP2[6]	FP2[5]	FP2[4]	FP2[3]	FP2[2]	FP2[1]	FP2[0]	0	0	0	0	0	0	0	0	C3	5	–
23	0	SDT[2]	SDT[1]	SDT[0]	0	NOW[2]	NOW[1]	NOW[0]	0	0	0	0	0	MCP[2]	MCP[1]	MCP[0]	C4	1	2
24	VEQW[3]	VEQW[2]	VEQW[1]	VEQW[0]	0	0	VEM[1]	VEM[0]	0	0	0	0	SPCW[3]	SPCW[2]	SPCW[1]	SPCW[0]	C4	3	4
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4	5	–
26	0	0	0	PROPO0[4]	PROPO0[3]	PROPO0[2]	PROPO0[1]	PROPO0[0]	0	0	0	PROPO1[4]	PROPO1[3]	PROPO1[2]	PROPO1[1]	PROPO1[0]	C8	1	2
27	0	0	0	PROPO2[4]	PROPO2[3]	PROPO2[2]	PROPO2[1]	PROPO2[0]	PROPO4[3]	PROPO4[2]	PROPO4[1]	PROPO4[0]	PROPO3[3]	PROPO3[2]	PROPO3[1]	PROPO3[0]	C8	3	4
28	0	0	0	0	PROPO5[3]	PROPO5[2]	PROPO5[1]	PROPO5[0]	0	0	0	PROPO6[4]	PROPO6[3]	PROPO6[2]	PROPO6[1]	PROPO6[0]	C8	5	6
29	0	0	0	PROPO7[4]	PROPO7[3]	PROPO7[2]	PROPO7[1]	PROPO7[0]	0	0	0	PROPO8[4]	PROPO8[3]	PROPO8[2]	PROPO8[1]	PROPO8[0]	C8	7	8
30	0	0	PIROP1[1]	PIROP1[0]	0	0	PIROP0[1]	PIROP0[0]	0	0	PIROP3[1]	PIROP3[0]	0	0	PIROP2[1]	PIROP2[0]	C8	9	10
31	0	0	0	PRONO0[4]	PRONO0[3]	PRONO0[2]	PRONO0[1]	PRONO0[0]	0	0	0	PRONO1[4]	PRONO1[3]	PRONO1[2]	PRONO1[1]	PRONO1[0]	C8	11	12
32	0	0	0	PRONO2[4]	PRONO2[3]	PRONO2[2]	PRONO2[1]	PRONO2[0]	PRONO4[3]	PRONO4[2]	PRONO4[1]	PRONO4[0]	PRONO3[3]	PRONO3[2]	PRONO3[1]	PRONO3[0]	C8	13	14
33	0	0	0	0	PRONO5[3]	PRONO5[2]	PRONO5[1]	PRONO5[0]	0	0	0	PRONO6[4]	PRONO6[3]	PRONO6[2]	PRONO6[1]	PRONO6[0]	C8	15	16
34	0	0	0	PRONO7[4]	PRONO7[3]	PRONO7[2]	PRONO7[1]	PRONO7[0]	0	0	0	PRONO8[4]	PRONO8[3]	PRONO8[2]	PRONO8[1]	PRONO8[0]	C8	17	18
35	0	0	PIRON1[1]	PIRON1[0]	0	0	PIRON0[1]	PIRON0[0]	0	0	PIRON3[1]	PIRON3[0]	0	0	PIRON2[1]	PIRON2[0]	C8	19	20
36	0	0	0	PR1PO0[4]	PR1PO0[3]	PR1PO0[2]	PR1PO0[1]	PR1PO0[0]	0	0	0	PR1PO1[4]	PR1PO1[3]	PR1PO1[2]	PR1PO1[1]	PR1PO1[0]	C9	1	2
37	0	0	0	PR1PO2[4]	PR1PO2[3]	PR1PO2[2]	PR1PO2[1]	PR1PO2[0]	PR1PO4[3]	PR1PO4[2]	PR1PO4[1]	PR1PO4[0]	PR1PO3[3]	PR1PO3[2]	PR1PO3[1]	PR1PO3[0]	C9	3	4
38	0	0	0	0	PR1PO5[3]	PR1PO5[2]	PR1PO5[1]	PR1PO5[0]	0	0	0	PR1PO6[4]	PR1PO6[3]	PR1PO6[2]	PR1PO6[1]	PR1PO6[0]	C9	5	6
39	0	0	0	PR1PO7[4]	PR1PO7[3]	PR1PO7[2]	PR1PO7[1]	PR1PO7[0]	0	0	0	PR1PO8[4]	PR1PO8[3]	PR1PO8[2]	PR1PO8[1]	PR1PO8[0]	C9	7	8
40	0	0	PIR1P1[1]	PIR1P1[0]	0	0	PIR1PO[1]	PIR1PO[0]	0	0	PIR1P3[1]	PIR1P3[0]	0	0	PIR1P2[1]	PIR1P2[0]	C9	9	10
41	0	0	0	PR1NO0[4]	PR1NO0[3]	PR1NO0[2]	PR1NO0[1]	PR1NO0[0]	0	0	0	PR1NO1[4]	PR1NO1[3]	PR1NO1[2]	PR1NO1[1]	PR1NO1[0]	C9	11	12
42	0	0	0	PR1NO2[4]	PR1NO2[3]	PR1NO2[2]	PR1NO2[1]	PR1NO2[0]	PR1NO4[3]	PR1NO4[2]	PR1NO4[1]	PR1NO4[0]	PR1NO3[3]	PR1NO3[2]	PR1NO3[1]	PR1NO3[0]	C9	13	14
43	0	0	0	0	PR1NO5[3]	PR1NO5[2]	PR1NO5[1]	PR1NO5[0]	0	0	0	PR1NO6[4]	PR1NO6[3]	PR1NO6[2]	PR1NO6[1]	PR1NO6[0]	C9	15	16
44	0	0	0	PR1NO7[4]	PR1NO7[3]	PR1NO7[2]	PR1NO7[1]	PR1NO7[0]	0	0	0	PR1NO8[4]	PR1NO8[3]	PR1NO8[2]	PR1NO8[1]	PR1NO8[0]	C9	17	18
45	0	0	PIR1N1[1]	PIR1N1[0]	0	0	PIR1NO[1]	PIR1NO[0]	0	0	PIR1N3[1]	PIR1N3[0]	0	0	PIR1N2[1]	PIR1N2[0]	C9	19	20
46	0	0	0	PR2PO0[4]	PR2PO0[3]	PR2PO0[2]	PR2PO0[1]	PR2PO0[0]	0	0	0	PR2PO1[4]	PR2PO1[3]	PR2PO1[2]	PR2PO1[1]	PR2PO1[0]	CA	1	2
47	0	0	0	PR2PO2[4]	PR2PO2[3]	PR2PO2[2]	PR2PO2[1]	PR2PO2[0]	PR2PO4[3]	PR2PO4[2]	PR2PO4[1]	PR2PO4[0]	PR2PO3[3]	PR2PO3[2]	PR2PO3[1]	PR2PO3[0]	CA	3	4
48	0	0	0	0	PR2PO5[3]	PR2PO5[2]	PR2PO5[1]	PR2PO5[0]	0	0	0	PR2PO6[4]	PR2PO6[3]	PR2PO6[2]	PR2PO6[1]	PR2PO6[0]	CA	5	6
49	0	0	0	PR2PO7[4]	PR2PO7[3]	PR2PO7[2]	PR2PO7[1]	PR2PO7[0]	0	0	0	PR2PO8[4]	PR2PO8[3]	PR2PO8[2]	PR2PO8[1]	PR2PO8[0]	CA	7	8
50	0	0	PIR2P1[1]	PIR2P1[0]	0	0	PIR2PO[1]	PIR2PO[0]	0	0	PIR2P3[1]	PIR2P3[0]	0	0	PIR2P2[1]	PIR2P2[0]	CA	9	10
51	0	0	0	PR2NO0[4]	PR2NO0[3]	PR2NO0[2]	PR2NO0[1]	PR2NO0[0]	0	0	0	PR2NO1[4]	PR2NO1[3]	PR2NO1[2]	PR2NO1[1]	PR2NO1[0]	CA	11	12
52	0	0	0	PR2NO2[4]	PR2NO2[3]	PR2NO2[2]	PR2NO2[1]	PR2NO2[0]	PR2NO4[3]	PR2NO4[2]	PR2NO4[1]	PR2NO4[0]	PR2NO3[3]	PR2NO3[2]	PR2NO3[1]	PR2NO3[0]	CA	13	14
53	0	0	0	0	PR2NO5[3]	PR2NO5[2]	PR2NO5[1]	PR2NO5[0]	0	0	0	PR2NO6[4]	PR2NO6[3]	PR2NO6[2]	PR2NO6[1]	PR2NO6[0]	CA	15	16
54	0	0	0	PR2NO7[4]	PR2NO7[3]	PR2NO7[2]	PR2NO7[1]	PR2NO7[0]	0	0	0	PR2NO8[4]	PR2NO8[3]	PR2NO8[2]	PR2NO8[1]	PR2NO8[0]	CA	17	18
55	0	0	PIR2N1[1]	PIR2N1[0]	0	0	PIR2NO[1]	PIR2NO[0]	0	0	PIR2N3[1]	PIR2N3[0]	0	0	PIR2N2[1]	PIR2N2[0]	CA	19	20
56	0	0	0	0	0	VC[2]	VC[1]	VC[0]	1	1	0	0	0	BT[2]	BT[1]	BT[0]	D0	1	2
57	1	0	0	VRH[4]	VRH[3]	VRH[2]	VRH[1]	VRH[0]	0	0	1	1	0	0	1	0	D0	3	4
58	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	D0	5	6
59	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D0	7	–
60	0	VCM[6]	VCM[5]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]	0	0	0	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	D1	1	2
61	0	0	0	0	0	0	VCMR	SELVCM	0	0	0	0	0	0	0	0	D1	3	–
62	0	0	0	0	0	0	APO[1]	APO[0]	0	DC10[2]	DC10[1]	DC10[0]	0	DC00[2]	DC00[1]	DC00[0]	D2	1	2
63	0	0	0	0	0	0	AP1[1]	AP1[0]	0	DC11[2]	DC11[1]	DC11[0]	0	DC01[2]	DC01[1]	DC01[0]	D3	1	2
64	0	0	0	0	0	0	AP2[1]	AP2[0]	0	DC12[2]	DC12[1]	DC12[0]	0	DC02[2]	DC02[1]	DC02[0]	D4	1	2
65	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	D6	1	2
66	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	D6	3	–
67	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	D7	1	2
68	1	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	D7	3	4
69	1	0	1	0	1	0	1	0	0	0	0	0	1	0	1	0	D7	5	6
70	1	1	0	0	1	0	1	0	0	0	0	0	1	1	0	0	D7	7	8
71	0	1	1	1	0	1	0	1	0	1	1	1	0	1	0	1	D8	1	2
72	0	0	1	1	0	0	1	1	0	1	1	1	0	1	0	1	D8	3	4
73	0	0	0	1	0	0	0	1	1	0	0	1	0	0	0	1	D8	5	6
74	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	D8	7	8
75	1	1	1	1	1	0	1	1	0	0	0	1	1	1	1	1	D9	1	2
76	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	F4	1	–
77	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FC	1	2
78	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FC	3	4
79	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FC	5	6
80	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FC	7	8
81	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FC	9	–
82	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FD	1	2
83	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	FD	3	4
84	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FD	5	6
85	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FE	1	2
86	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	FE	3	4

Frame Memory

Arrangement

The frame memory stores display pixels and consists of 1,382,400 bits (320 x 240 x 18 bits).

Address Mapping from Memory to Display

Normal Display On or Partial Mode On, Vertical Scroll OFF

In this mode, contents of the frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.

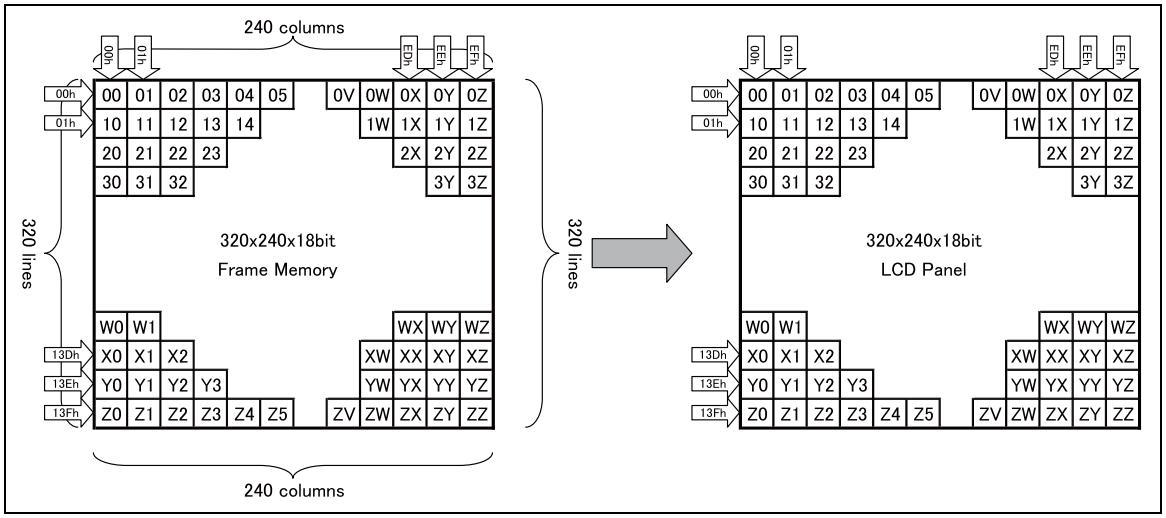


Figure 34

Vertical Scroll Mode

There is a vertical scrolling mode, which are determined by the commands “set_scroll_area (33h)” and “set_scroll_start (37h)”.

Example 1: TFA = 2, VSA = 318, BFA = 0 when set_address_mode (36h) B4 = 0, VSP = 3

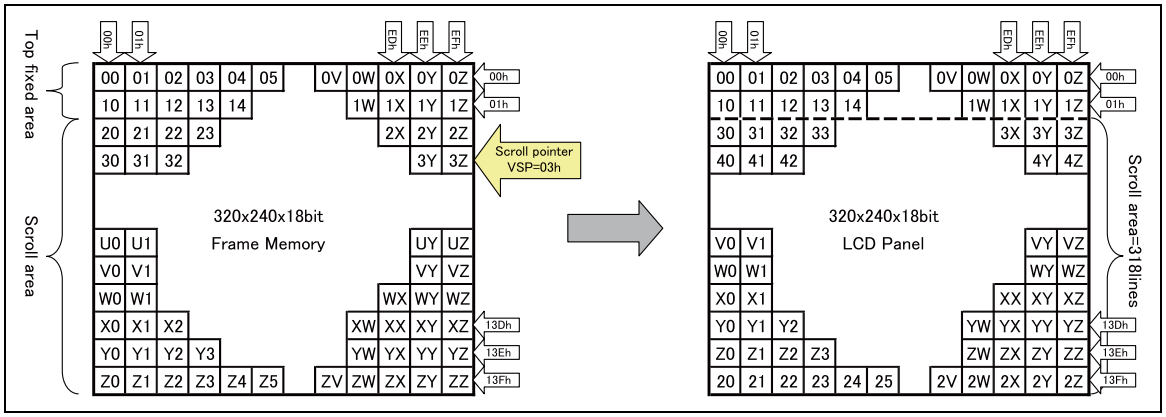


Figure 35

Example 2: TFA = 2, VSA = 316, BFA = 2 when set_address_mode (36h) B4 = 0, VSP = 3

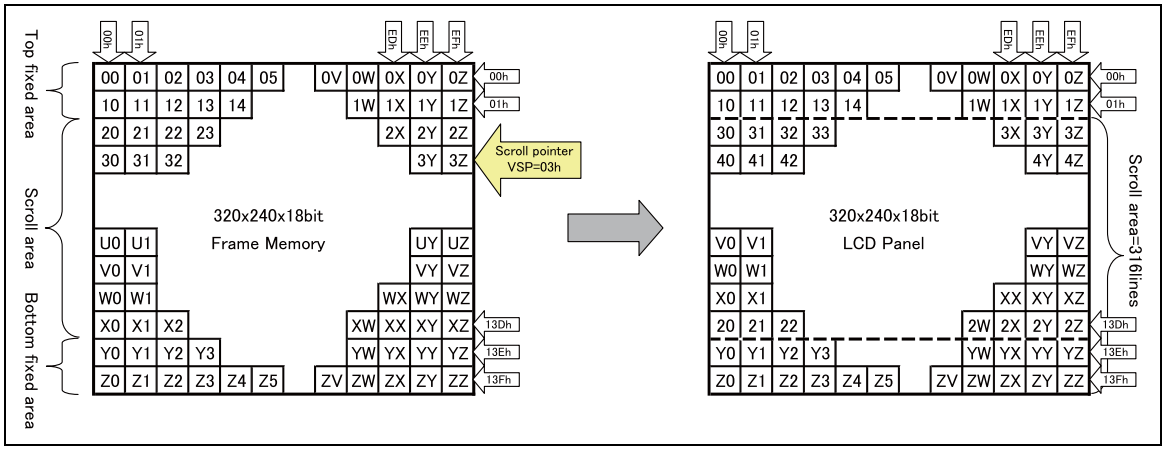


Figure 36

Example 3: TFA = 2, VSA = 316, BFA = 2 when set_address_mode (36h) B4 = 0, VSP = 5

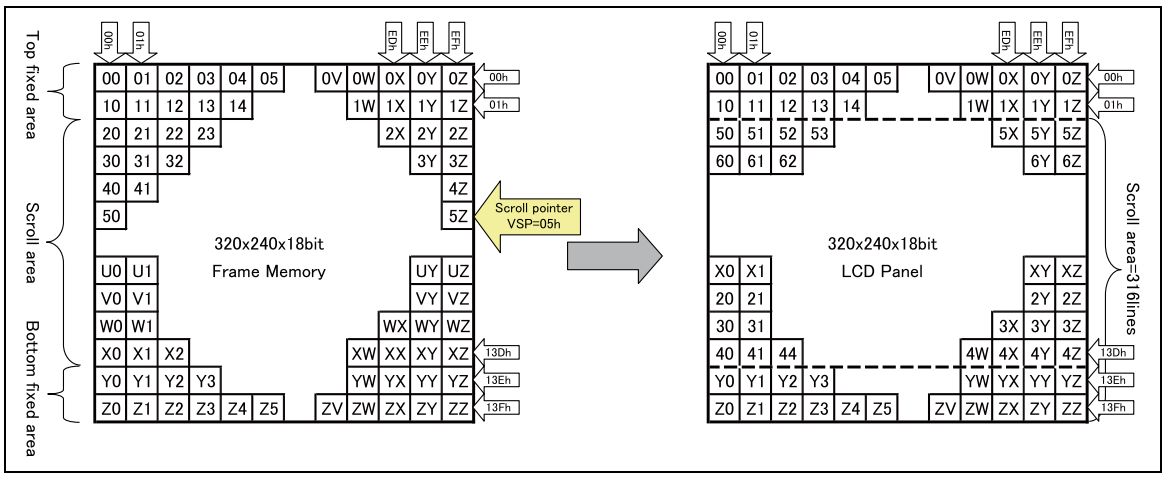


Figure 37

Vertical Scroll Example

Case 1: TFA+VSA+BFA≠320

If such an setting is made, the command will be accepted but an undesirable image will be displayed.

Case 2: TFA+VSA+BFA = 320 (Rolling scrolling)

Example 2-a: when TFA = 0, VSA = 320, BFA = 0 and VSP = 40
(set_address_mode (36h) B4=1)

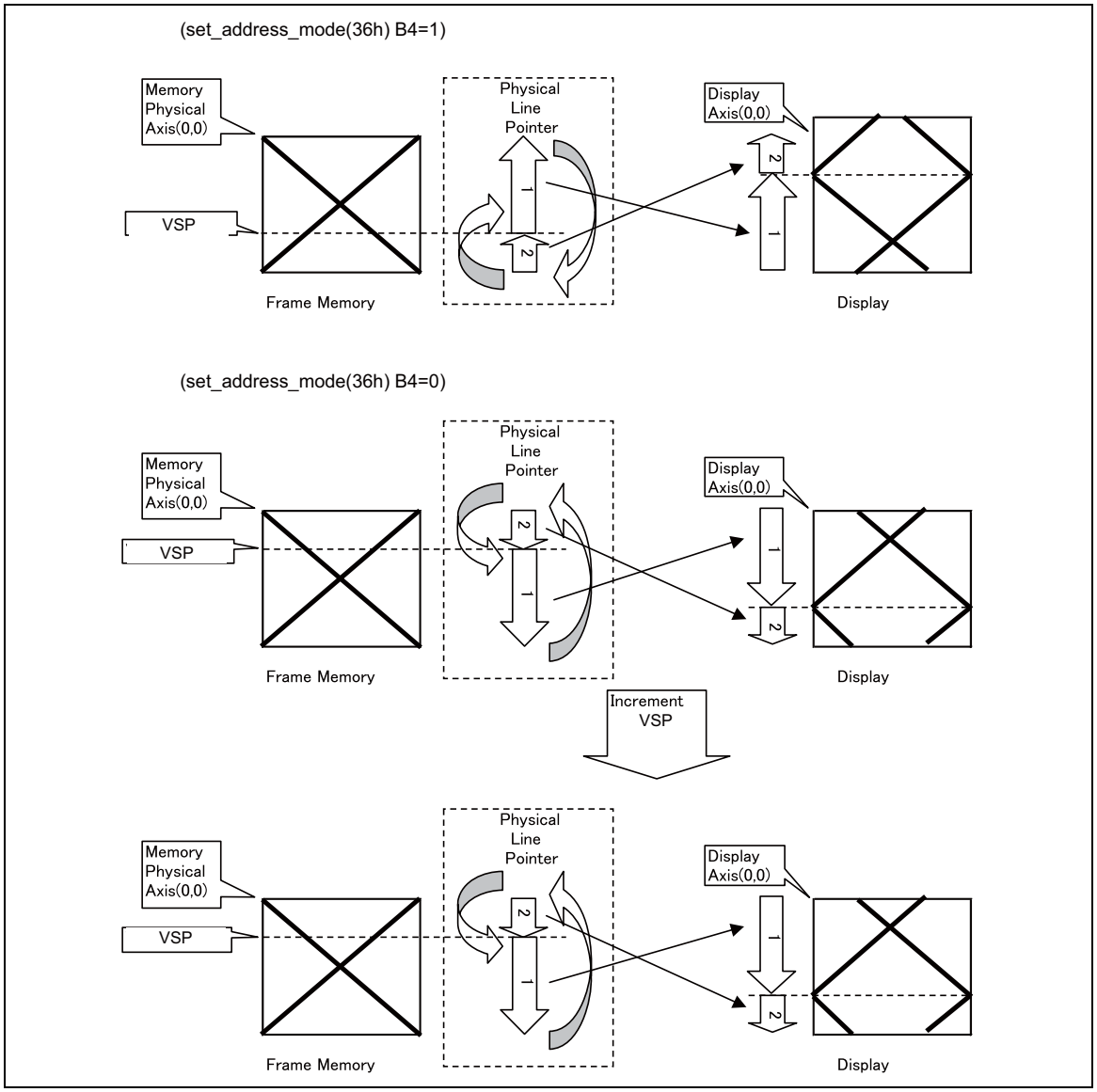


Figure 38

Example 2-b: when TFA = 30, VSA = 210, BFA = 0 and VSP = 80
(set_address_mode (36h) B4=0)

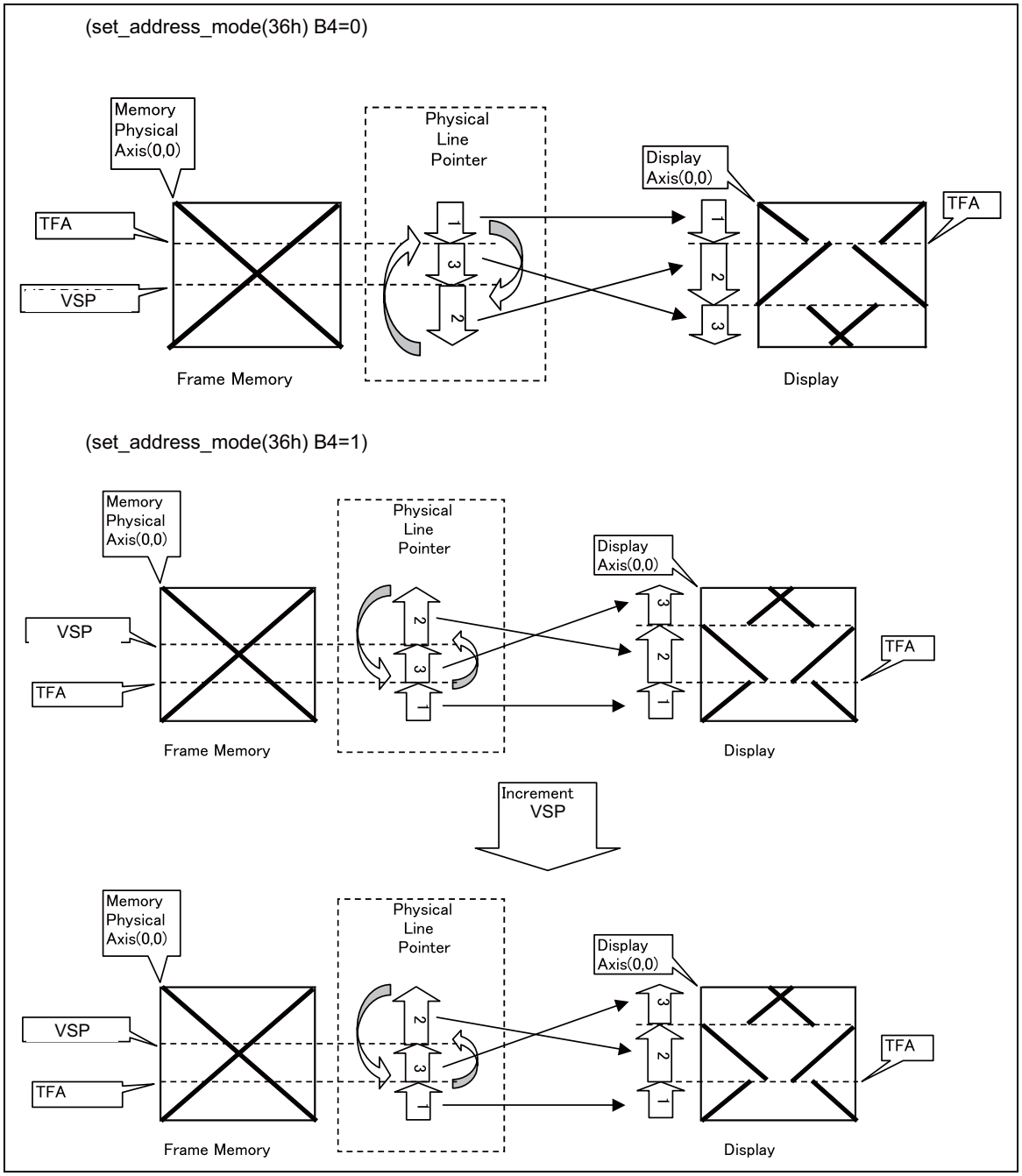


Figure 39

Host Processor to Memory Write/Read Direction

The data stream from host processor is as follows.

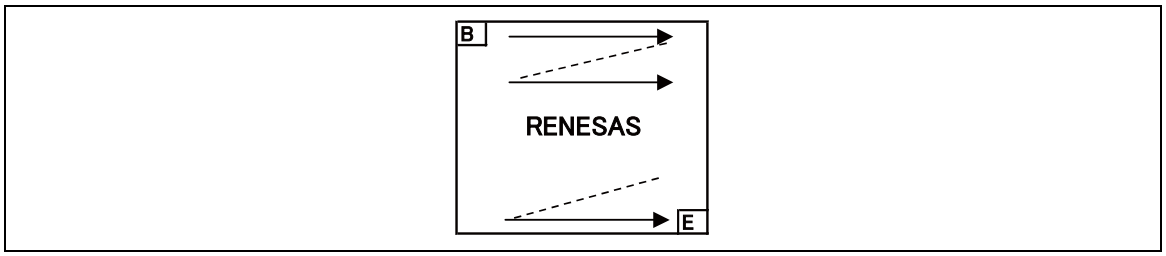


Figure 40

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "set_address_mode (36h)" command Bits B5, B6, B7 as described below.

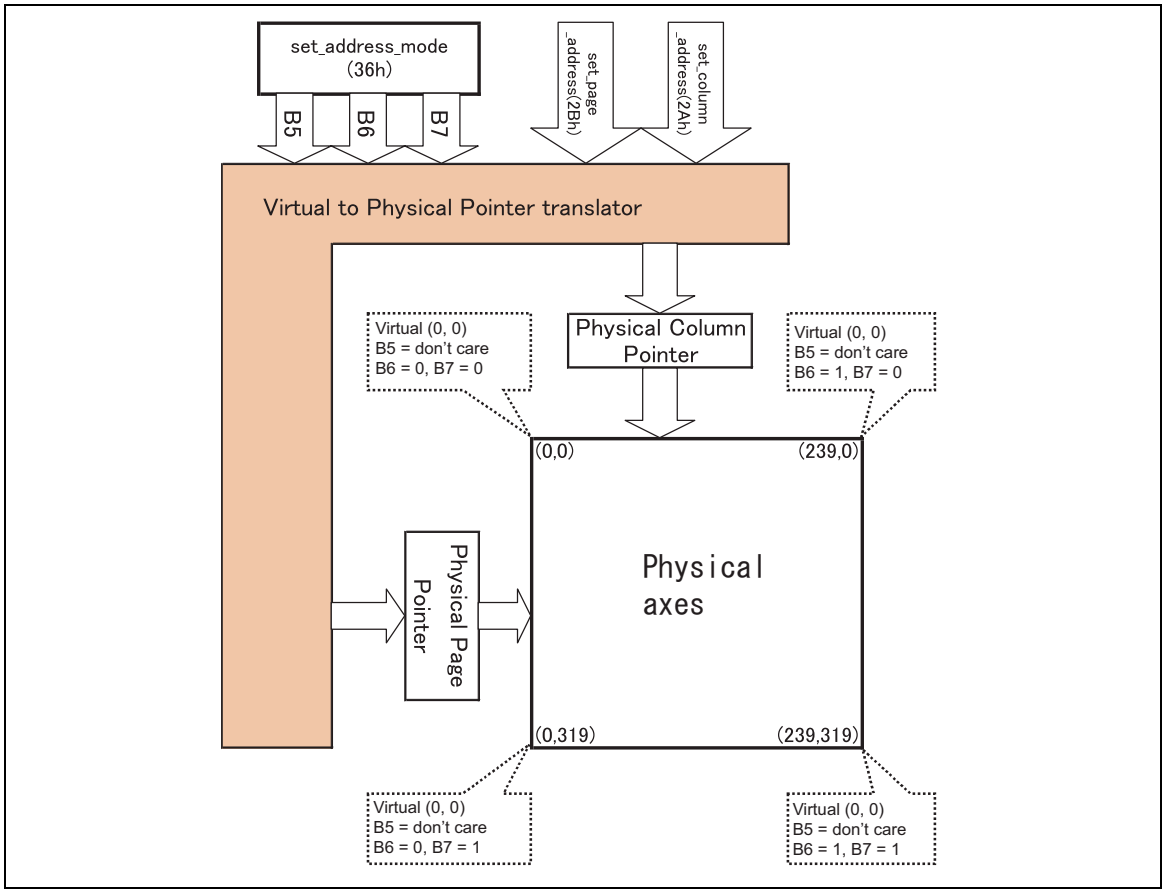


Figure 41

Table 23 set_address_mode Command

D5	D6	D7	Column Address	Page Address
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

For each image orientation, the controls on the column and page counters apply as below.

Table 24

Condition	Column Counter	Page Counter	Notes
When write_memory_start (2Ch)/read_memory_start (2Eh) command is accepted.	Return to "Start Column"	Return to "Start Page"	
Complete Pixel Read/Write action	Increment by 1	No change	
The Column counter value is larger than that of "End column."	Return to Start Column"	Increment by 1	
The Column counter value is larger than that of "End column" and the Page counter value is larger than that of "End page".	Stop	Stop	Entry Mode (B3h) WEMODE = 0
	Return to "Start Column"	Return to "Start Page"	Entry Mode (B3h) WEMODE = 1

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by set_address_mode (36h) bits B7, B6 and B5. The write order for each pixel unit is as follows.

Table 25

D 17	D 16	D 15	D 14	D 13	D 12	D 11	D 10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory. See the next page for the resultant image for each orientation setting.

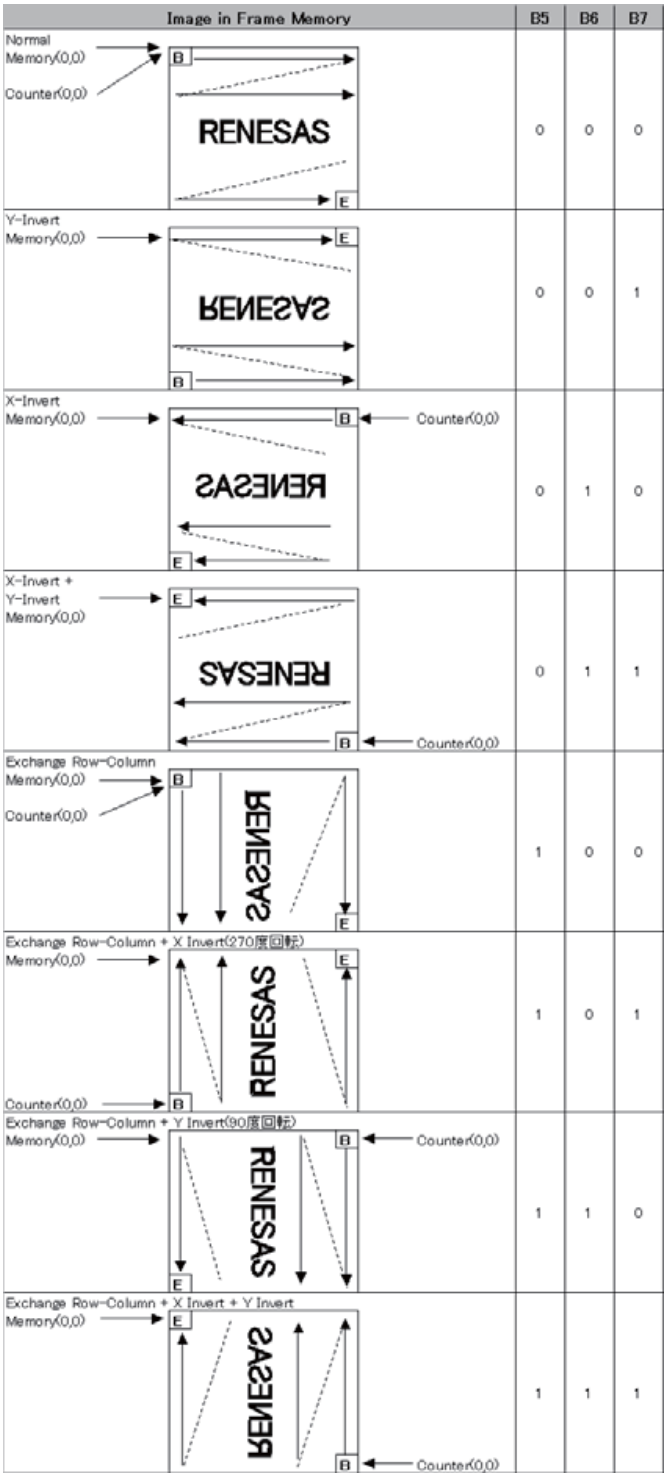


Image in Frame Memory
B5
B6
B7
Normal
Memory(0,0)
Counter(0,0)
RENESAS
0 0 0
Y-Invert
Memory(0,0)
0 0 1
X-Invert
Memory(0,0)
Counter(0,0)
0 1 0
X-Invert +
Y-Invert
Memory(0,0)
Counter(0,0)
0 1 1
Exchange Row-Column
Memory(0,0)
Counter(0,0)
1 0 0
Exchange Row-Column + X Invert(270度回転)
Memory(0,0)
Counter(0,0)
1 0 1
Exchange Row-Column + Y Invert(90度回転)
Memory(0,0)
Counter(0,0)
1 1 0
Exchange Row-Column + X Invert + Y Invert
Memory(0,0)
Counter(0,0)
1 1 1

Figure 42

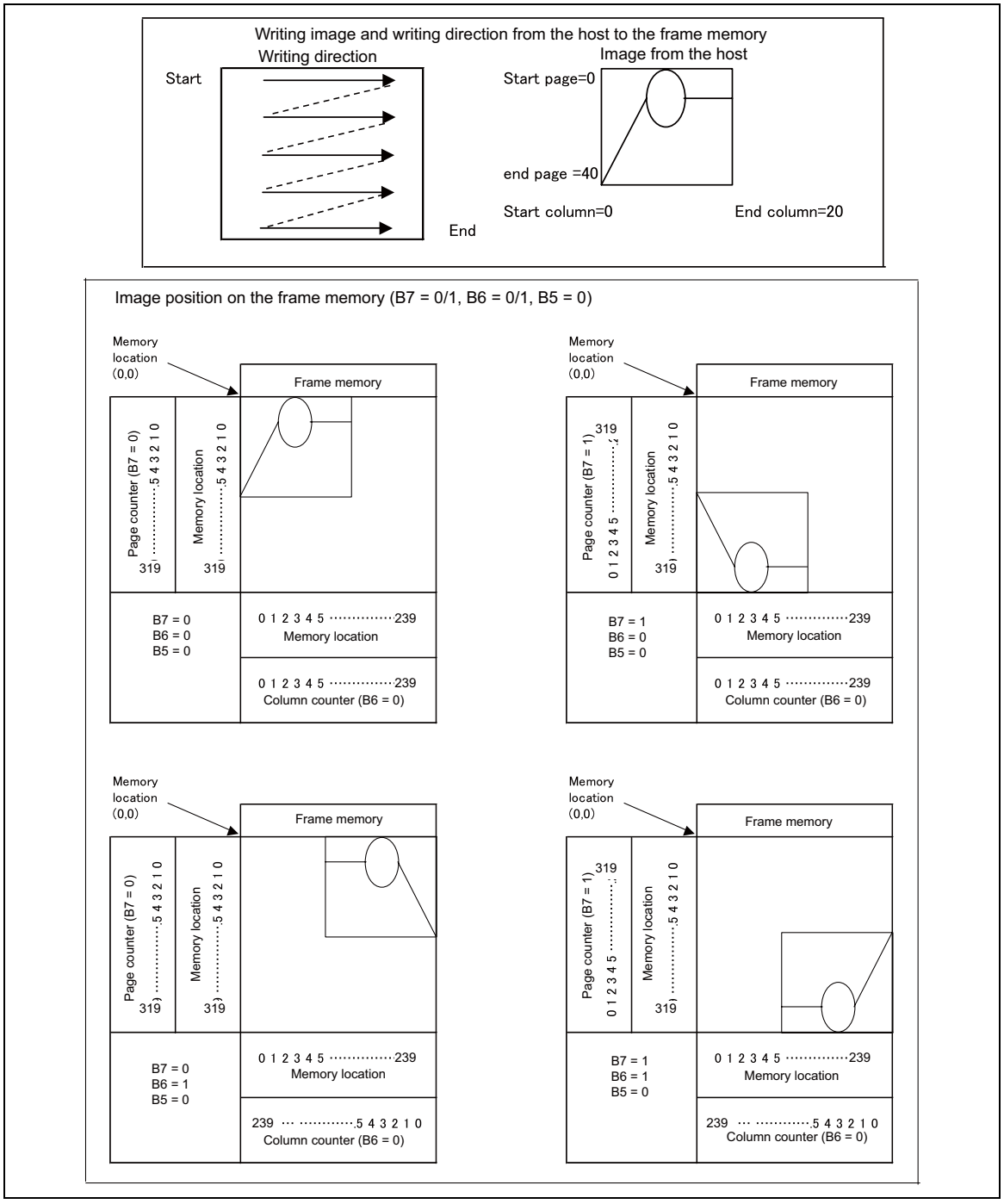

Writing image and writing direction from the host to the frame memory
Writing direction
Image from the host
Start
Start page=0
end page =40
Start column=0
End column=20
End
Image position on the frame memory (B7 = 0/1, B6 = 0/1, B5 = 0)
Memory location (0,0)
Frame memory
Page counter (B7 = 0)
Memory location
319
B7 = 0
B6 = 0
B5 = 0
0 1 2 3 4 5 ····· 239
Memory location
Column counter (B6 = 0)
Page counter (B7 = 1)
B7 = 1
B6 = 0
B5 = 0
B6 = 1
B5 = 1
239 ··· 5 4 3 2 1 0

Figure 43

When B5 =1

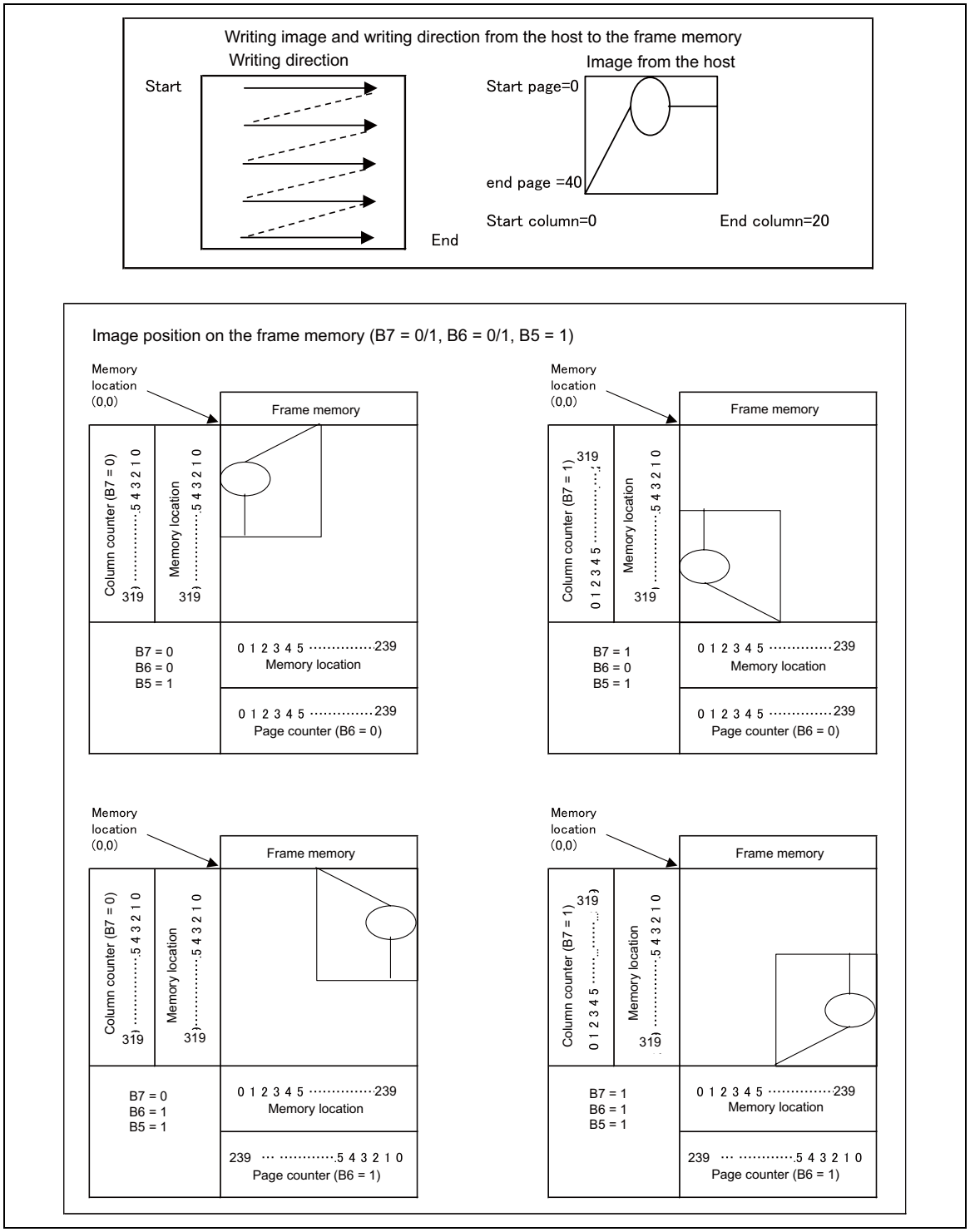


Figure 44

High Speed Frame Memory Write Function

The R61516 supports high-speed frame memory write function to write data to each line of window address area at a time. This function makes the R61516 available with the applications, which require high-speed, low-power-consumption data write operation such as color video image display.

When enabling high-speed frame memory write function (HWM = "1"), the data is first stored in the internal register of the R61516 in order to rewrite the frame memory data in each horizontal line of the window address area at a time. Also, when transferring the data from the internal register to the internal frame memory, the data written in the next line of the window address area can be transferred to the internal register of the R61516. The high-speed write function minimizes the number of frame memory access in write operation and enables high-speed consecutive frame memory write operation required for video image display with low power consumption.

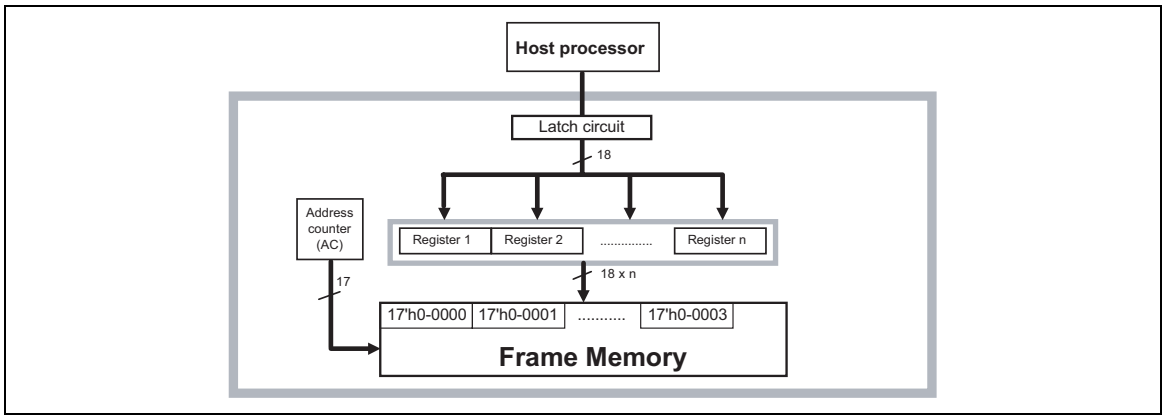


Figure 45 High-speed Consequtive Frame Memory Write Operation

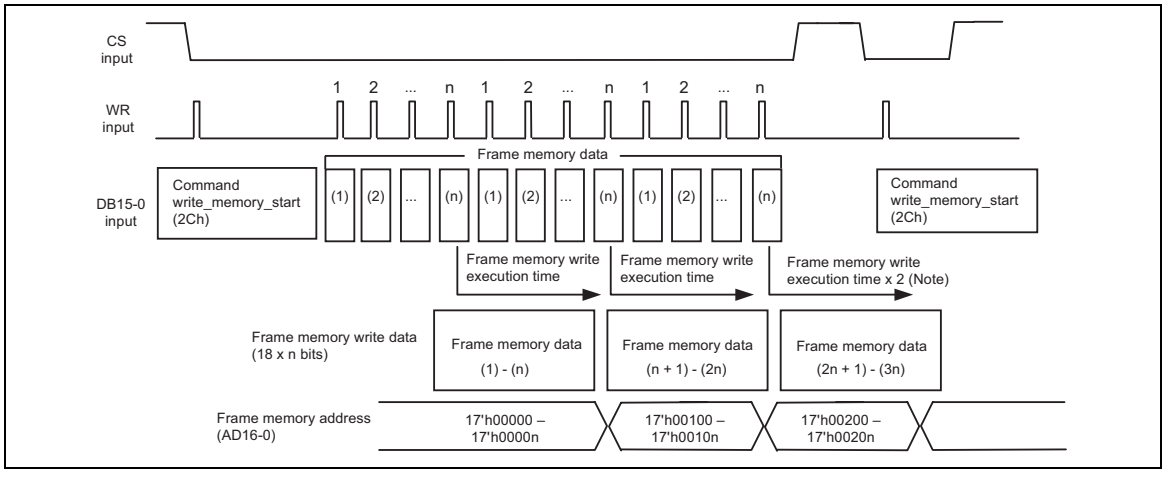


Figure 46 High-speed Frame Memory Write Operation Example (HWM = 1)

Note: When switching from high-speed frame memory write operation to index write operation, wait at least for two normal frame memory write bus cycle periods (2 x t_{cycw}) before executing next command.

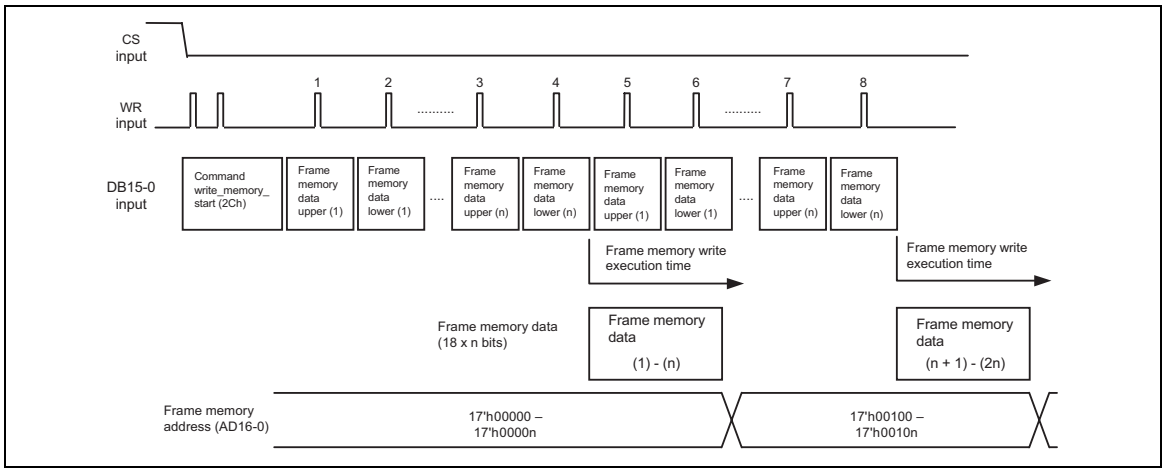


Figure 47

Note: In high-speed frame memory write operation, the R61516 writes data in units of 1word in 1 transfer operation, 2 words in 2 transfer opearation and 3 words in 3 transfer operation.

Notes to high-speed frame memory write function

1. In high-speed frame memory write mode, the R61516 performs write operation to the internal frame memory in units of lines. If the data inputted to the internal write register is not enough to rewrite the data in the horizontal line of the window address area, the data is not written correctly in that line address.

2. If the write_memory_start (2Ch) is selected, the R61516 always performs frame memory write operation. With this setting, the R61516 does not perform frame memory read operation. Make sure to set HWM = 0, when performing frame memory read operation.

3. The high-speed frame memory write function cannot be used when writing data in normal frame memory write function mode. When switching form one write mode to the other, change the mode before starting write operation.

Table 26

	Normal frame memory write operation (HWM="0")	**High-speed frame memory write operation (HWM="1")**
Address set set_column_address set_page_address	In units of words (Minimum: 1 word x 1 line)	In units of words (Minimum: 8 words x 1 line)
Frame memory read	In units of word	Not available
Frame memory write	In units of word	In units of line
DPI	Available	Available
set_address_mode (36h)	B5=1/0	B5=0

High-speed frame memory data write in a window address area

The R61516 performs consecutive high-speed data rewrite operation within a rectangular area (minimum: 8 words x 1 line) made in the internal frame memory with the following settings.

When writing data to the internal frame memory using high-speed frame memory write function, make sure each line of the window address area is overwritten at a time. If the data buffered in the internal register of the R61516 is not enough to overwrite the horizontal line in the window address area, the data is not written correctly in that line.

The following is an example of writing data in the window address area using high-speed frame memory write function when a window address area is made by setting SC=8'h12, EC=8'h30, SP=9'h008, EP=9'h046.

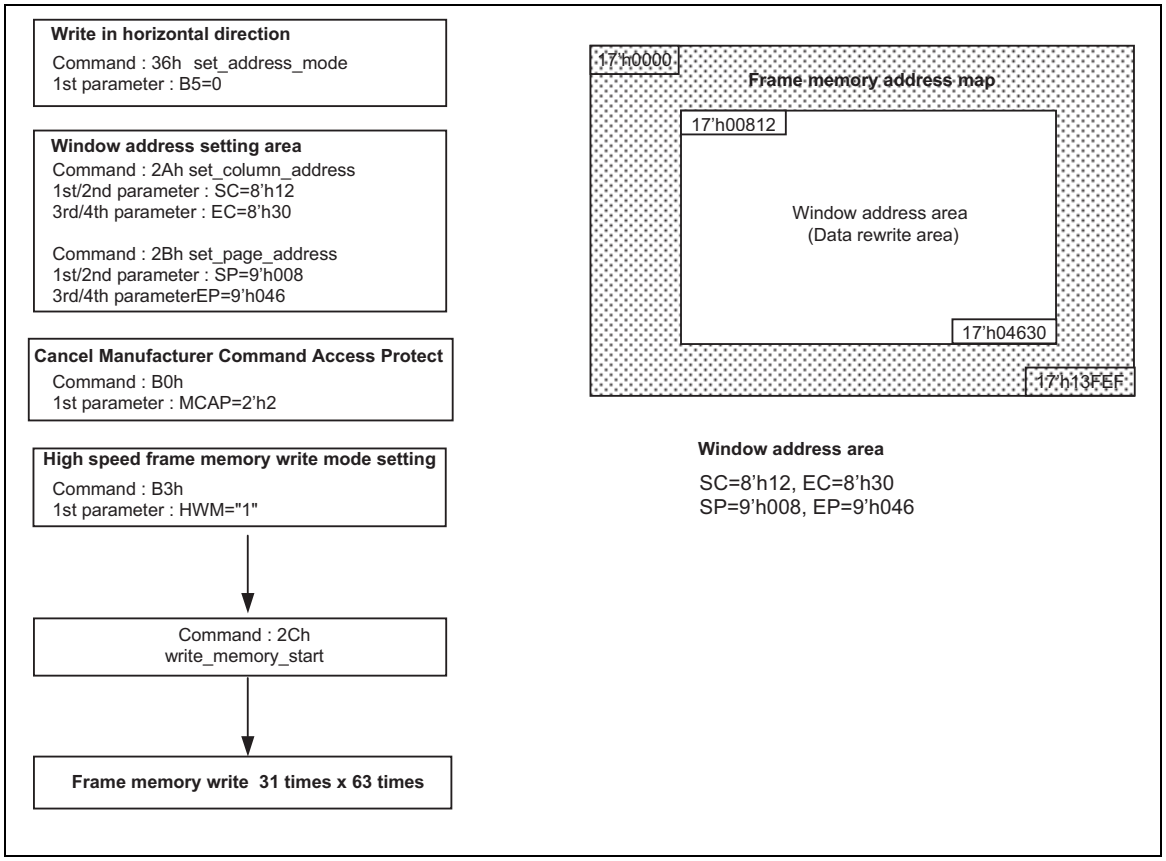


Figure 48

Self-diagnostic Functiuons

The R61516 supports the self-diagnostic functions. Set get_diagnostic_result (0Fh) 1st parameter's D7 and D6 bits as following flow chart.

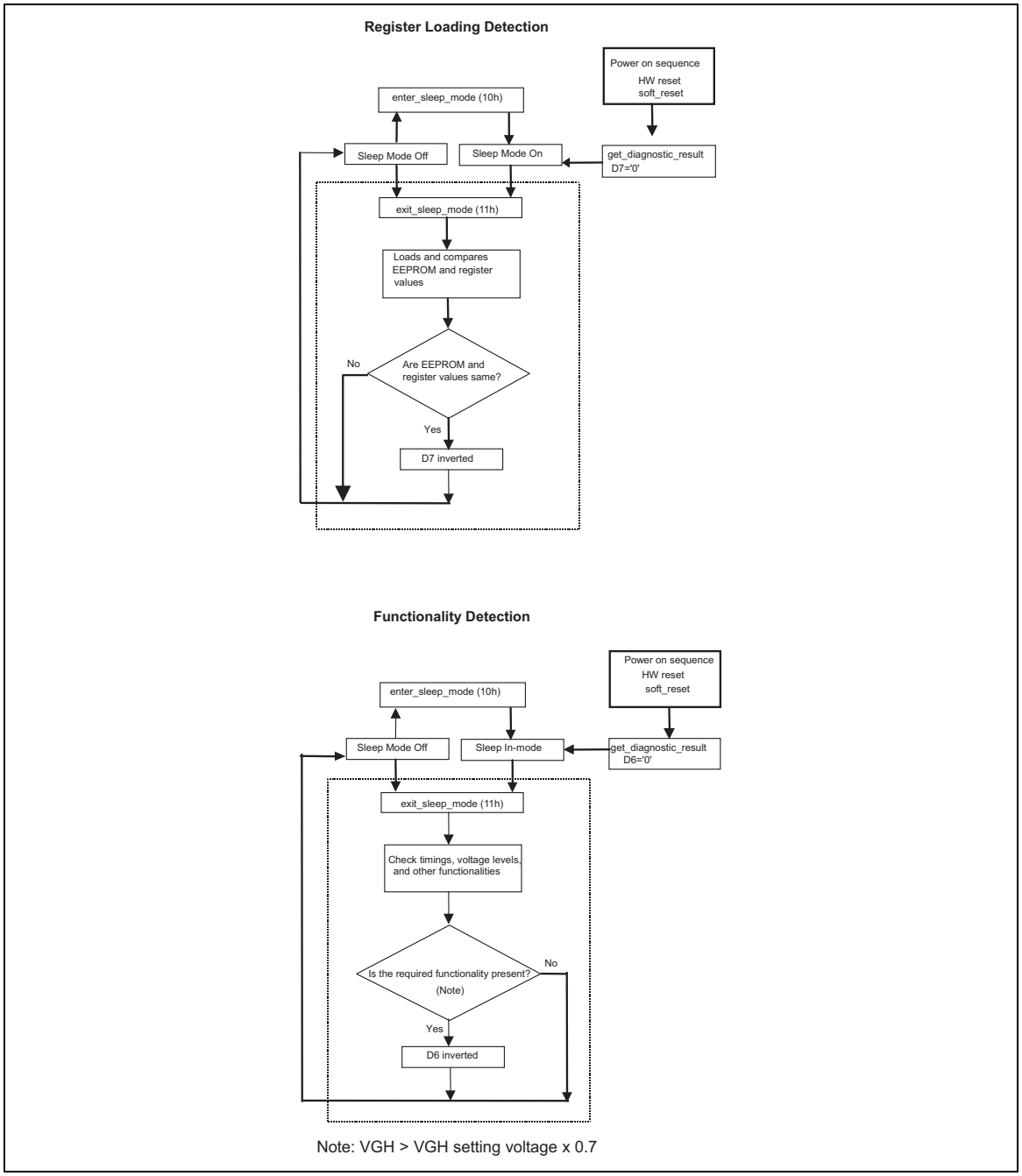


Figure 49

Register Loading Detection

The exit_sleep_mode command is a trigger for the Register Loading Detection function. This function indicates if the display module correctly loaded the factory default values from EEPROM to the registers. If the registers were loaded properly then bit D7 of the SDR register is inverted.

This function is enabled when external EEPROM is used (EEPROME=VCC).

Functionality Detection

The exit_sleep_mode command is a trigger for the Functionality Detecction function. If VGH level is VGH setting value x 0.7 or greater, the step-up circuit is regarded as operating properly, then bit D6 of the SDR register is inverted.

Scan Mode Setting

The relationship among driver arrangement, GS, SM, SS and BGR register settings and the Frame Memory Address (1)

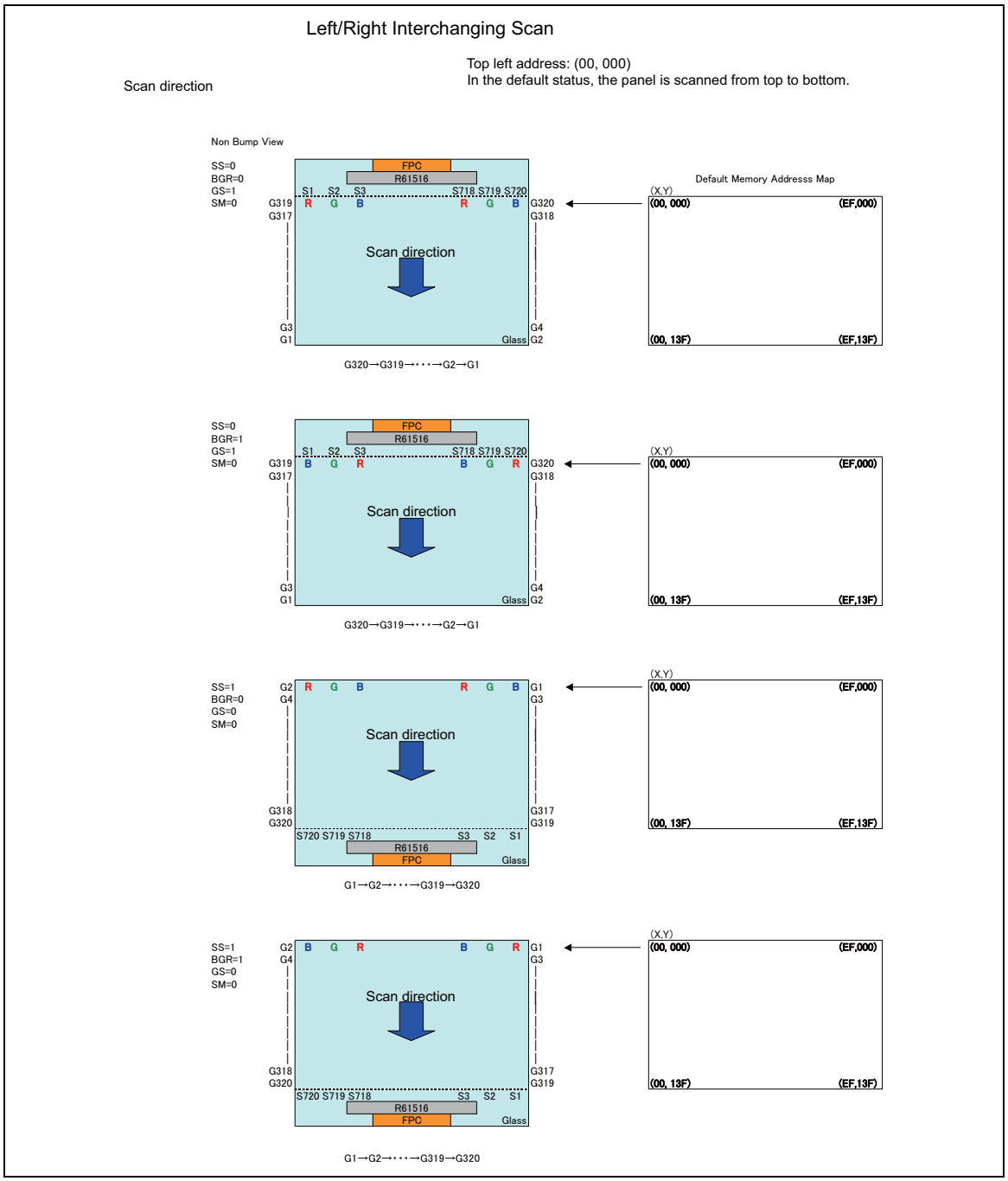


Figure 50

The relationship among driver arrangement, GS, SM, SS and BGR register settings and the Frame Memory Address (2)

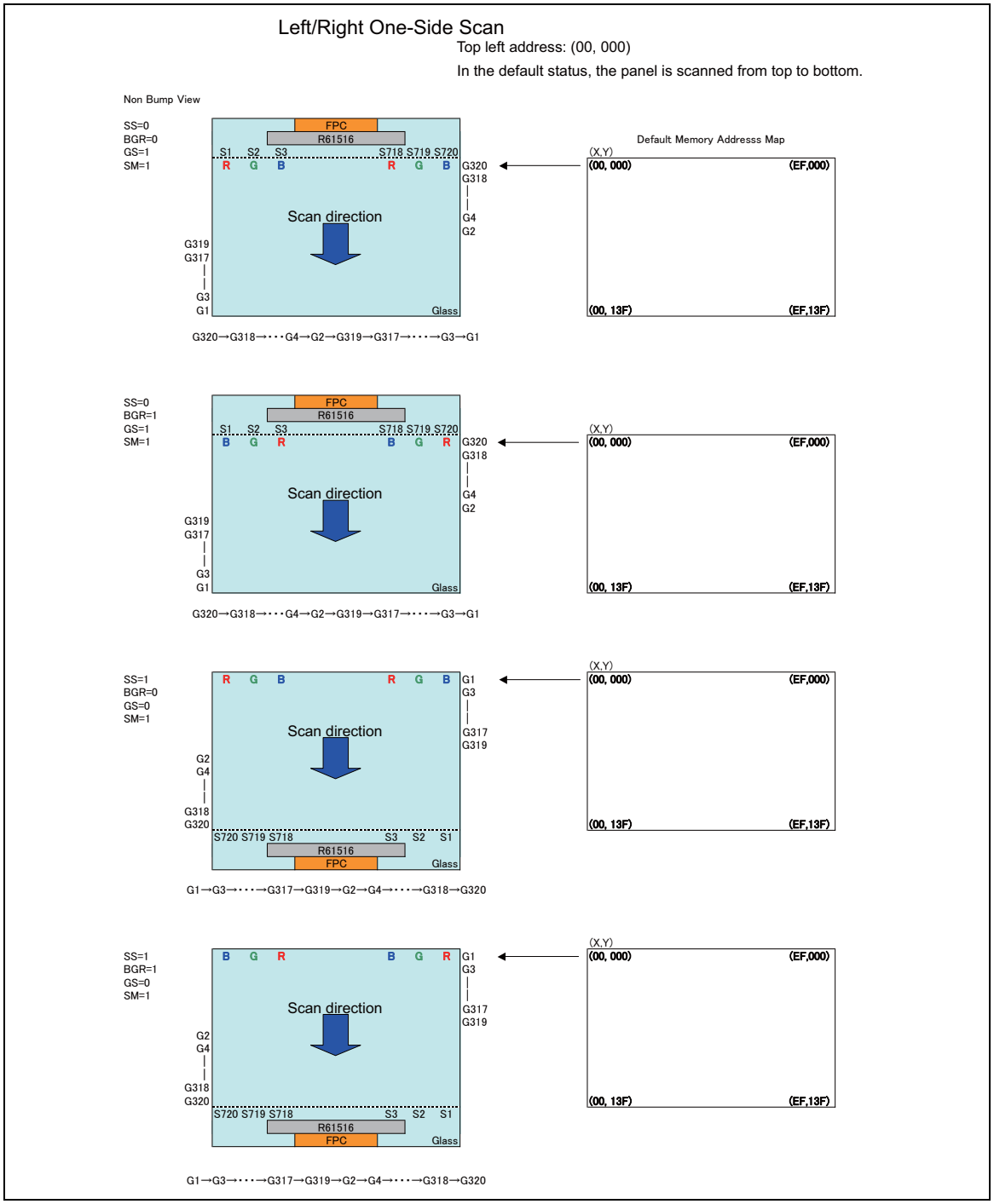


Figure 51

Frame-Frequency Adjustment Function

The R61516 supports a function to adjust frame frequency. The frame frequency for driving the LCD can be adjusted by setting Display Timing Setting (C1h-C2h, DIV and RTN bits) without changing the oscillation frequency.

It is possible to set a low frame frequency for saving power consumption when displaying a still picture and set a high frame frequency when displaying video image.

Also, the R61516 has frame-frequency adjustment parameters which can set frame frequency according to display modes (normal mode, partial mode, and idle mode).

Relationship between the Liquid Crystal Drive Duty and the Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following equation. The frame frequency can be changed by setting 1H period setting (RTN) bit and operating clock frequency division ratio setting (DIV) bit.

Equation for calculating frame frequency

$$FrameFrequency = \frac{fosc}{NumberofClocks/line \times DivisionRatio \times (NL + FP + BP)} [Hz]$$

fosc: Internal operation clock frequency
Number of clocks per line: RTN bit
Division ratio: DIV bit
Line: number of lines to drive the LCD (NL bit)
Number of lines for front porch: FP
Number of lines for back porch: BP

Example of Calculation: when Maximum Frame Frequency = 60 Hz

fosc : 678 kHz
Number of lines: 320 lines
1H period: 17 clock cycles (RTN[4:0] = “10001”)
Division ratio of operating clock: 1/2
Front porch: 8 lines
Back porch: 8 lines

$$\therefore f_{FLM} = \frac{678kHz}{17clocks \times \frac{1}{2} \times (320 + 8 + 8)} \approx 60Hz$$

In the conditions described here, the frame frequency can be changed as follows by setting RTN and DIV. (NL=320line, BP=8line, FP=8line, fosc=678kHz).

Line Inversion AC Drive

The R61516, in addition to frame-inversion liquid crystal alternating current drive, supports line inversion alternating current drive.

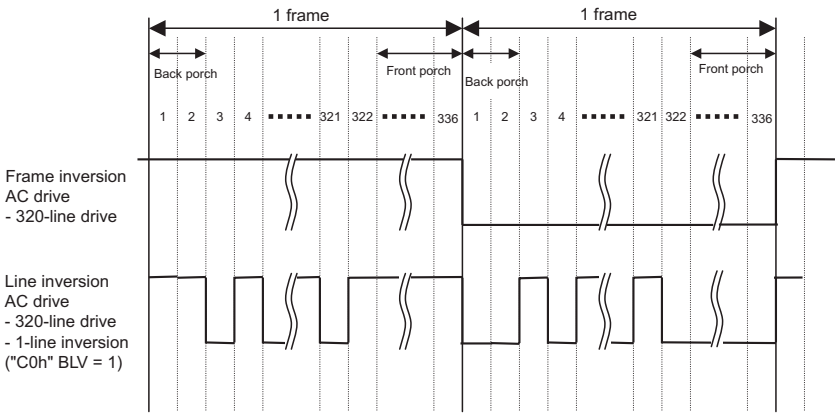


Figure 52 Liquid Crystal Inversion Drive Waveform

Alternating Timing

The following figure illustrates the liquid-crystal polarity inversion timing of different LCD driving methods.

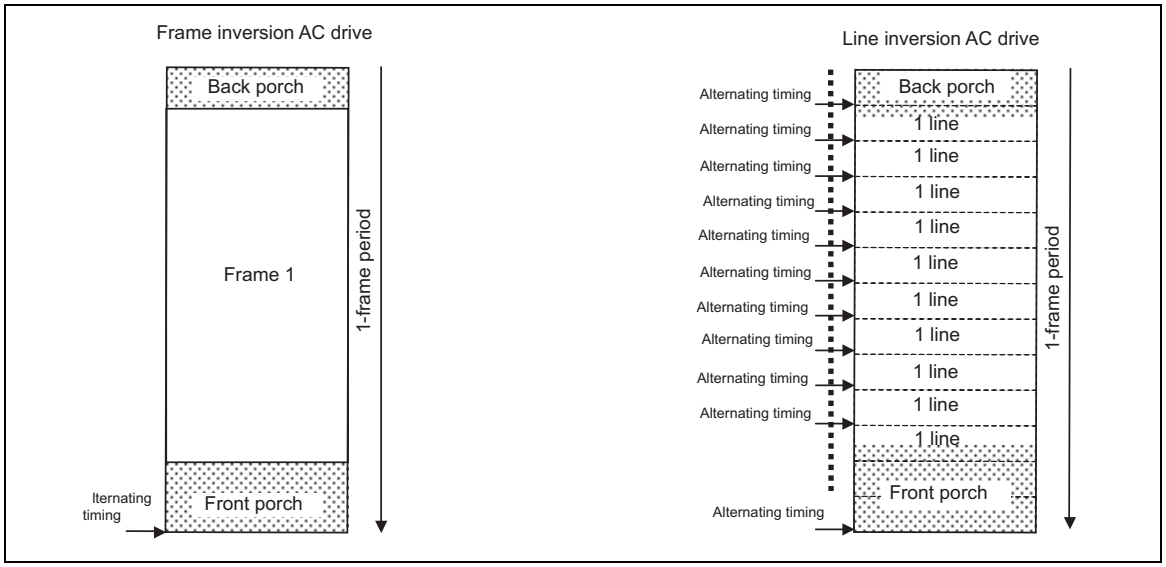


Figure 53 Alternating Timing

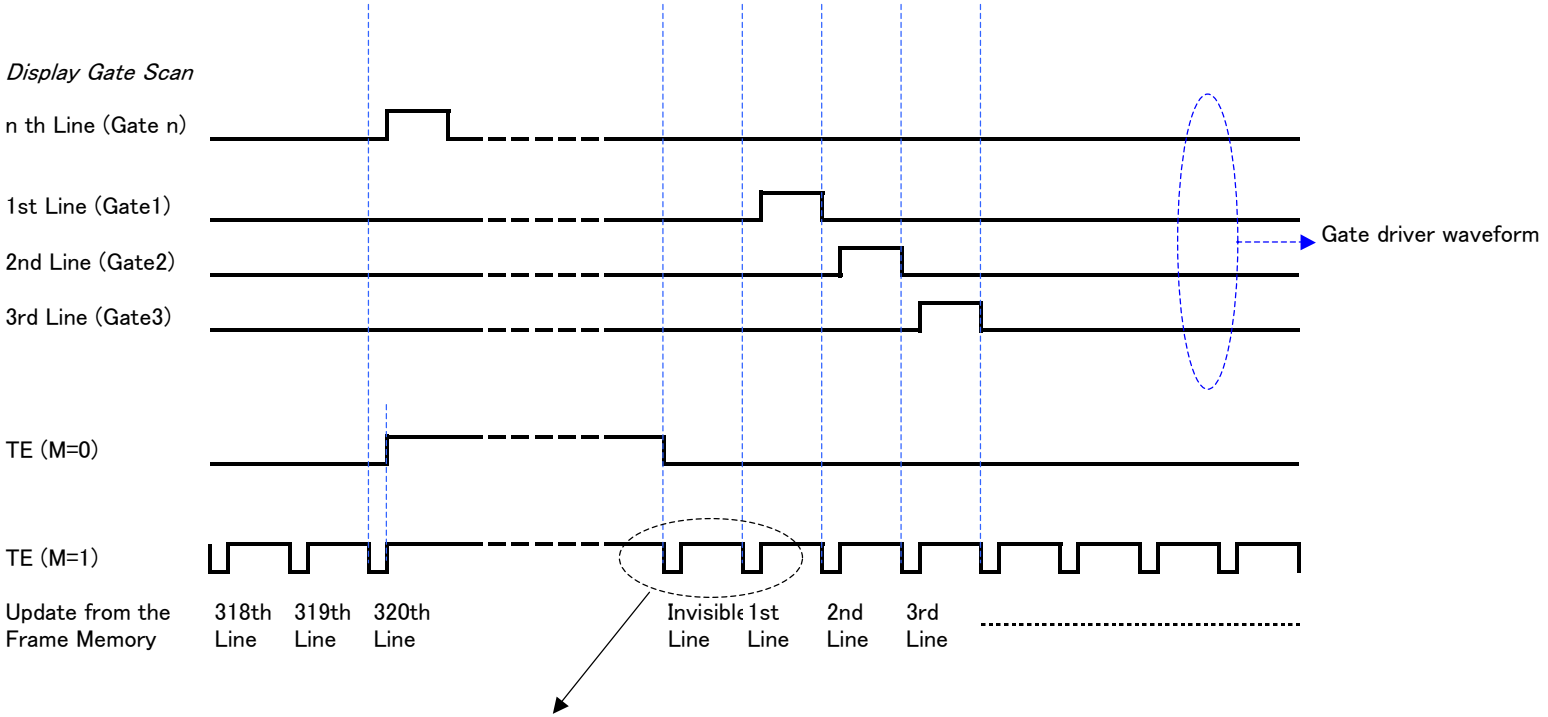
TE Pin Output Signal

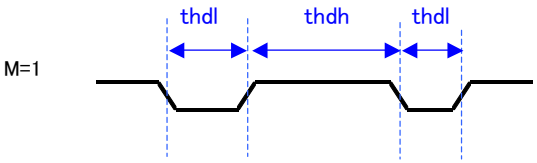
Tearing Effect Line signal or FMARK signal can be output from TE pin as frame memory data transfer synchronous signals. TE signal is trigger for frame memory write operation to enable data transfer in synchronization with the scanning operation. Tearng Effect Output signal is turned on/off by set_tear_off (34h) and set_tear_on (35h) commands.

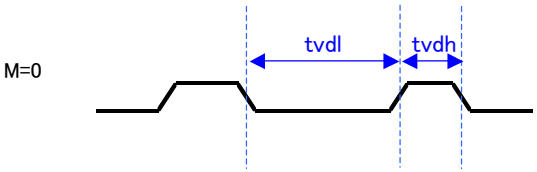
Table 27

TEON(35h)	TELOM (35h's1st parameter)	TE pin output
0	*	GND
1	0	TE (Mode1)
1	1	TE (Mode2)

35h set tear on command







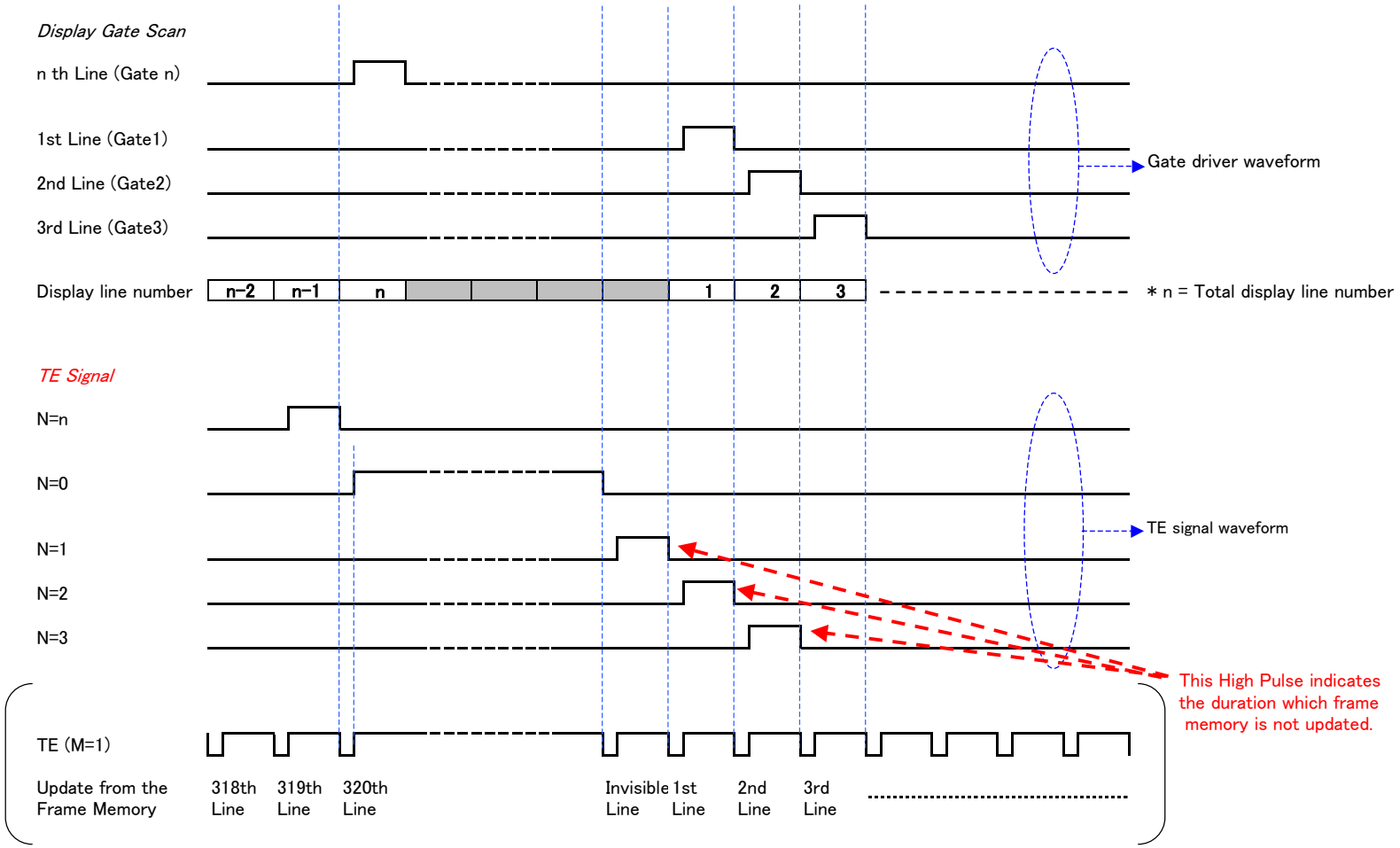
Definition

thdh : The LCD Display is not updated from the Frame Memory.
thdl : The LCD Display is updated from the Frame Memory.

tvdh : The LCD Display is not updated from the Frame Memory.
tvdl : The LCD Display is updated from the Frame Memory.

44h set_tear_scanline command

STS[8:0] Setting (N=0 ～ n)



When STS[8:0]=0, the waveform of TE is same as the one when 35h M=0.
When STS[8:0] is not equal 0, TE signal is shown above.

Restrictions
N≦(Number of line (NL bit)) + 1

Display-Synchronous Data Transfer Using TE/FMARK Signal

The R61516 enables data transfer in synchronization with the display scan by writing data to the internal frame memory using the TE signal as the trigger.

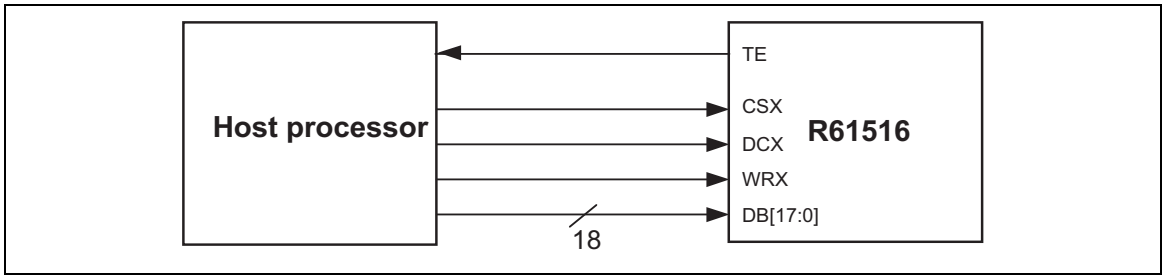


Figure 54 Interface Example for Display-Synchronous Data Transfer

By writing data to the internal Frame Memory at faster than calculated minimum speed, it becomes possible to rewrite the video image data without flickering the display and display video image via system interface. The display data is written in the Frame Memory so that the R61516 rewrites the data only within the video image area and minimize the number of data transfer required to display video image.

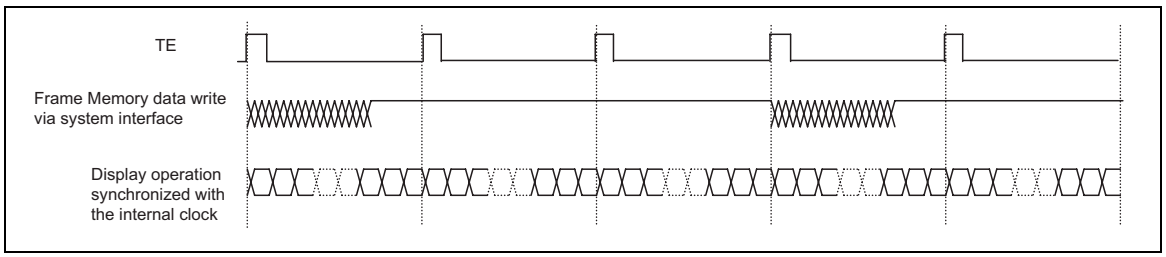


Figure 55 Video Image Data Write via TE/FMARK

When transferring data using TE as the trigger, there are restrictions in setting the minimum Frame Memory data write speed and the minimum internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

Internal clock frequency (fosc) [Hz] = Frame frequency × (Display lines (NL) + Front porch (FP) + Back porch (BP)) × Clocks per 1H (RTN) × Variances

Frame memory write speed (min.) [Hz] >
240 × Display lines (NL) / {(FP + BP + Display lines (NL) − Margins) × Division ratio (DIV) × Clocks per 1H (RTN) × 1/ fosc}

Note: When frame memory write operation is not started right after the rising edge of TE, the time from the rising edge of FMARK until the start of frame memory write operation must also be taken into account.

An example of calculating the minimum frame memory writing speed and internal clock frequency for writing data in synchronization with display operation.

[Example]

Display size 240 RGB × 320 lines
Display lines 320 lines
Back/front porch 8/8 lines (BP = 4'h8/ FP = 4'h8)
Frame marker position (FMP) The end line of the display: 320th line
Frame frequency 60 Hz
Internal operation clock 678kHz x 1.07 = 726kHz
Division ratio of display operation clock 1/2
Clocks in 1H period 17 clocks

Note: This example includes variances attributed to LSI production process and room temperature. Other possible causes of variances, such as voltage change, are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for frame memory writing [Hz]
> 240 × 320 / {((8+8 + 320 - 2) lines × 2 × 17 clocks) × 1/726 kHz} = 4.91 MHz

Notes: 1. In this example, it is assumed that the R61516 starts writing data in the frame memory on the rising edge of TE.
2. There must be at least a margin of 2 lines between the line to which the R61516 has just written data and the line where the display operation on the LCD is performed.
3. TE signal may be set on any line.

In this example, the frame memory write operation at a speed of 4.91MHz or more, which starts on the rising edge of FMARK, guarantees the completion of data write operation in a certain line address before the R61516 starts the display operation of the data written in that line and can write video image data without causing flicker on the display.

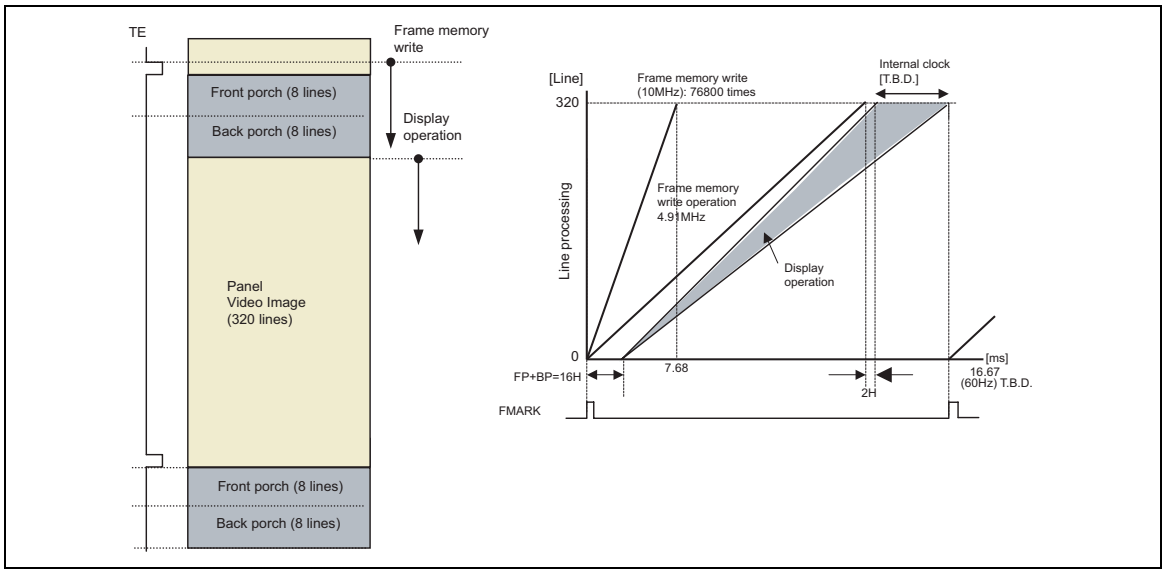


Figure 56

Liquid Crystal Panel Interface Timing

The following figure shows the timing of DPI and liquid crystal panel interface signals in DPI operation.

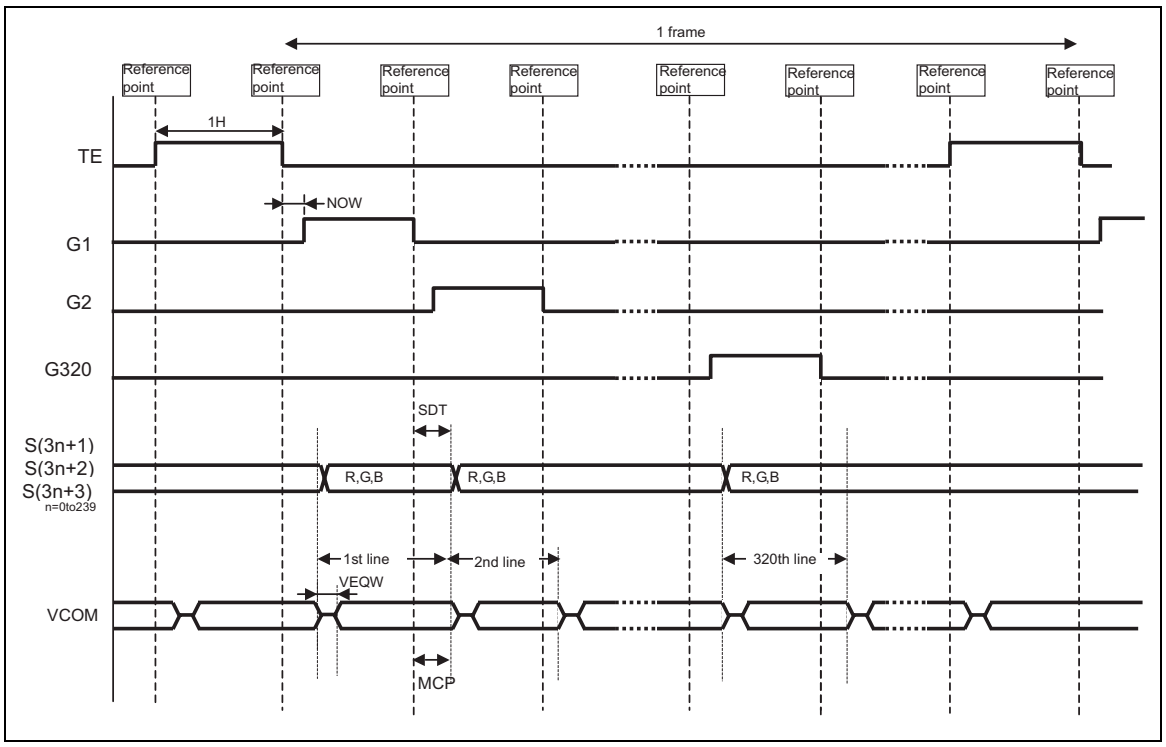


Figure 57 Liquid Crystal Panel Interface Timing in Internal Clock Opearation

VCOM and source output alternating positions are defined separately.

Note 1: The shown TE waveform has values M=0, set_tear_scanline N[9:0]=1.

Note 2: In the figure above, VCOM waveform is example when BCn=1, PTV=1.

Setting range
MCP[2:0]: 1 to 7clks
SDT[2:0]: 1 to 7clks
NOW[2:0]: 1 to 7clks
Units: 1clk

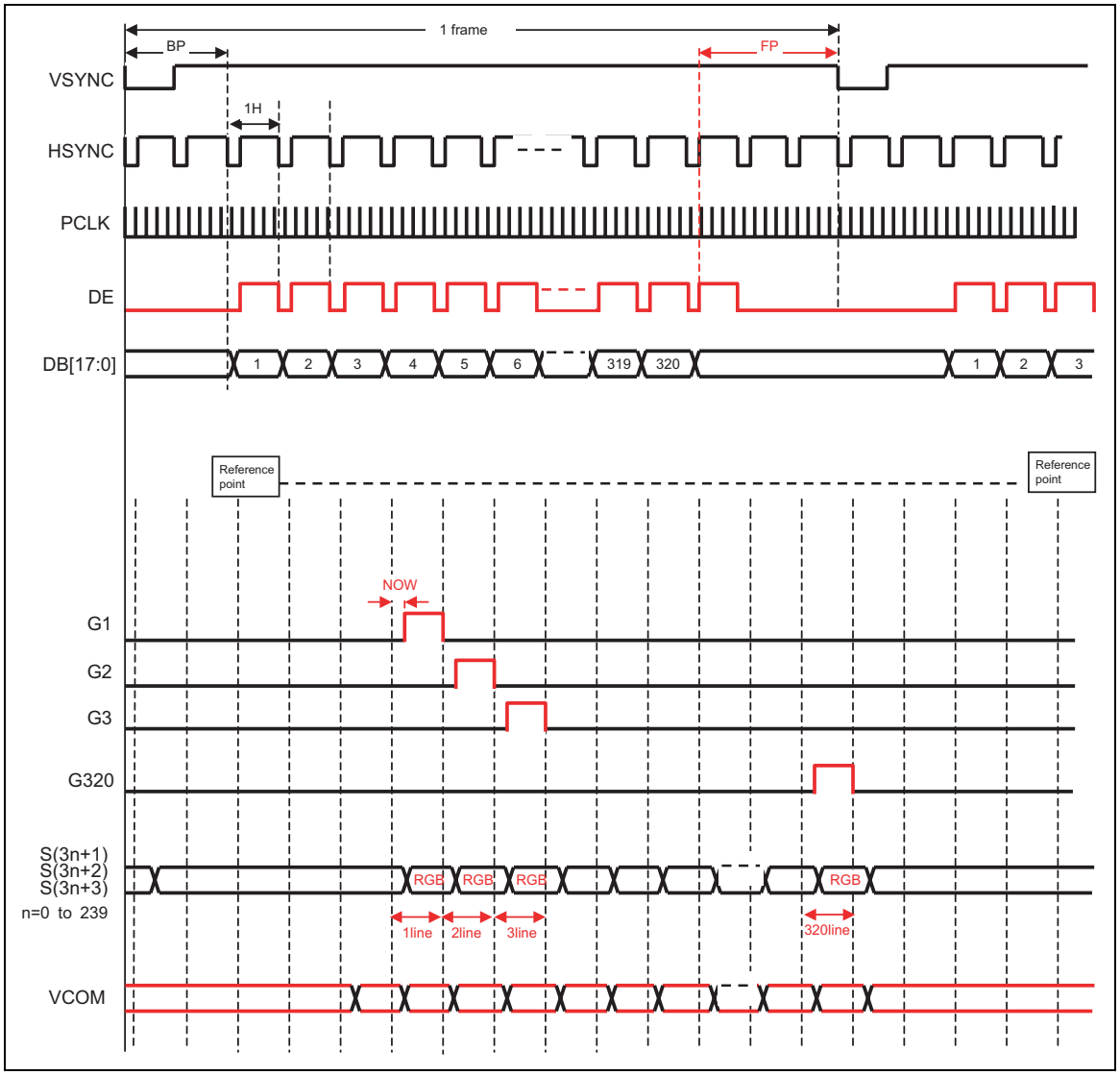


Figure 58 Liquid Crystal Panel Interface Timing in DPI Operation

Note: In the figure above, VCOM waveform is example when BCn=1, PTV=1.

γ Correction Function

γ Correction Function

The R61516 supports γ-correction function to make the optimal colors according to the characteristics of the panel. The R61516 has registers for positive and negative polarities to allow different settings for R, G, and B dots.

γ Correction Circuit

The following figure shows the γ-correction circuit. According to the settings of variable resistors R0 to R8, the voltage the level of which is the difference is between VREG and VGS is evenly divided into 12-grayscale reference voltages (V0, V1, V8, V20, V43, V55, V62 and V63). Other 42-grayscale voltages are generated by setting the level at a certain interval between the reference voltages. For grayscale voltage, see "Grayscale Volatge Calculation Formula".

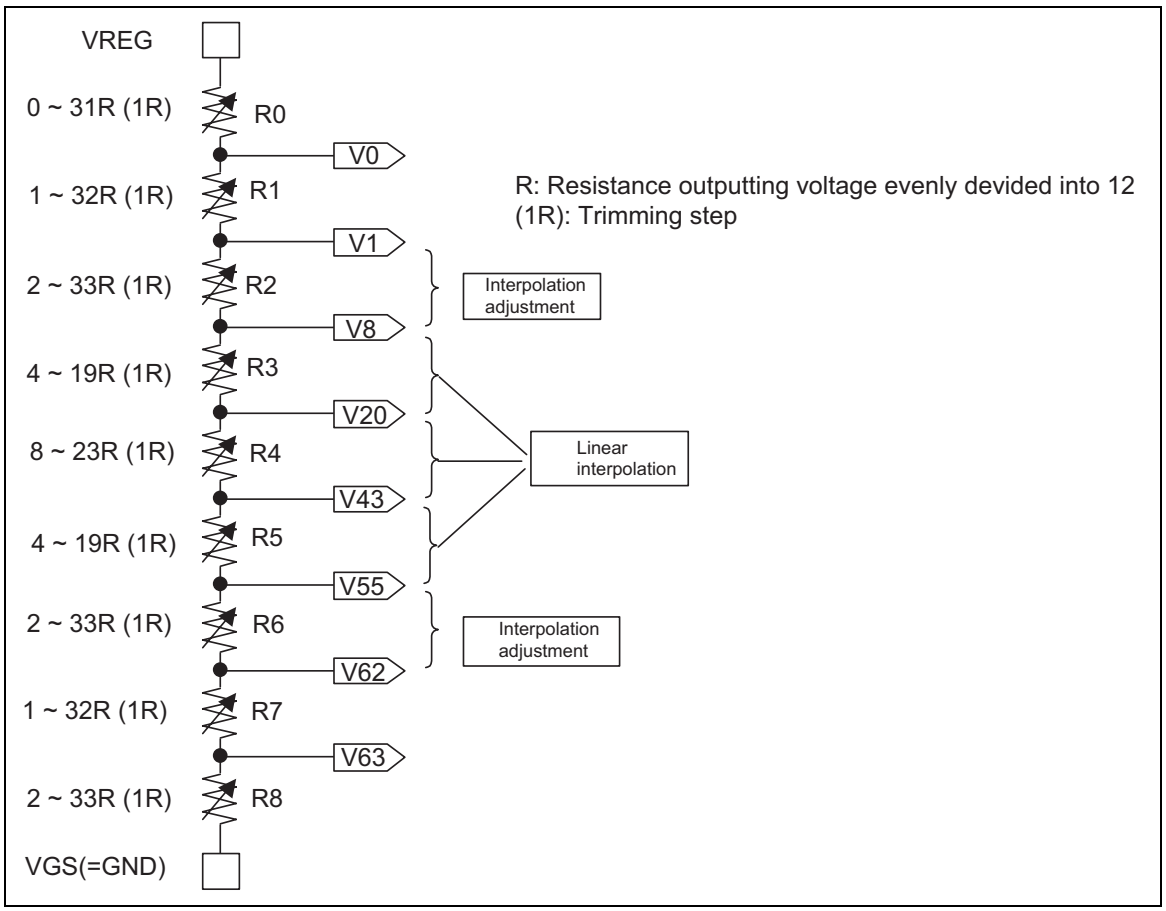


Figure 59

γ Correction Registers

The γ-correction registers include 42 bits per R, G, and B dots and 8bit interpolation adjustment registers. In the 8-color mode, R, G and B bits have same value which is determined by GammaSet A setting.

Reference level adjustment registers

Table 28 Reference level adjustment registers

Resistor	Gamma Set A		Gamma Set B		Gamma Set C	
	Positive polarity	Negative polarity	Positive polarity	Negative polarity	Positive polarity	Negative polarity
R0	PR0P00[4:0]	PR0N00[4:0]	PR1P00[4:0]	PR1N00[4:0]	PR2P00[4:0]	PR2N00[4:0]
R1	PR0P01[4:0]	PR0N01[4:0]	PR1P01[4:0]	PR1N01[4:0]	PR2P01[4:0]	PR2N01[4:0]
R2	PR0P02[4:0]	PR0N02[4:0]	PR1P02[4:0]	PR1N02[4:0]	PR2P02[4:0]	PR2N02[4:0]
R3	PR0P03[3:0]	PR0N03[3:0]	PR1P03[3:0]	PR1N03[3:0]	PR2P03[3:0]	PR2N03[3:0]
R4	PR0P04[3:0]	PR0N04[3:0]	PR1P04[3:0]	PR1N04[3:0]	PR2P04[3:0]	PR2N04[3:0]
R5	PR0P05[3:0]	PR0N05[3:0]	PR1P05[3:0]	PR1N05[3:0]	PR2P05[3:0]	PR2N05[3:0]
R6	PR0P06[4:0]	PR0N06[4:0]	PR1P06[4:0]	PR1N06[4:0]	PR2P06[4:0]	PR2N06[4:0]
R7	PR0P07[4:0]	PR0N07[4:0]	PR1P07[4:0]	PR1N07[4:0]	PR2P07[4:0]	PR2N07[4:0]
R8	PR0P08[4:0]	PR0N08[4:0]	PR1P08[4:0]	PR1N08[4:0]	PR2P08[4:0]	PR2N08[4:0]

Table 29 Reference level adjustment registers and resistors

Resistor	Register		Resistance	Resistor	Register		Resistance
	Name	Value			Name	Value	
R0	PR**0[4:0]	5'h00	0R	R5	PR**5[3:0]	4'h0	4R
		5'h01	1R			4'h1	5R
		5'h02	2R			4'h2	6R
		⋮	⋮			⋮	⋮
		5'h1F	31R			4'hF	19R
R1	PR**1[4:0]	5'h00	1R	R6	PR**6[4:0]	5'h00	2R
		5'h01	2R			5'h01	3R
		5'h02	3R			5'h02	4R
		⋮	⋮			⋮	⋮
		5'h1F	32R			5'h1F	33R
R2	PR**2[4:0]	5'h00	2R	R7	PR**7[4:0]	5'h00	1R
		5'h01	3R			5'h01	2R
		5'h02	4R			5'h02	3R
		⋮	⋮			⋮	⋮
		5'h1F	33R			5'h1F	32R
R3	PR**3[3:0]	4'h0	4R	R8	PR**8[4:0]	5'h00	2R
		4'h1	5R			5'h01	3R
		4'h2	6R			5'h02	4R
		⋮	⋮			⋮	⋮
		4'hF	19R			5'h1F	33R
R4	PR**4[3:0]	4'h0	8R				
		4'h1	9R				
		4'h2	10R				
		⋮	⋮				
		4'hF	23R				

Note: ** indicates 0P / 0N / 1P / 1N / 2P / 2N.

Interpolation Registers

Table 30 Interpolation Registers

Interpolation adjustment	Gamma Set A		Gamma Set B		Gamma Set C	
	Positive polarity	Negative polarity	Positive polarity	Negative polarity	Positive polarity	Negative polarity
V2～V7	PI0P0[1:0]	PI0N0[1:0]	PI1P0[1:0]	PI1N0[1:0]	PI2P0[1:0]	PI2N0[1:0]
	PI0P1[1:0]	PI0N1[1:0]	PI1P1[1:0]	PI1N1[1:0]	PI2P1[1:0]	PI2N1[1:0]
V56～V61	PI0P2[1:0]	PI0N2[1:0]	PI1P2[1:0]	PI1N2[1:0]	PI2P2[1:0]	PI2N2[1:0]
	PI0P3[1:0]	PI0N3[1:0]	PI1P3[1:0]	PI1N3[1:0]	PI2P3[1:0]	PI2N3[1:0]

Table 31 Interpolation factor for V2 to V7

(See "Grayscale Voltage Calculation Formula" for IPV* level)

PI**0[1:0]	PI**1[1:0]	IPV2	IPV3	IPV4	IPV5	IPV6	IPV7
2'h0	2'h0	81%	67%	52%	39%	26%	13%
	2'h1	78%	61%	43%	33%	22%	11%
	2'h2	73%	52%	31%	23%	15%	8%
	2'h3	72%	50%	28%	21%	14%	7%
2'h1	2'h0	80%	68%	56%	42%	28%	14%
	2'h1	76%	62%	48%	36%	24%	12%
	2'h2	70%	52%	35%	26%	17%	9%
	2'h3	69%	50%	31%	23%	16%	8%
2'h2	2'h0	78%	70%	61%	46%	30%	15%
	2'h1	74%	63%	53%	39%	26%	13%
	2'h2	66%	53%	39%	29%	20%	10%
	2'h3	64%	50%	36%	27%	18%	9%
2'h3	2'h0	78%	70%	63%	47%	31%	16%
	2'h1	73%	64%	54%	41%	27%	14%
	2'h2	65%	53%	41%	31%	20%	10%
	2'h3	63%	50%	37%	28%	19%	9%

Table 32 Interpolation factor for V56 to V61

PI**3[1:0]	PI**2[1:0]	IPV56	IPV57	IPV58	IPV59	IPV60	IPV61
2'h0	2'h0	87%	74%	61%	48%	33%	19%
	2'h1	89%	78%	67%	57%	39%	22%
	2'h2	92%	85%	77%	69%	48%	27%
	2'h3	93%	86%	79%	72%	50%	28%
2'h1	2'h0	86%	72%	58%	44%	32%	20%
	2'h1	88%	76%	64%	52%	38%	24%
	2'h2	91%	83%	74%	65%	48%	30%
	2'h3	92%	84%	77%	69%	50%	31%
2'h2	2'h0	85%	70%	54%	39%	30%	22%
	2'h1	87%	74%	61%	47%	37%	26%
	2'h2	90%	80%	71%	61%	47%	34%
	2'h3	91%	82%	73%	64%	50%	36%
2'h3	2'h0	84%	69%	53%	38%	30%	22%
	2'h1	86%	73%	59%	46%	36%	27%
	2'h2	90%	80%	69%	59%	47%	35%
	2'h3	91%	81%	72%	63%	50%	37%

Note: ** indicates 0P / 0N / 1P / 1N / 2P / 2N.

Table 33 Grayscale Voltage Calculation Formula

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	ΔV x Σ(R1～R8)/SUMR	V32	V43 + (V20 − V43) x 11/23
V1	ΔV x Σ(R2～R8)/SUMR	V33	V43 + (V20 − V43) x 10/23
V2	V8 + (V1 − V8) x IPV2	V34	V43 + (V20 − V43) x 9/23
V3	V8 + (V1 − V8) x IPV3	V35	V43 + (V20 − V43) x 8/23
V4	V8 + (V1 − V8) x IPV4	V36	V43 + (V20 − V43) x 7/23
V5	V8 + (V1 − V8) x IPV5	V37	V43 + (V20 − V43) x 6/23
V6	V8 + (V1 − V8) x IPV6	V38	V43 + (V20 − V43) x 5/23
V7	V8 + (V1 − V8) x IPV7	V39	V43 + (V20 − V43) x 4/23
V8	ΔV x Σ(R3～R8)/SUMR	V40	V43 + (V20 − V43) x 3/23
V9	V20 + (V8 − V20) x 11/12	V41	V43 + (V20 − V43) x 2/23
V10	V20 + (V8 − V20) x 10/12	V42	V43 + (V20 − V43) x 1/23
V11	V20 + (V8 − V20) x 9/12	V43	ΔV x Σ(R5～R8)/SUMR
V12	V20 + (V8 − V20) x 8/12	V44	V55 + (V43 − V55) x 11/12
V13	V20 + (V8 − V20) x 7/12	V45	V55 + (V43 − V55) x 10/12
V14	V20 + (V8 − V20) x 6/12	V46	V55 + (V43 − V55) x 9/12
V15	V20 + (V8 − V20) x 5/12	V47	V55 + (V43 − V55) x 8/12
V16	V20 + (V8 − V20) x 4/12	V48	V55 + (V43 − V55) x 7/12
V17	V20 + (V8 − V20) x 3/12	V49	V55 + (V43 − V55) x 6/12
V18	V20 + (V8 − V20) x 2/12	V50	V55 + (V43 − V55) x 5/12
V19	V20 + (V8 − V20) x 1/12	V51	V55 + (V43 − V55) x 4/12
V20	ΔV x Σ(R4～R8)/SUMR	V52	V55 + (V43 − V55) x 3/12
V21	V43 + (V20 − V43) x 22/23	V53	V55 + (V43 − V55) x 2/12
V22	V43 + (V20 − V43) x 21/23	V54	V55 + (V43 − V55) x 1/12
V23	V43 + (V20 − V43) x 20/23	V55	ΔV x Σ(R6～R8)/SUMR
V24	V43 + (V20 − V43) x 19/23	V56	V62 + (V55 − V62) x IPV56
V25	V43 + (V20 − V43) x 18/23	V57	V62 + (V55 − V62) x IPV57
V26	V43 + (V20 − V43) x 17/23	V58	V62 + (V55 − V62) x IPV58
V27	V43 + (V20 − V43) x 16/23	V59	V62 + (V55 − V62) x IPV59
V28	V43 + (V20 − V43) x 15/23	V60	V62 + (V55 − V62) x IPV60
V29	V43 + (V20 − V43) x 14/23	V61	V62 + (V55 − V62) x IPV61
V30	V43 + (V20 − V43) x 13/23	V62	ΔV x (R7 + R8)/SUMR
V31	V43 + (V20 − V43) x 12/23	V63	ΔV x R8/SUMR

Note: Make sure that
ΔV = VREG – VGS
SUMR = Σ(R0～R8) ≥ 70R.
V63 ≥ 0.2V

Frame Memory Data and the Grayscale Voltage

Table 34

Frame memory data	Grayscale Voltage				Frame memory data	Grayscale Voltage			
	REV = 1		REV = 0			REV = 1		REV = 0	
	Positive polarity	Negative polarity	Positive polarity	Negative polarity		Positive polarity	Negative polarity	Positive polarity	Negative polarity
6'h00	V0	V63	V63	V0	6'h20	V32	V31	V31	V32
6'h01	V1	V62	V62	V1	6'h21	V33	V30	V30	V33
6'h02	V2	V61	V61	V2	6'h22	V34	V29	V29	V34
6'h03	V3	V60	V60	V3	6'h23	V35	V28	V28	V35
6'h04	V4	V59	V59	V4	6'h24	V36	V27	V27	V36
6'h05	V5	V58	V58	V5	6'h25	V37	V26	V26	V37
6'h06	V6	V57	V57	V6	6'h26	V38	V25	V25	V38
6'h07	V7	V56	V56	V7	6'h27	V39	V24	V24	V39
6'h08	V8	V55	V55	V8	6'h28	V40	V23	V23	V40
6'h09	V9	V54	V54	V9	6'h29	V41	V22	V22	V41
6'h0A	V10	V53	V53	V10	6'h2A	V42	V21	V21	V42
6'h0B	V11	V52	V52	V11	6'h2B	V43	V20	V20	V43
6'h0C	V12	V51	V51	V12	6'h2C	V44	V19	V19	V44
6'h0D	V13	V50	V50	V13	6'h2D	V45	V18	V18	V45
6'h0E	V14	V49	V49	V14	6'h2E	V46	V17	V17	V46
6'h0F	V15	V48	V48	V15	6'h2F	V47	V16	V16	V47
6'h10	V16	V47	V47	V16	6'h30	V48	V15	V15	V48
6'h11	V17	V46	V46	V17	6'h31	V49	V14	V14	V49
6'h12	V18	V45	V45	V18	6'h32	V50	V13	V13	V50
6'h13	V19	V44	V44	V19	6'h33	V51	V12	V12	V51
6'h14	V20	V43	V43	V20	6'h34	V52	V11	V11	V52
6'h15	V21	V42	V42	V21	6'h35	V53	V10	V10	V53
6'h16	V22	V41	V41	V22	6'h36	V54	V9	V9	V54
6'h17	V23	V40	V40	V23	6'h37	V55	V8	V8	V55
6'h18	V24	V39	V39	V24	6'h38	V56	V7	V7	V56
6'h19	V25	V38	V38	V25	6'h39	V57	V6	V6	V57
6'h1A	V26	V37	V37	V26	6'h3A	V58	V5	V5	V58
6'h1B	V27	V36	V36	V27	6'h3B	V59	V4	V4	V59
6'h1C	V28	V35	V35	V28	6'h3C	V60	V3	V3	V60
6'h1D	V29	V34	V34	V29	6'h3D	V61	V2	V2	V61
6'h1E	V30	V33	V33	V30	6'h3E	V62	V1	V1	V62
6'h1F	V31	V32	V32	V31	6'h3F	V63	V0	V0	V63

Power-Supply Generating Circuit

The following figure shows the configutration of LCD drive voltage generating circuit of the R61516.

Power Supply Circuit Connection Example 1

VCI level is adjusted internally by the VCI1 output circuit.

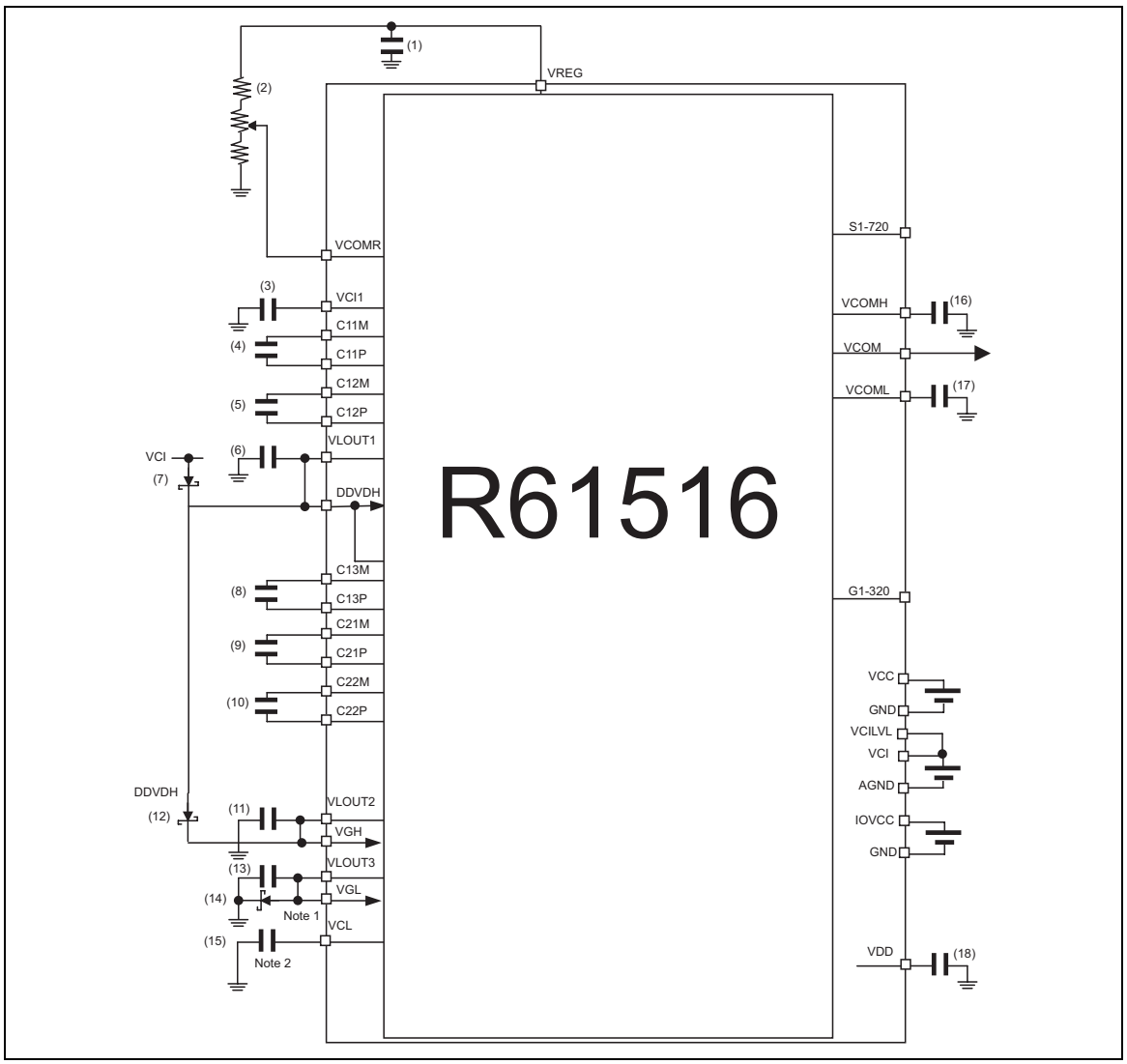


Figure 60

Note 1: The wiring resistance from GND and VGL to the schottky diode must be 10 ohm or less.
Note 2: Variable resistor (2) is not required if VCOM setting value is loaded from internal NVM or EEPROM.

Power Supply Circuit Connection Example 2 (VCI1 = VCI direct input)

The electrical potential VCI is directly applied to VCI1. In this case, the VCI1 level cannot be adjusted internally (see Note 2), but step-up operation becomes more effective. (Only when VCI=3.0V or less)

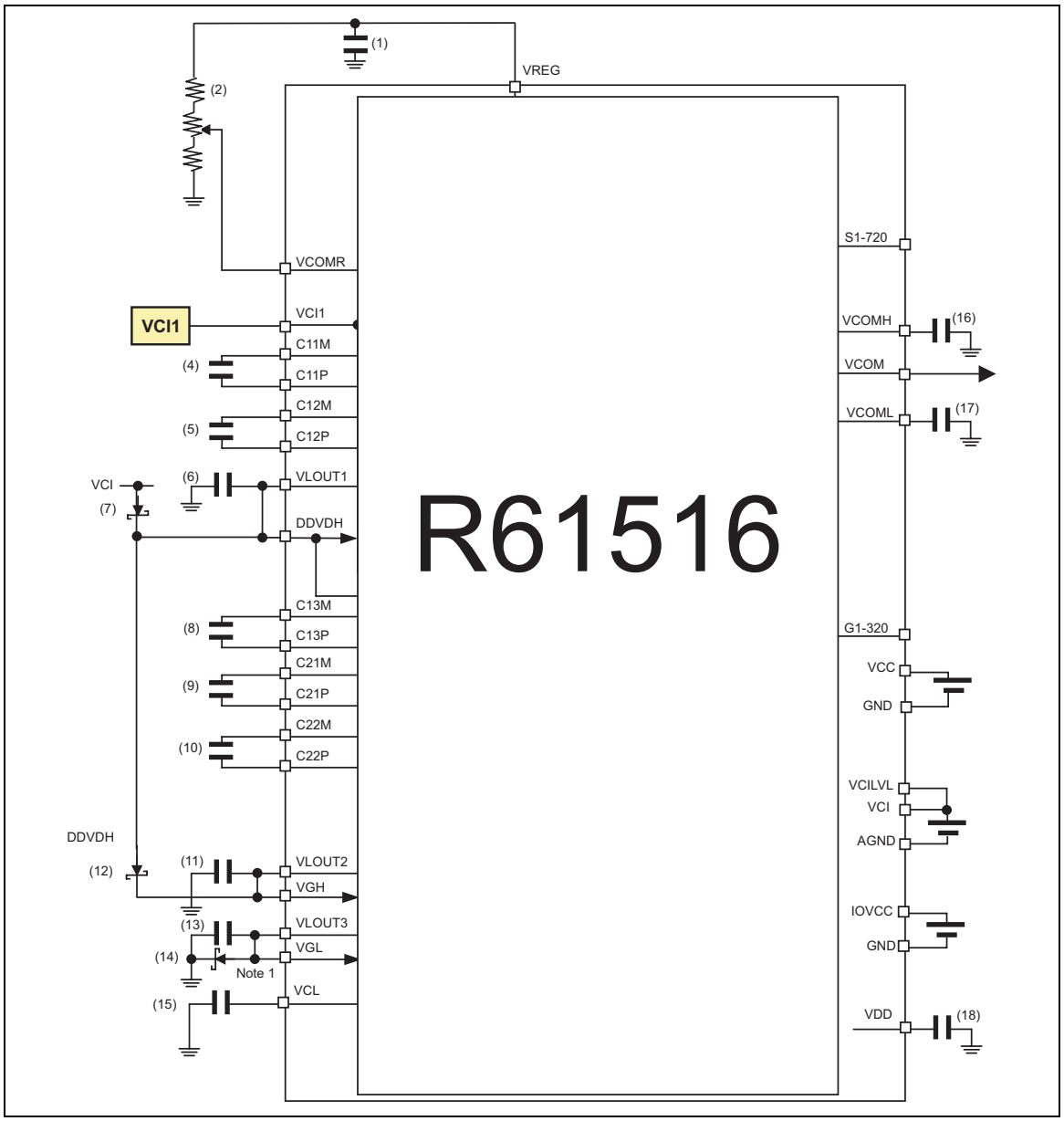


Figure 61

Note 1: The wiring resistance from GND and VGL to the schottky diode must be 10 ohm or less.

Note 2: Variable resistor (2) is not required if VCOM setting value is loaded from internal NVM or EEPROM.

Note 3: When the VCI level is direcly applied to VCI1, set VC[2:0]=3'h7 (1st parameter, D0h)=1 (VCI1 halts). Capacitor connected to VCI1 is not required.

Specifications of External Elements Connected to the Power Supply Circuit

The following table shows specifications of external elements connected to the R61516's power supply circuit. The numbers of the pins to connect correspond to the numbers shown in Configuration of Power Supply Circuit.

Table 35 Capacitor Connected to LCD Power Supply Circuit

Capacity	Recommended voltage	Pin to connect
1 μF (B characteristics)	6V	(1)VREG, (3)VCI1, (4)C11P/M, (5)C12P/M, (8)C13P/M, (15)VCL, (16)VCOMH, (17)VCOML, (18)VDD
	10V	(6)VLOUT1, (9)C21P/M, (10)C22P/M
	25V	(11)VLOUT2, (13)VLOUT3

Table 36 Schottky Diode

Feature	Pin to connect
VF < 0.4V / 20mA at 25°C, VR ≥25V (Recommended diode: HSD226)	(7) VCI – DDVDH (12) DDVDH – VGH (14) GND – VGL

Table 37 Variable Resistance

Variable resistance	Pin to connect
>200Ω	(2)VCOMR

Note 1: Variable resistor (2) is not required if VCOM setting value is loaded from internal NVM or EEPROM.

Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the R61516 and the relationship between TFT display application voltage waveforms and electrical potential.

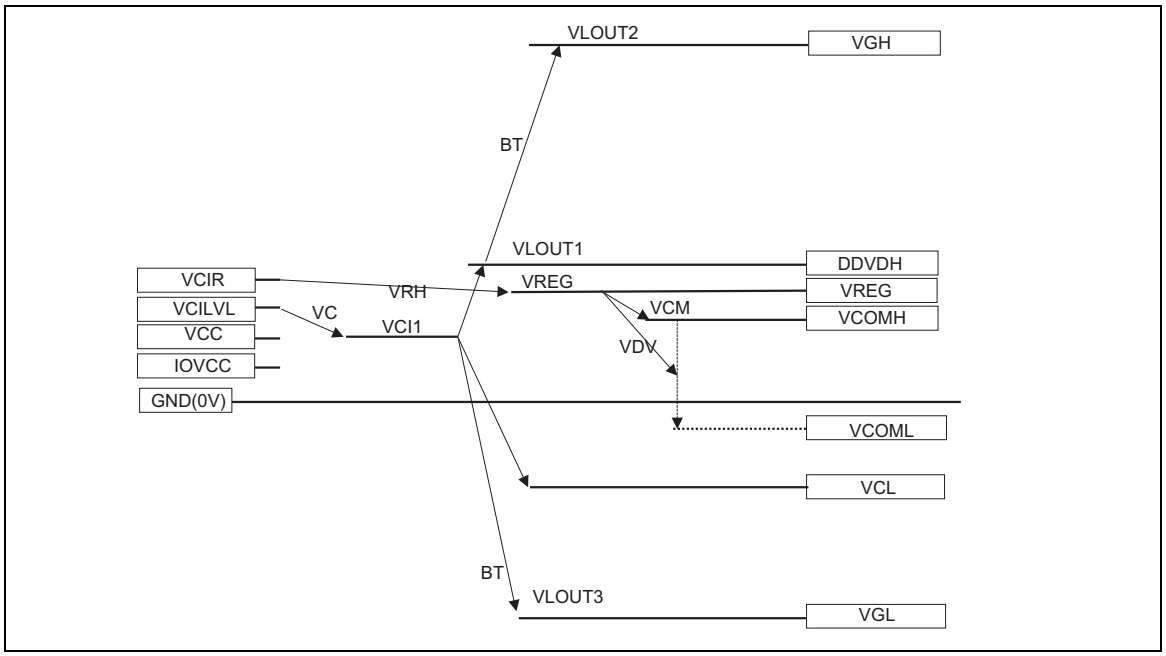


Figure 62 Voltage Setting Pattern Diagram

Note: 1. The DDVDH, VGH, VGL, VCL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at respective outputs. When the alternating cycle of Vcom is high (e.g. polarity inverts every line cycle), current consumption will increase. In this case, check the voltage before use.

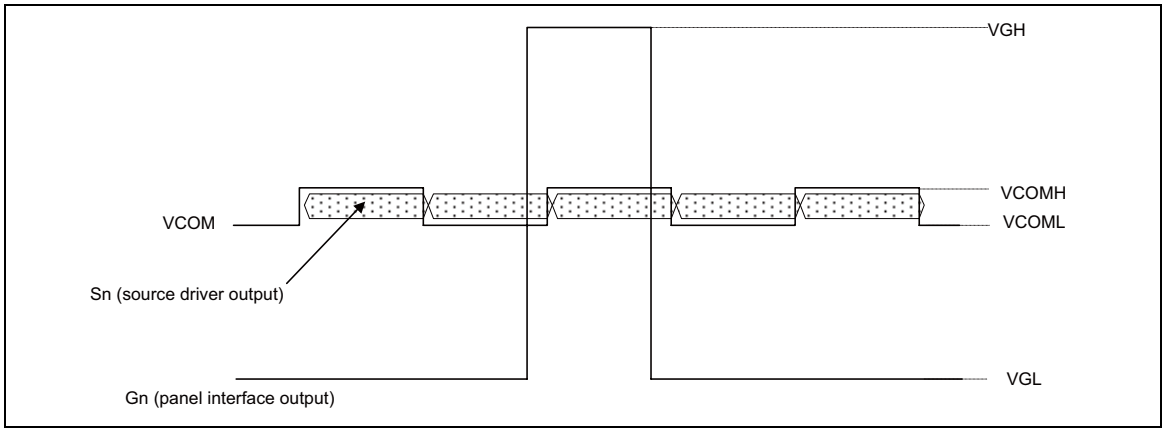


Figure 63 Voltage Application to TFT Display

NVM Control

The R61516 incorporates 39 bit NVM for user's use.

- 7 bit is for VCOM adjustment (VCM register value is stored)
- 16 bit is for Supplier ID (read by read_DDB_start and read_DDB_continue commands)
- 16 bit is for Supplier Elective Data (read by read_DDB_start and read_DDB_continue commands)

To write, read and erase data from/to the NVM, follow the sequences below. Data on the NVM is loaded to internal registers automatically when the sequences are performed.

Power On sequence

HW RESET sequence

exit_sleep_mode sequence

soft_reset sequence

Data written to the NVM is invalid if external EEPROM is used (EEPROME=High (VCC)).

Write VCM register value, Supplier ID and Supplier Elective Data to the EEPROM.

Data stored in the NVM is retained permanently even if power supply is turned off.

NVM Read Sequence

Data on the NVM is loaded either automatically or by setting a command.

The data written to the NVM is transferred to the internal register so that it is read.

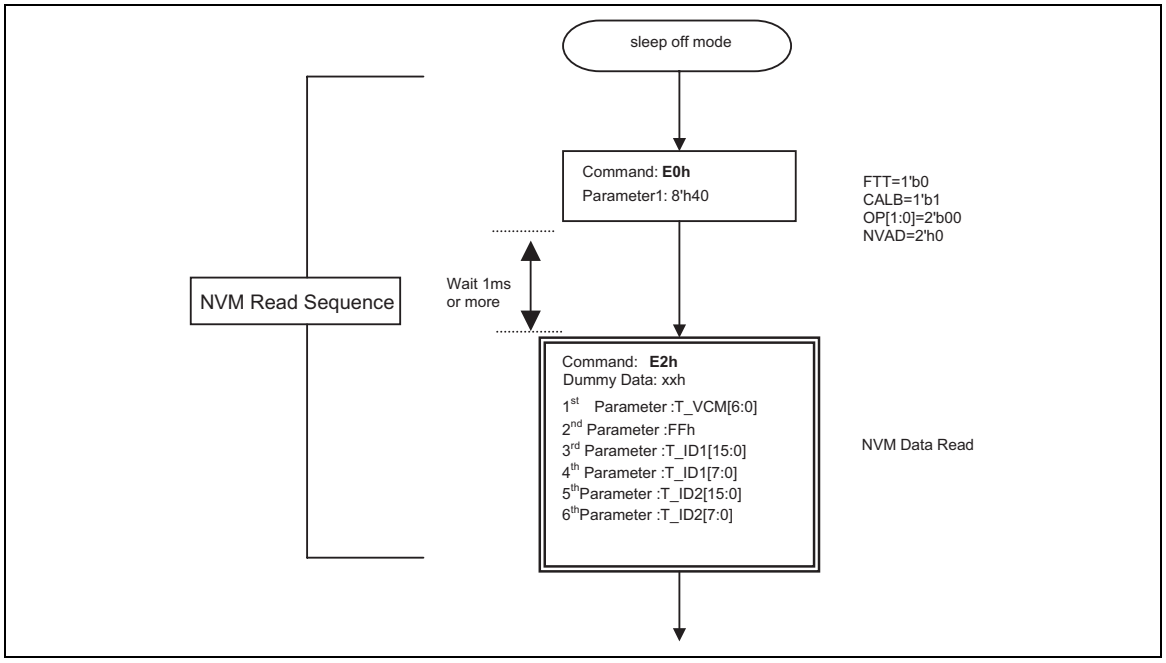


Figure 64 NVM Read Data Sequence

NVM Write Sequence

Defined 16 bit data is written to the selected address. When "0" is written to these bits, the bits are set to "0". If the data is erased from the bit, the bit is returned to "1". The bit to which data is not written should be set to "1".

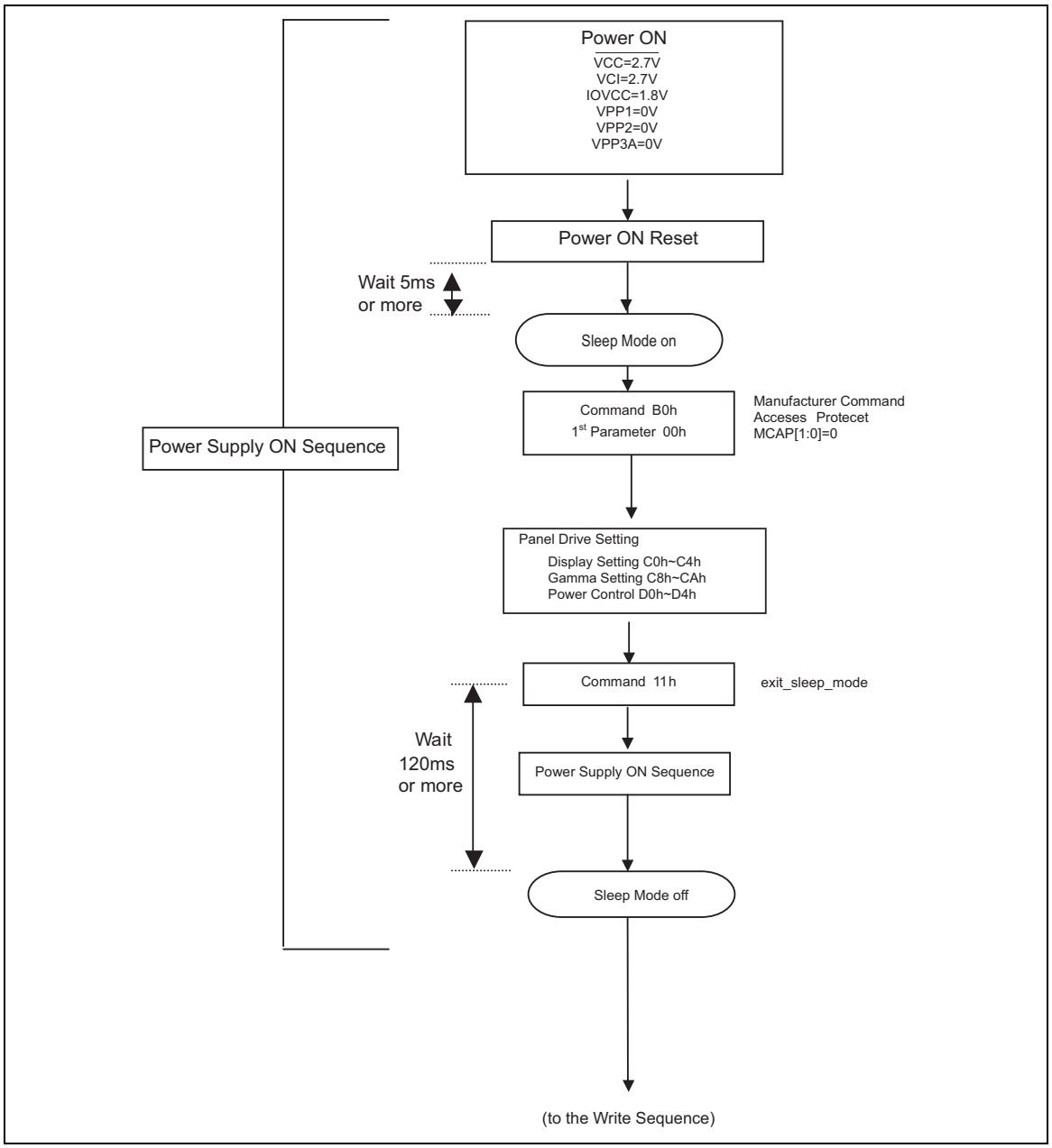


Figure 65 NVM Write Sequence

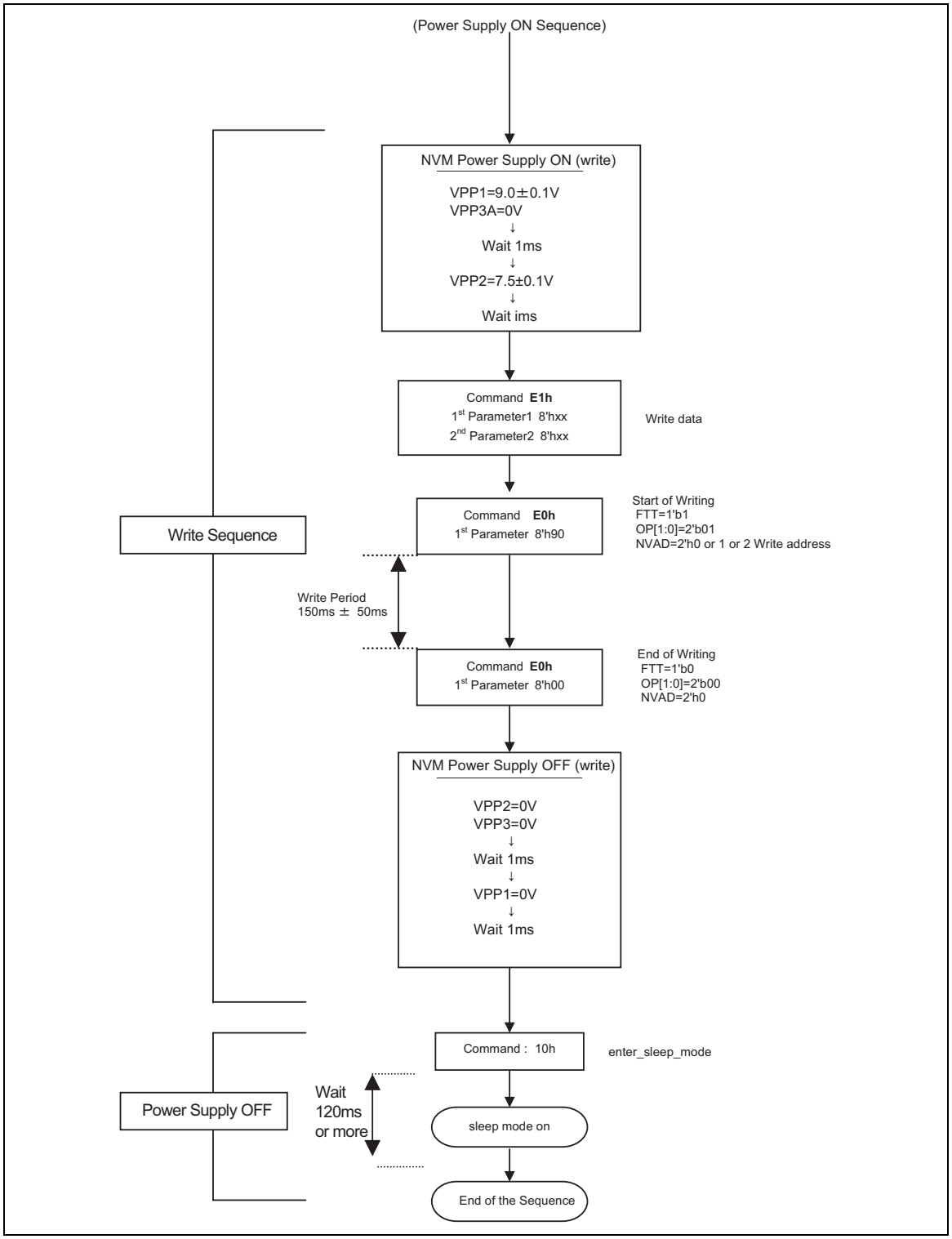


Figure 66 NVM Write Sequence (continued)

NVM Erase Sequence

The data written to the selected 16 bits is erased all together. The bits from which data is erased are set to "1".

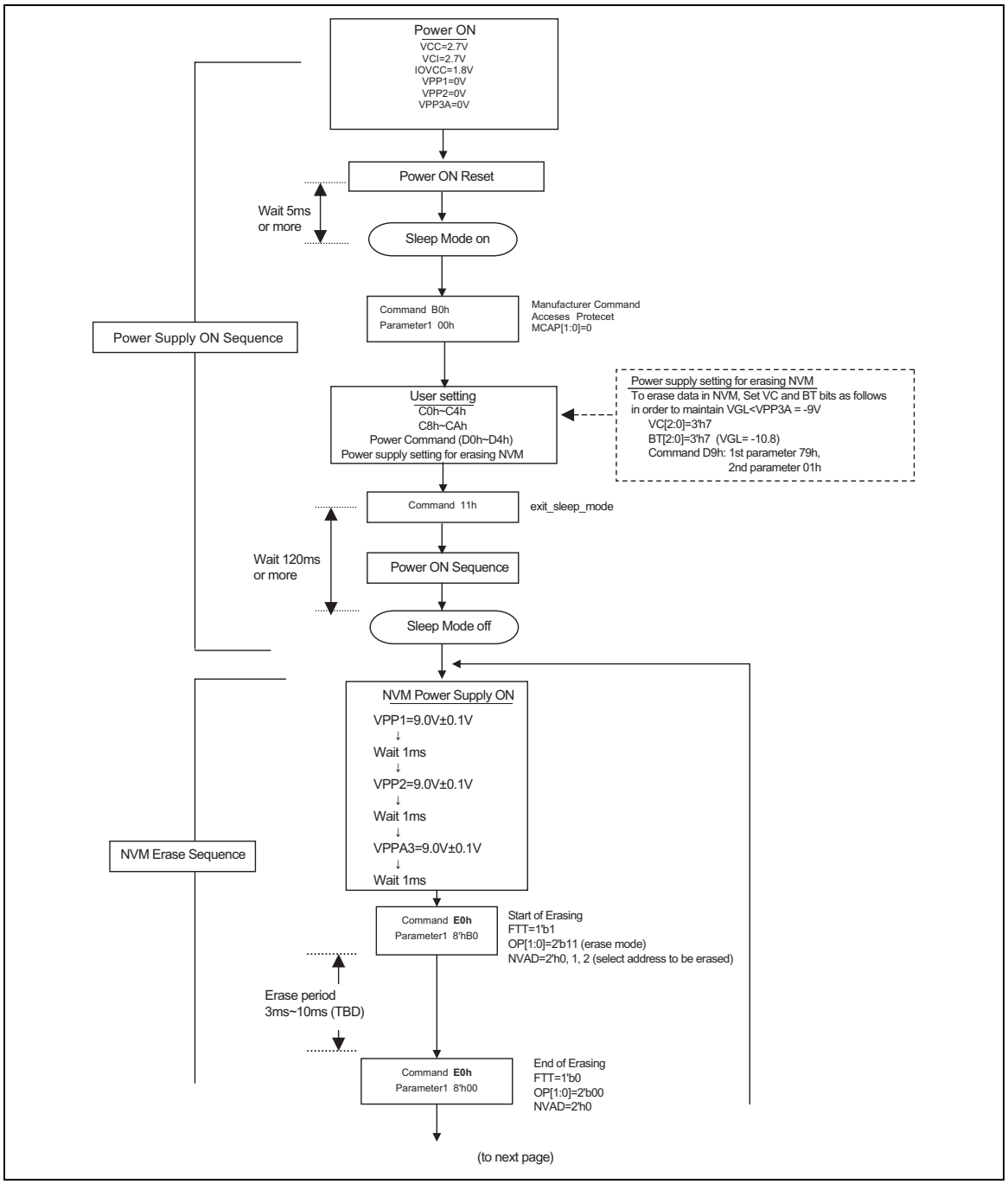


Figure 67 NVM Erase Sequence

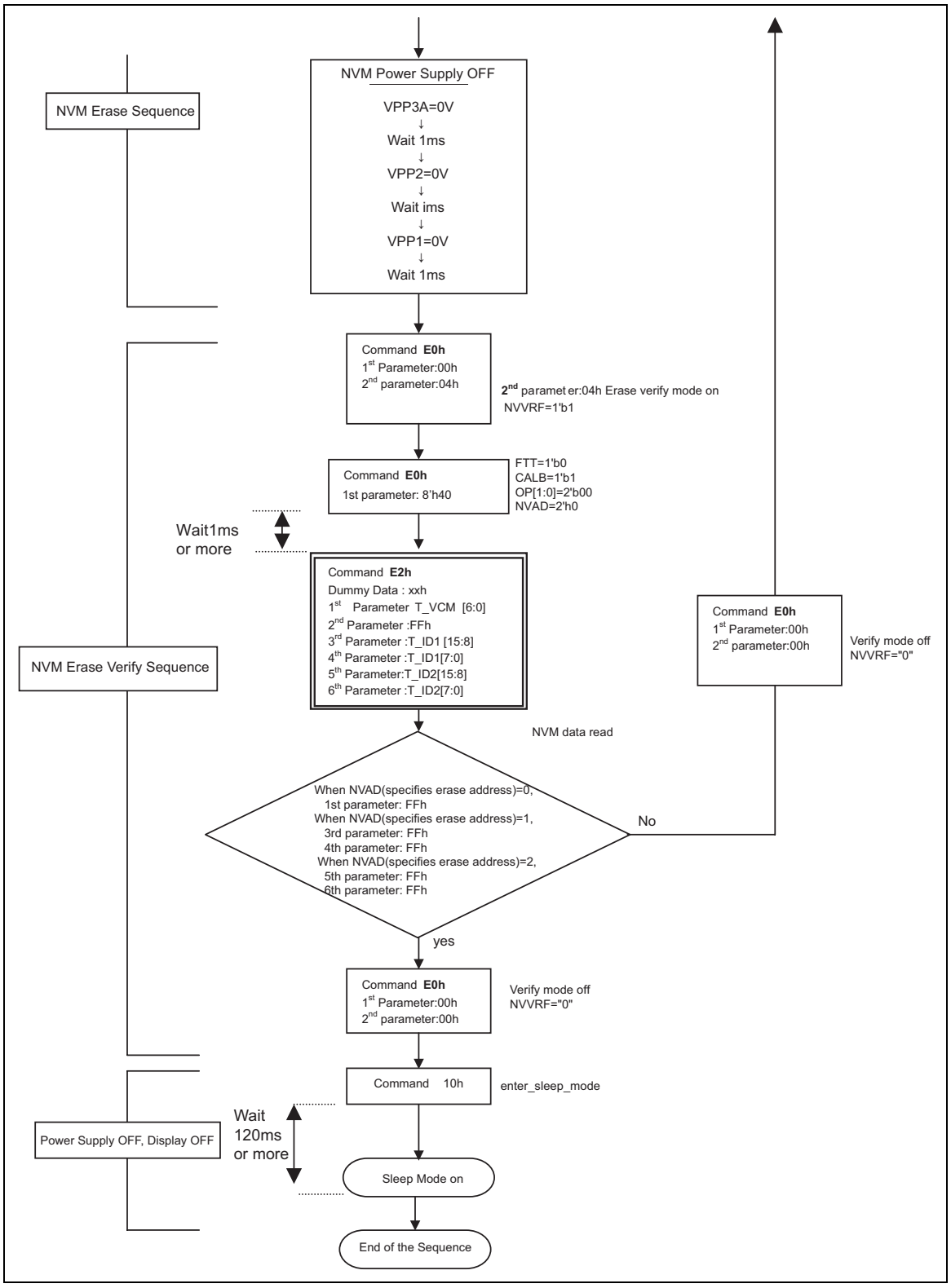


Figure 68 NVM Erase Sequence (continued)

Absolute Maximum Rating

Table 38

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	VCC,IOVCC	V	-0.3 ～ +4.6	1, 2
Power supply voltage (2)	VCI – AGND	V	-0.3 ～ +4.6	1, 3
Power supply voltage (3)	DDVDH – AGND	V	-0.3 ～ +6.5	1, 4
Power supply voltage (4)	AGND – VCL	V	-0.3 ～ +4.6	1
Power supply voltage (5)	DDVDH – VCL	V	-0.3 ～ +9.0	1, 5
Power supply voltage (7)	AGND– VGL	V	-0.3 ～ +13.0	1, 6
Power supply voltage (8)	VGH– VGL	V	-0.3 ～ +30.0	1
Power supply voltage (9)	VPP1	V	-0.3 ～ +10.0	1
Power supply voltage (10)	VPP2	V	-0.3 ～ +10.0	1
Power supply voltage (11)	VPP3A	V	-10.0 ～ +0.3	1
Input voltage	Vt	V	-0.3 ～ IOVCC + 0.3	1
Operating temperature	Topr	℃	-40 ～ +85	1, 7
Internal NVM write temperature	Twep	℃	+25～+35	1
Storage temperature	Tstg	℃	-55 ～ +110	1

Notes: 1. If used beyond the absolute maximum ratings, the LSI may be destroyed. It is strongly recommended to use the LSI within the limits of its electrical characteristics during normal operation. The reliability of LSI is not guaranteed if used in the conditions above the limits and it may lead to malfunction.

2. Make sure (High) VCC ≥ GND (Low), (High) IOVCC ≥ GND (Low).
3. Make sure (High) VCI ≥ AGND (Low).
4. Make sure (High) DDVDH ≥ AGND (Low).
5. Make sure (High) DDVDH ≥ VCL (Low).
6. Make sure (High) AGND ≥ VGL (Low).
7. The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

Electrical Characteristics

DC Characteristics

Table 39 (VCC= 2.5V ~ 3.3V, IOVCC=1.65V~ 3.1V, Ta=-40℃ ~ +85℃ Note 1) Target Spec

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Inpupt ”High” level voltage 1 Interface pin (except RESX)	V_{IH1}	V	IOVCC=1.65V ~ 3.1V	0.80 x IOVCC	–	IOVCC +0.3	2,3
Input ”Low” level voltage 1 Interface pin (except RESX)	V_{IL1}	V	IOVCC=1.65V ~ 3.1V	-0.3	–	0.20 x IOVCC	2, 3
Input”High” levele voltage 2 RESX pin	V_{IH2}	V	IOVCC=1.65V ~ 3.1V	0.90 x IOVCC	–	IOVCC + 0.3	2, 3
Input”Low” level voltage 2 RESX pin	V_{IL2}	V	IOVCC=1.65V ~ 3.1V	-0.3	–	0.10 x IOVCC	2, 3
Input ”High” level voltage 3 SDI pin	V_{IH3}	V	VCC=2.5V ~ 3.3V	0.80 x VCC	–	VCC + 0.3	2, 3
Input”Low” level voltage 3 SDI pin	V_{IL3}	V	VCC=2.5V ~ 3.3V	-0.3	–	0.20 x VCC	2, 3
Output ”High” level voltage 1 (DB[17:0], TE)	V_{OH1}	V	IOVCC=1.65V ~ 3.1V, IOH=-0.1mA	0.8 x IOVCC	–	–	2
Output ”Low” level voltage 1 (DB[17:0], TE)	V_{OL1}	V	IOVCC=1.65V ~ 3.1V, IOL=0.1mA	–	–	0.20 x IOVCC	2
Output ”High” level voltage 1 (SCS, SCL, SDO)	V_{OH3}	V	VCC=2.5V ~ 3.3V, IOH=-0.1mA	0.8 x VCC	–	–	2
Output ”Low” level voltage 1 (SCS, SCL, SDO)	V_{OL3}	V	VCC=2.5V ~ 3.3V, IOL=0.1mA	–	–	0.20 x VCC	2
Input/output leakage current from bus interface pins	I_{LI}	µA	Vin=0 ~ IOVCC	-1	–	1	4
Current consumption ((IOVCC-GND) + (VCC-GND)) Normal mode (260k-color, display operation)	I_{OP1}	µA	320 line drive, IOVCC=1.80V, VCC=VCI=2.80V, fFLM=60Hz, Ta=25C, Frame memory data: 18’h00000	–	200	300	5
Current consumption ((IOVCC-GND) + (VCC-GND)) Idel mode (64 line, partial display operation)	I_{op2}	µA	64 line partial display operation, IOVCC=1.80V, VCC=VCI=2.80V, fFLM=40Hz, Ta=25C, Frame memory data: 18h’00000	–	160	–	5
Current consumption ((IOVCC-GND) + (VCC-GND)) Sleep mode	I_{ST}	µA	IOVCC=VCC=2.8V, Ta=25C	–	50	-	5

Current consumption ((IOVCC-GND) + (VCC-GND)) Deep Stand by mode	I_{DST}	μA	IOVCC=VCC=2.8V, Ta=25C	–	0.1	1.0	5
Current consumption ((IOVCC-GND) + (VCC-GND)) Frame memory access mode (1) (HWM=0)	I_{RAM1}	mA	IOVCC=1.80V, VCC=VCI=2.80V, tCYCW=100ns, Ta=25℃, Consecutive frame memory access during display operation	–	2.8	–	5
Current consumption ((IOVCC-GND) + (VCC-GND)) Frame memory access mode (2) (HWM=1)	I_{RAM2}	mA	IOVCC=1.80V, VCC=VCI=2.80V, tCYCW=50ns, Ta=25C, Consecutive frame memory access during display operation	–	1.5	–	5
LCD power supply current (VCI-AGND) 260-k color display operation (Normal mode+Idle mode off)	Ici1	mA	IOVCC=1.8V, VCC=VCI=2.8V, 320 line drive, fFLM=60Hz, Ta=25C, Frame memory data: 18'h00000, REV=0, BC0=0, FP0=5, BP0=8, VC=3'h1, BT=3'h4, VRH=5'h18, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h5, DC10=3'h2, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0 PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2) No load on the panel	–	2.5	3.0	5

LCD power supply current (VCI-AGND) 8-color (64 line partial display operation) (Partial mode+Idele mode on)			Ici2	mA	IOVCC=1.8V, VCC=VCI=2.8V, 64 line partial display operation, fFLM=40Hz, Ta=25C, Frame memory data: 18'h00000, REV=0, BC2=0, FP2=5, BP2=8, VC=3'h1, BT=3'h4, VRH=5'h18, VCM=7'h7F, VDV=5'h11, AP2=2'h3, DC02=3'h5, DC12=3'h2, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0 PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2) No load on the panel	—	0.8	—	5
NVM current consumption	Write	VPP1	I_{VPP1W}	mA	VPP1=9.0V VPP2=7.5V VPP3A=GND (During Write period)	—	—	1.0	5
		VPP2	I_{VPP2W}	mA		—	—	20.0	5
		VPP3A	I_{VPP3AW}	mA		—	—	1.0	5
	Erase	VPP1	I_{VPP1E}	mA	VPP1=9.0V VPP2=9.0V VPP3A=-9.0V (During Erase period)	—	—	1.0	5
		VPP2	I_{VPP2E}	mA		—	—	1.0	5
		VPP3A	I_{VPP3AE}	mA		—	—	1.0	5
Output voltage dispersion			ΔVO	mV	—	—	5	—	6
Average output voltae variance			ΔVΔ	mV	—	−35	—	35	7

Step-up Circuit Characteristics

Table 40 Step-up Circuit Characteristics (Target Spec)

Item		Unit	Test Condition	Min.	Typ.	Max.	Note
Step-up output voltage	VLOUT1	V	IOVCC=VCC=2.8V, VCI =2.8V, Ta=25C, VC=3'h1, BT=3'h4, AP*=2'h3, DC0*=3'h5, DC1*=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, VLOUT1=VLOUT2=VLOUT3=VCL=1[uF]/B characteristics, No load on the panel, Iload1=-3 [mA]	4.89	5.16	-	Step-up output voltage
	VLOUT2	V	IOVCC=VCC=2.8V, VCI =2.8V, Ta=25C, VC=3'h1, BT=3'h4, AP*=2'h3, DC0*=3'h5, DC1*=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, VLOUT1=VLOUT2=VLOUT3=VCL=1[uF]/B characteristics, Iload2=-100[uA], No load on the panel	14.74	15.42	-	
	VLOUT3	V	IOVCC=VCC=2.8V, VCI =2.8V, Ta=25C, VC=3'h1, BT=3'h4, AP*=2'h3, DC0*=3'h5, DC1*=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, VLOUT1=VLOUT2=VLOUT3=VCL=1[uF]/B characteristics, Iload3=+100[uA], No load on the panel	-	-10.31	-10.04	
	VCL	V	IOVCC=VCC=2.8V, VCI =2.8V, Ta=25C, VC=3'h1, BT=3'h4, AP*=2'h3, DC0*=3'h5, DC1*=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, VLOUT1=VLOUT2=VLOUT3=VCL=1[uF]/B characteristics, Iload4=+200[uA], No load on the panel	-	-2.47	-2.42	

Internal Reference Voltage

Table 41 Internal Reference Voltage (VCC= 2.5V~3.3V, Ta=-40℃~ +85℃)

Item	Symbol	Unit	Min.	Typ.	Max.	Note
Internal reference voltage	VCIR	V	TBD	2.50	TBD	

Power Supply Voltage Range

Table 42 Power Supply Voltage Range (Ta=-40C ~ +85C, GND=AGND=0V)

Item	Symbol	Unit	Min.	Typ.	Max.	Condition
Power supply voltage	IOVCC	V	1.65	1.80/2.80	3.10	-
Power supply voltage	VCC	V	2.50	2.80	3.30	-
Power supply voltage	VCI	V	2.50	2.80	3.30	-
Power supply voltage	VPP1	V	8.9	9.0	9.1	Write
		V	8.9	9.0	9.1	Erase
Power supply voltage	VPP2	V	7.4	7.5	7.6	Write
		V	8.9	9.0	9.1	Erase
Power supply voltage	VPP3A	V	-0.3	0.0	+0.3	Write
		V	-9.1	-9.0	-8.9	Erase

Output Voltage Range

Table 43 Output Voltage Range （Ta=-40C ~ +85C, GND=AGND=0V）

Item	Symbol	Unit	Min.	Typ.	Max.	Condition
Grayscale. VCOM reference voltage	VREG	V	-	-	DDVDH-0.5	-
Source driver		V	GND+0.2	-	VREG	-
VCOMH output	VCOMH	V	-	-	VREG	-
VCOML output	VCOML	V	VCL+0.5	-	-	-
VCOM amplitude		V	-	-	6.0	-
Step-up output voltage	VLOUT1	V	4.5	-	6.0	-
Step-up output voltage	VLOUT2	V	10.0	-	18.0	-
Step-up output voltage	VLOUT3	V	-13.5	-	-4.5	-
Step-up output voltage	VCL	V	-3.0	-	-1.9	-
Voltage between VCI and VCL		V	-	-	6.0	-
Voltage between VGH and VGL		V	-	-	28.0	-

AC Characteristics

(VCC= 2.50V ~ 3.30V, IOVCC=1.65V ~ 3.10V, Ta=-40C ~ +85C Note 1)

Clock Characteristics

Table 44 Clock Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.
RC oscillation clock	fosc	kHz	IOVCC=VCC=2.8V, 25C	630	678	725

DBI TypeB (18-/19-bit, 8-/9-bit) Timing Characteristics

Table 45 1- / 3/2- Transfer, Normal Write mode (HWM=0), High Speed Write mode (HWM=1), IOVCC=1.65V ~ 3.10V (Target Spec)

Item	Symbol		Unit	Test Condition	Min.	Max.
Address setup time	DCX	tast	ns		0	-
Address hold time (Write/Read)		taht	ns		10	-
Chip select setup time (Write)	CSX	tcs	ns		20	-
Chip select setup time (Read)		trcs	ns		170	-
Chip select wait time (Write/Read)		tcsf	ns		20	-
Write cycle time (Normal Write / High-speed write)	WRX	twc	ns		100/80	-
Write control pulse ”High” period		twrh	ns		35	-
Write control pulse ”Low” period		twrl	ns		35	-
Read cycle time	RDX	trc	ns		450	-
Read control pulse ”High” period		trdh	ns		250	-
Read control pulse ”Low” period		trdl	ns		170	-
Write data setup time	DB[17:0]	twds	ns	CL Max.30pF Min.8pF	15	-
Write data hold time		twdh	ns		25	-
Read access time		tracc	ns		10	340
Output disable time		trod	ns		10	-
Rise / Fall time	-	tr/tf	ns		-	15

Table 46 2- / 3- Transfer, Normal write mode (HWM=0) / High-speed write mode (HWM=1), IOVCC=1.65V ~ 3.10V) (Target Spec)

Item	Symbol		Unit	Test condition	Min..	Max.
Address setup time	DCX	tast	ns		0	-
Address hold time (Write/Read)		taht	ns		10	-
Chip select setup time (Write)	CSX	tcs	ns		20	-
Chip select setup time (Read)		trcs	ns		170	-
Chip select wait time (Write/Read)		tcsf	ns		20	-
Write cycle time (Normal write/ High-speed write)	WRX	twc	ns		80 / 50	-
Write control pulse"High" period (Normal/ High-speed)		twrh	ns		35 / 20	-
Write control pulse"Low" period (Normal/ High-speed)		twrl	ns		35 / 20	-
Read cycle time	RDX	trc	ns		450	-
Read control pulse "High" period		trdh	ns		250	-
Read control pulse "Low" period		trdl	ns		170	-
Write data setup time	DB[17:0]	twds	ns	CL Max.30pF Min.8pF	15	-
Write data hold time		twdh	ns		25	-
Read access time		tracc	ns		10	340
Output disable time		trod	ns		10	-
Rise / Fall time	-	tr/tf	ns		-	15

Note: 1 transfer: (1)16bit-I/F 16bit/pixel, (2)18bit-I/F 18bit/pixel
3/2- transfer: (1)16bit-I/F 18bit/pixel Option1
2 transfer: (1)8bit-I/F 16bit/pixel, (2) 9bit-I/F 18bit/pixel
3 transfer: (1)8bit-I/F 18bit/pixel, (2)18bit-I/F 18bit/pixel Option2

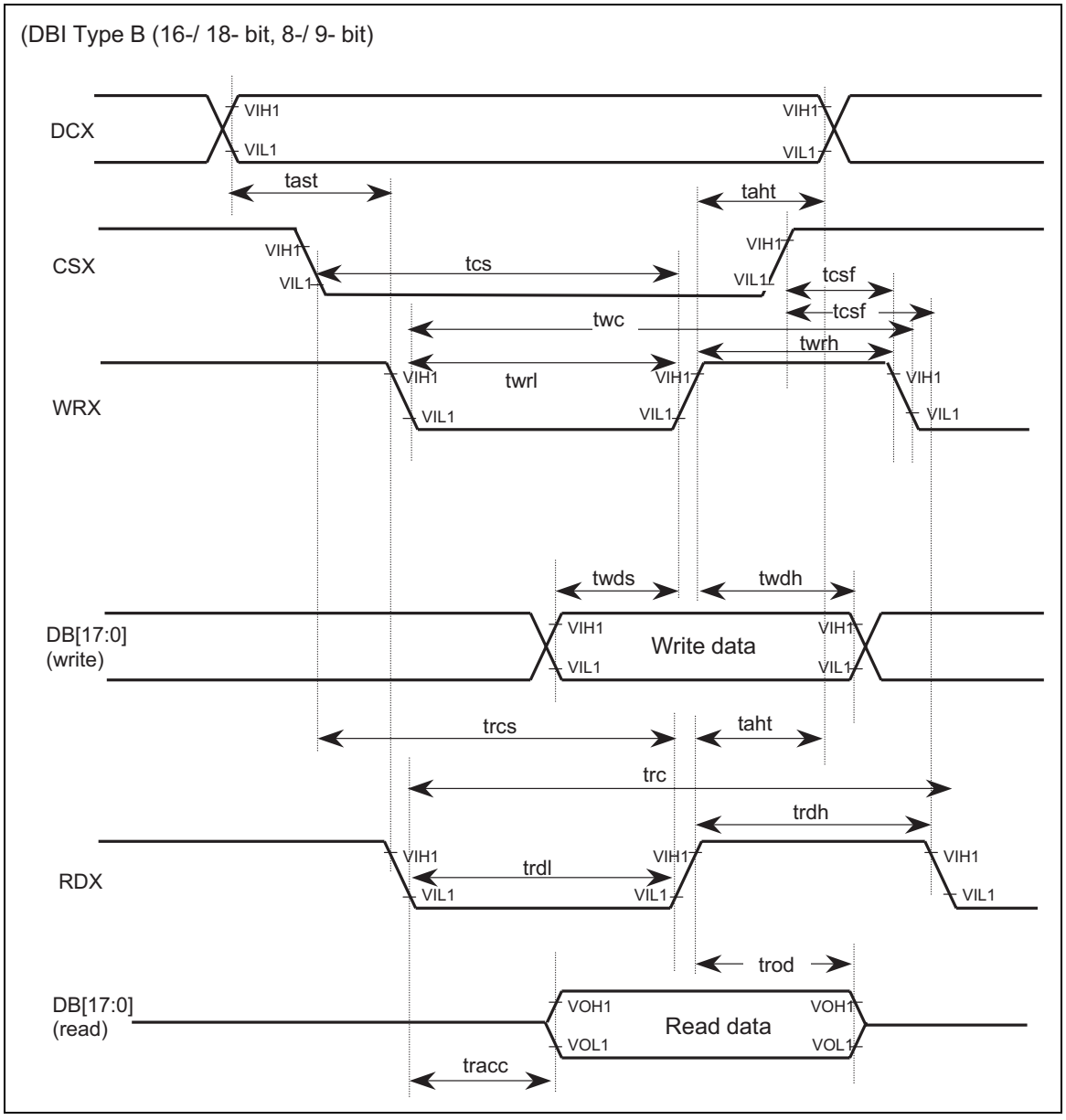


Figure A DBI Type B (16-/ 18- bit, 8-/9- bit timing) Bus Timing

Note 1: Logic High and Low levels of input signals are defined as follows:

RESX: IOVCC x 10%, 90%

Other than RESX: IOVCC x 20%, 80%

Note 2: Unused DB[17:0] pins shall be fixed at “IOVCC” or “GND”.

DBI TypeC Timing Characteristics

Table 47 IOVCC=1.65V ~ 3.10V (Target Spec)

Item	Symbol		Unit	Test Condition	Min..	Max.
Chip Select Setup Time (Write)	CSX	tcss	ns		40	-
Chip Select Setup Time (Read)		tcsh	ns		40	-
Address Setup Time	DCX	tas	ns		10	-
Address Hold Time (Write/Read)		tah	ns		10	-
Write Cycle Time	SCL (Write)	twc	ns		100	-
SCL "High" period (Write)		trdh	ns		40	-
SCL "Low" period (Write)		trdl	ns		40	-
Read Cycle Time	SCL (Read)	trc	ns		150	-
SCL "High" period (Write)		trdh	ns		60	-
SCL "Low" period (Write)		trdl	ns		60	-
Data Setup Time	DIN	tds	ns		30	-
Data Hold Time		tdh	ns		30	-
Access Time	DOUT	tacc	ns	CL Max.30pF Min.8pF	-	100
Output Disable Time		tod	ns		10	-
Rise/ Fall Time	-	tr/tf	ns		-	15

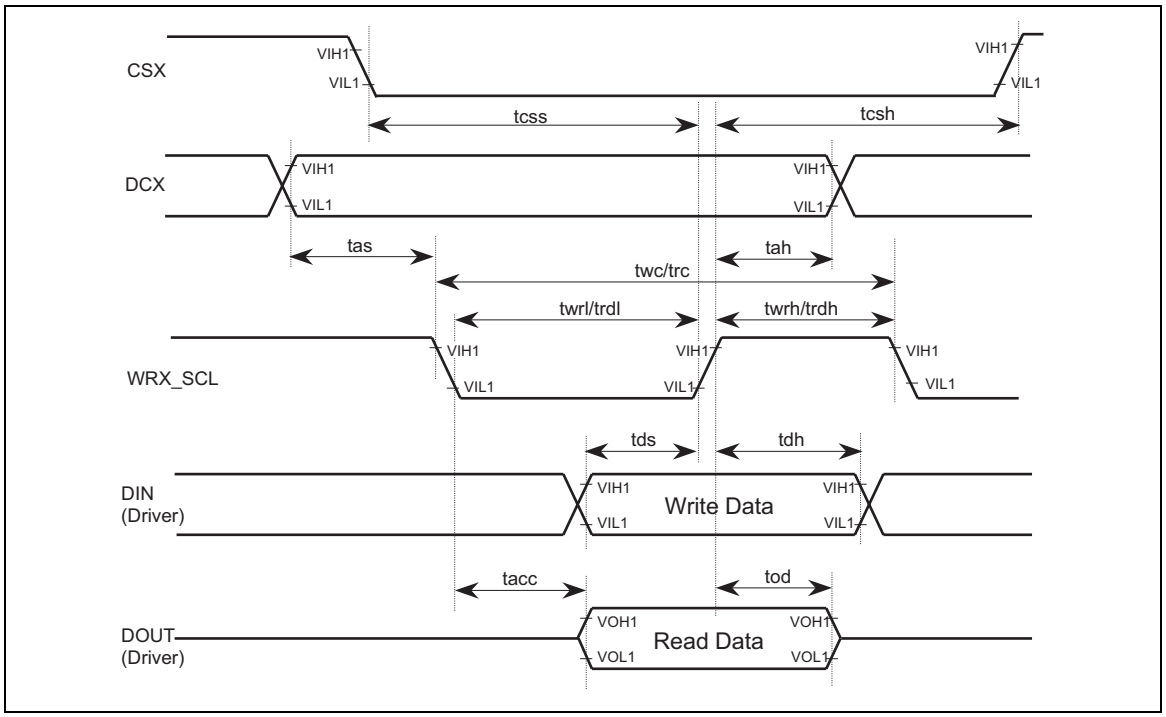


Figure B DBI Type C Timing

DPI Timing Charateristics

Table 48 IOVCC=1.65V ~ 3.10V (Target Spec)

Item	Symbol		Unit	Test condition	Min..	Max.
VSYNC Setup Time	VSYNC	tvss	ns		30	-
VSYNC Hold Time		tvsh	ns		30	-
HSYNC Setup Time	HSYNC	thss	ns		30	-
HSYNC Hold Time		thsh	ns		30	-
Pixel Clock Cycle Time	PCLK	tpclkcyc	ns		100	-
Pixel Clock ”Low” period		tpclkl	ns		30	-
Pixel Clock ”High” period		tpclkh	ns		30	-
Data Setup Time	DB[17:0] or DB[15:0] DE	tds	ns		30	-
Data Hold Time		tdh	ns		30	-
Rise / Fall Time	-	tr/tf	ns		-	15

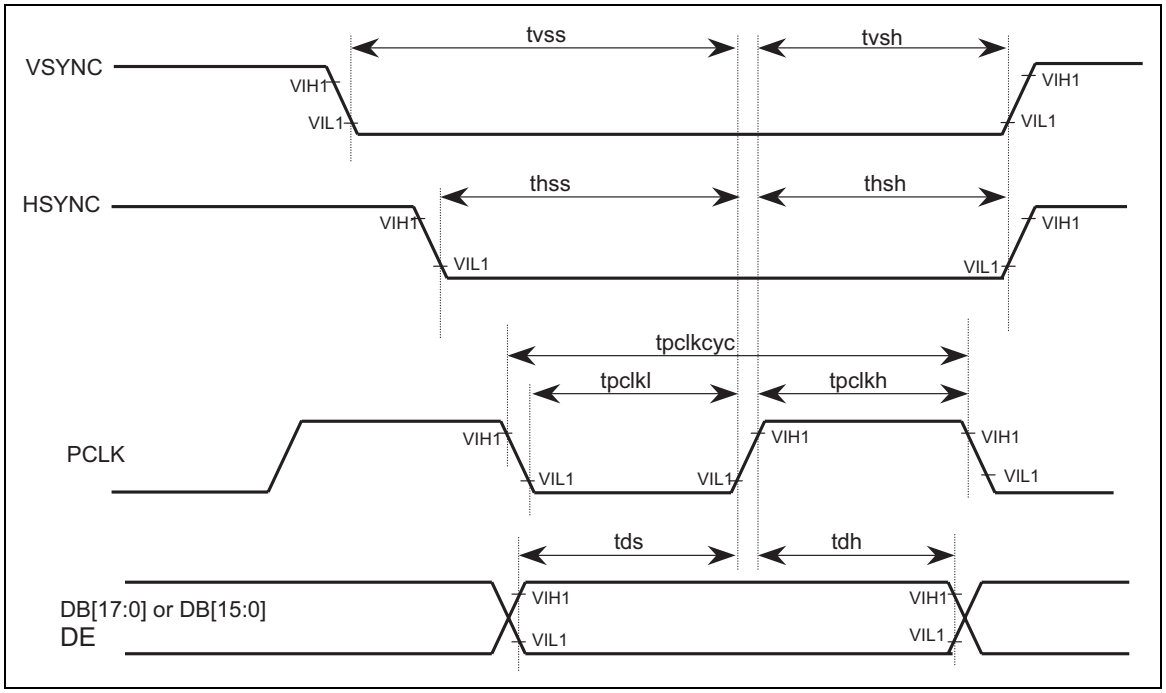


Figure C DPI Timing

Reset Timing Characteristics

Table 49 Reset Timing Characteristics (VCC= 2.5V ~ 3.3V, IOVCC=1.65V ~ 3.10V, Ta=-40℃ ~ +85℃)

Item	Symbol	Unit	Test Condition	Min.	Max.
Reset ”Low” level width	tRW	us	Power On	10	—
Reset Time	tRT	ms		—	5

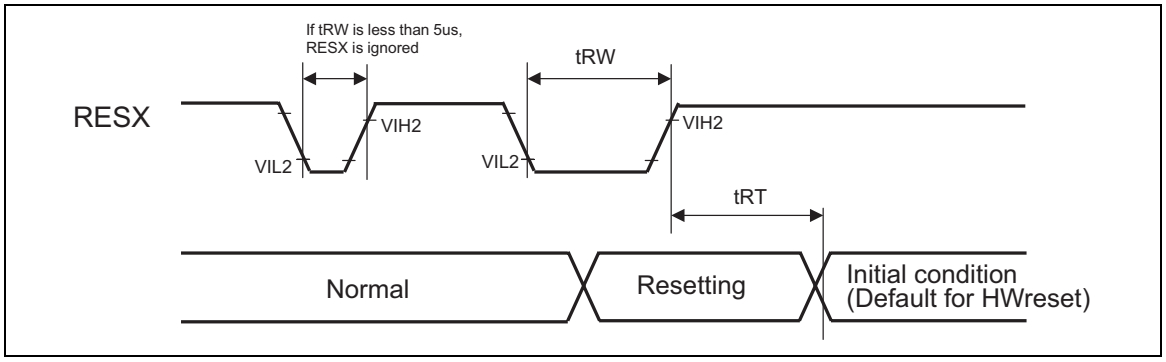


Figure D Reset Timing

Liquid Crystal Driver Output Characteristics

Table 50 Liquid Crystl Driver Output Characteristics (Target Spec)

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
VCOM Output Delay Time	tddv	us	IOVCC=1.80V, VCC=VCI=2.80V, Ta=25C, REV=0, BC0=0, FP0=5, BP0=8, VC=3'h1, BT=3'h4, VRH=5'h1D, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h5, DC10=3'h2, Time to reach +/- 35mV from VCOM polarity inversion timing, load resistance R=100ohm, load capacitance C=20nF	-	25	—	8
Source Driver Output Delay Time	tdds	Us	IOVCC=1.80V, VCC=VCI=2.80V, Ta=25C, REV=0, BC0=0, FP0=5, BP0=8, VC=3'h1, BT=3'h4, VRH=5'h1D, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h5, DC10=3'h2, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0 PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2) Same change from same grayscale at all time-division source output pins. Time to reach +/- 35mV from VCOM polarity inversion timing. Load resistance R=10kohm, Load capacitance C=30pF	-	25	—	9

Note: LCD driver output delay time depends on on load on the liquid crystal panel. Therefore, frame frequency and one line cycle needs to be specified checking image quality on the panel to be used.

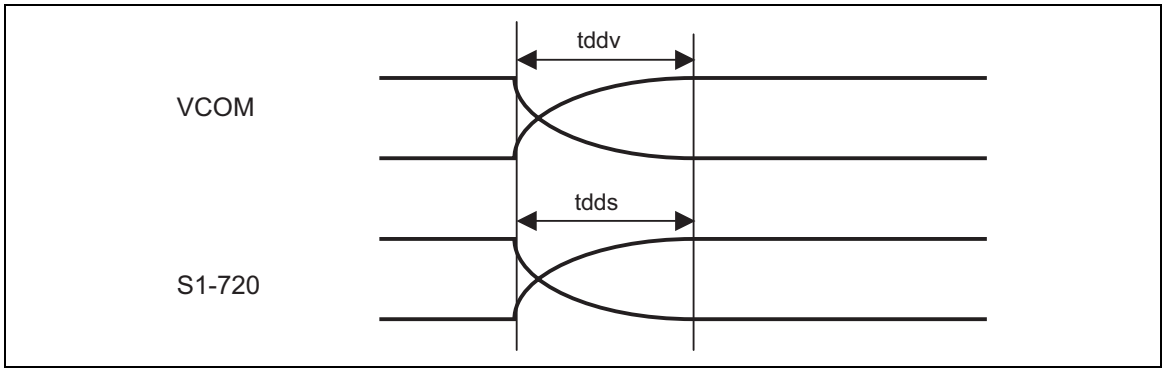


Figure E Liquid Crystl Driver Output Timing

EEPROM Interface Timing

Table 51 EEPROM Interface Timing VCC= 2.5V ~ 3.3V, Ta=-40℃ ~ +85℃)

Item	Symbol	Unit	Test Condition	Min.	Max.
SCS Setup Time	tCSS	ns	Figure F	1200	-
SCS Hold Time	tCSH	ns	Figure F	600	-
SCS Deselect Time	tCDS	ns	Figure F	1200	-
Data Setup Time	tDS	ns	Figure F	600	-
Data Hold Time	tDH	ns	Figure F	600	-
Output Delay Time	tPD	ns	Figure F	-	1200
Clock Frequency	fSCL	kHz	Figure F	-	725
SCL Clock ”L” Time	tSCLL	ns	Figure F	350	-
SCL Clock ”H” Time	tSCLH	ns	Figure F	350	-

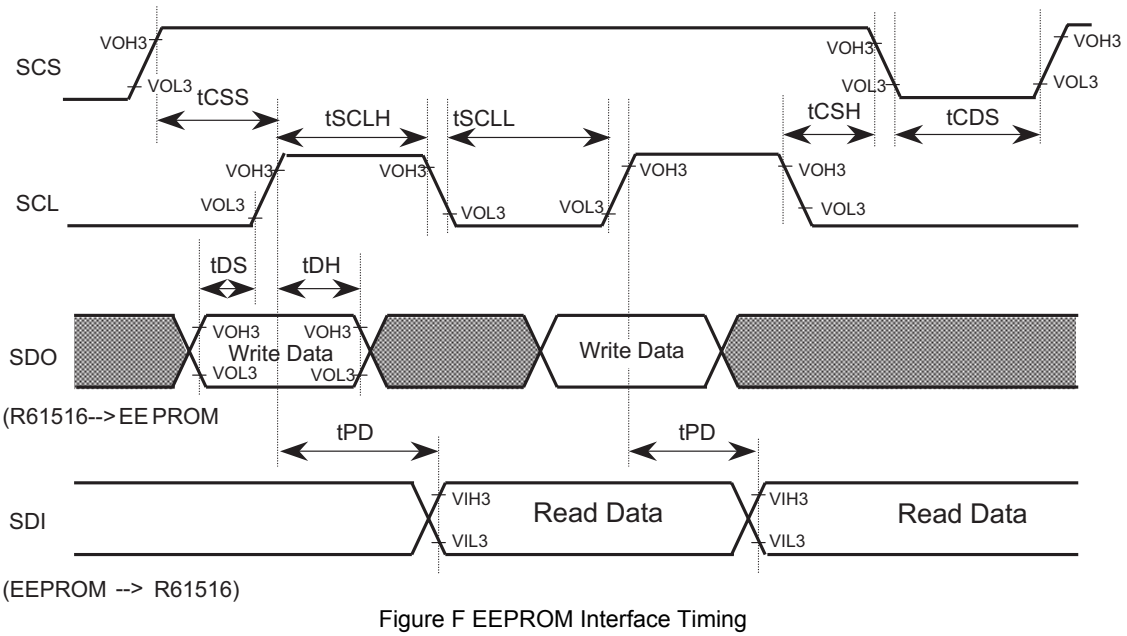


Figure F EEPROM Interface Timing

Note: Logic High and Low levels of input signals are defined as VCC x 80% and 20% respectively.

Notes on Electrical Characteristics

Note 1: DC/AC electrical characteristics of bare die and wafer area guaranteed at +85C.

Note 2: The following figures illustrate the configurations of input, I/O, and output pins.

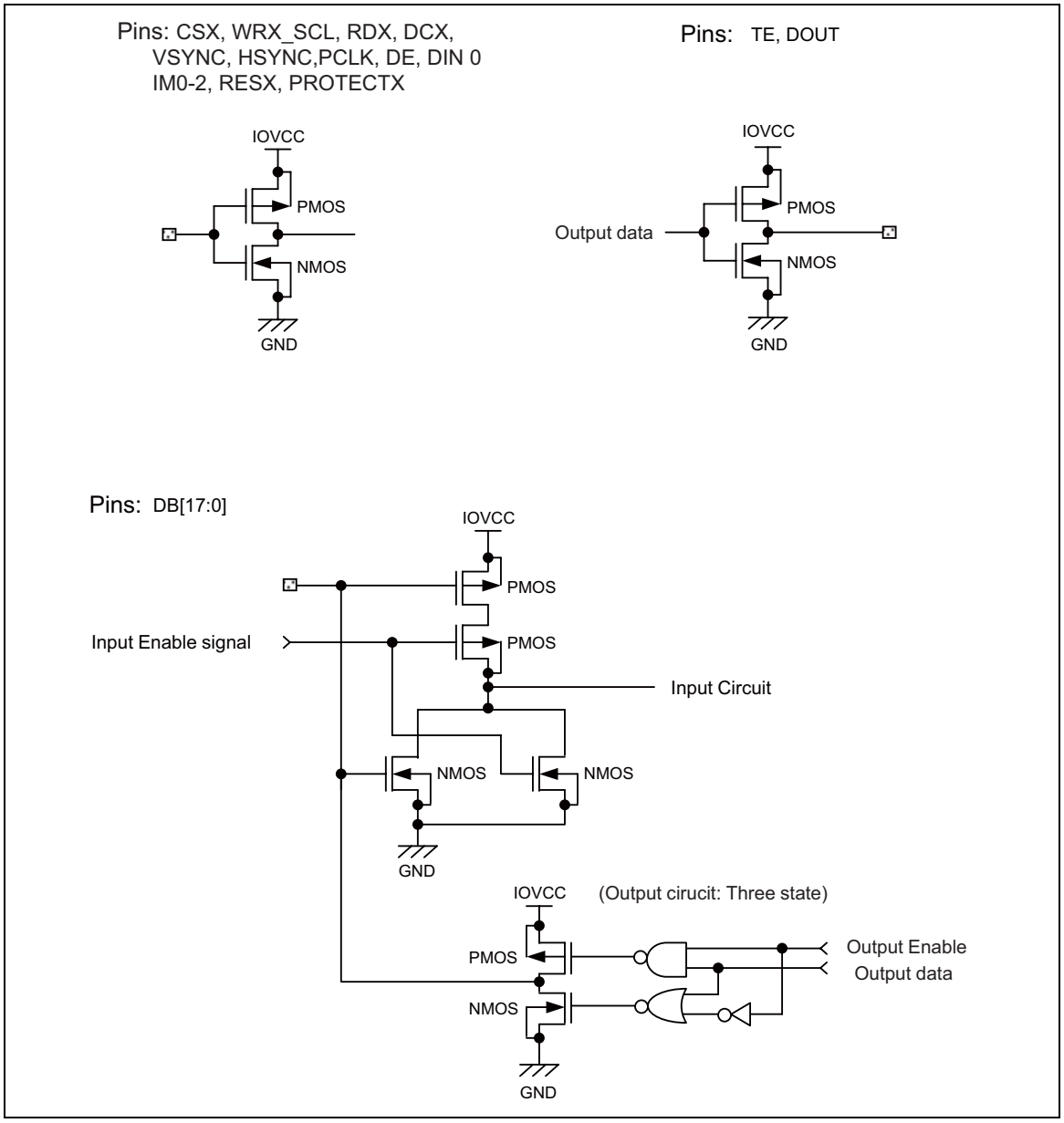


Figure 69

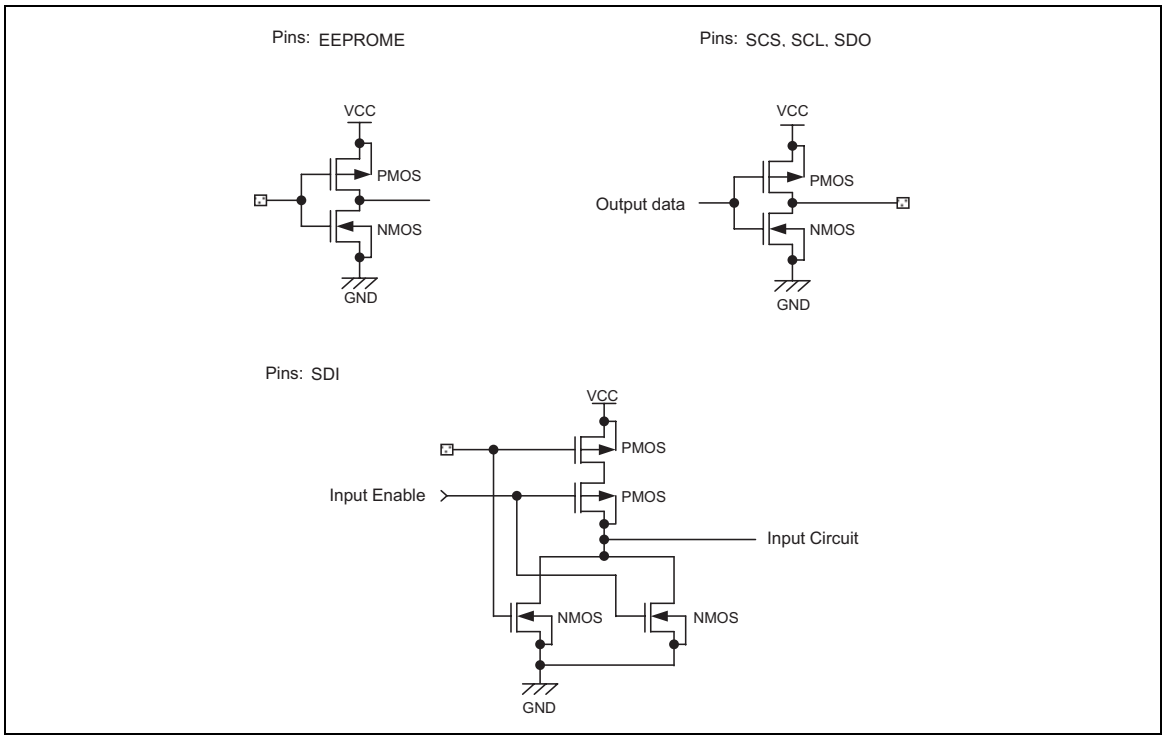


Figure 70

Note 3: Fix pins as follows: TEST1-5 to ground (GND), VREFC, VDDTEST and TSC to ground (GND), IM0-2 to IOVCC or ground (GND), VPP1-2 to VCC, VPP3 to ground (GND). This excludes the current in the output drove MOS.

Note 4: This excludes the current in the input/output units. Make sure that the input level is fixed because through current will increase in the input circuit when the CMOS input level takes a middle range level. The current consumption is unaffected by whether the CS* pin is "high" or "low" while not accessing via interface pins.

Note 5: This is average current value.

Note 6: The output voltage deviation is the difference in the voltages between output pins that are placed side by side in same display mode. The output voltage deviation is reference value.

Note 7: The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for one chip with same display data.

Note 8: This applie to operation of the internal oscillator when internal RC oscillator is used.

Note 9: VCOM output delay time depends on load on the liquid crystal panel. Therefore, frame frequency and one line cycle needs to be specified checking image quality on the panel to be used.

Note 10: LCD driver output delay time depends on on load on the liquid crystal panel. Therefore, frame frequency and one line cycle needs to be specified checking image quality on the panel to be used.

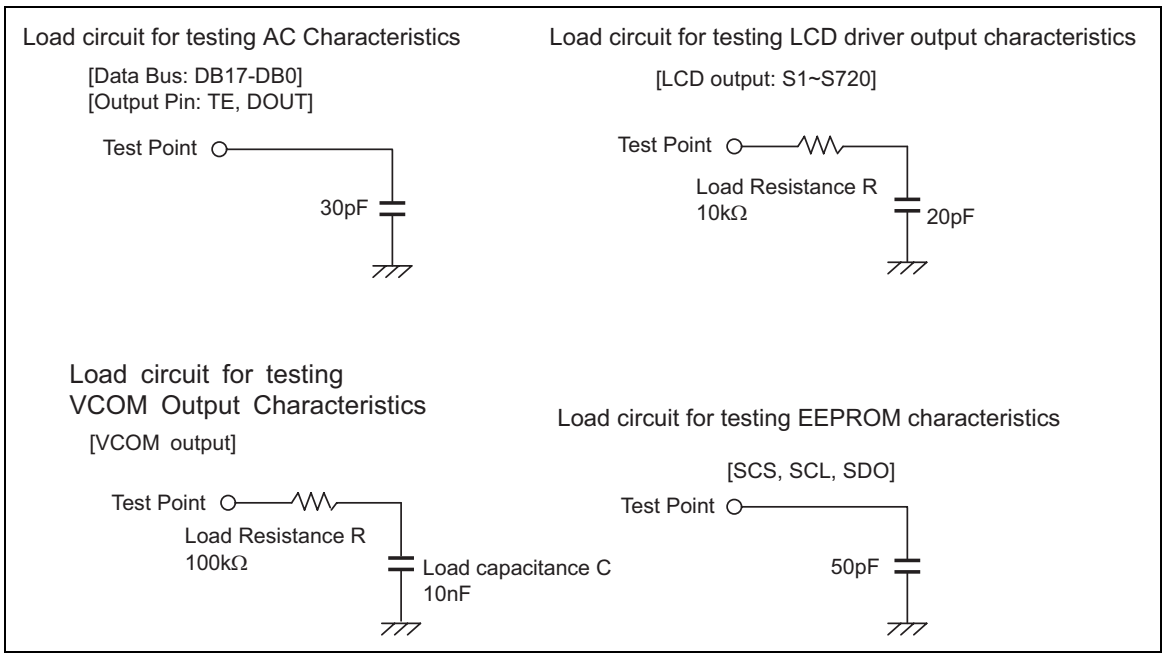


Figure G Test Circuits

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Colophon .1.0

Revision Record

Rev.	Date	Page No	Contents of Modification	Drawn by	Approved by
0.02	2007/04/10		First issue		
0.03	2007/07/11	All pages	Microcomputer, MPU, MCU, host → Host Processor		
		All pages	GRAM, RAM → frame memory		
		All pages	IOVCC=1.65 - 3.0V → 1.65 - 3.10V		
		All pages	Moving picture → video image		
		6	Description revised.		
		6	Features: Type C 3-line 8bit, 4-line 9bit serial → 4-line 9bit (Option 1), 8 bit (Option 3)		
		8	Table 1 Editorial error corrected.		
		9	Block Diagram: Deleted “3-line serial” (system interface). VCI1, VCL output→input/output. Add VCOMOL, VCOMOR, VPP1, VPP2, VPP3A, VPP3B and VPP3C pins.		
		16	Table 7 VCL: I→ I/O		
		10	Block Function 1. Interface→ System Interface. MIPI DBI TypeC (3/4-line) → (Option 1, 3). Table 2: DBI TypeC 3-lines(Option1) → DBI TypeC 9bit (Option1), DBI TypeC 4-lines(Option3)→ DBI Type C 8bit (Option 3).		
		11	(b) MIPI DBI Type C (3-/4- lines) → MIPI DBI Type C (Option 1, 3). 3-/ 4- line serial interface → 9bit (Option 1) and 8bit (Option 3) serial interface. Added “The R61516 supports synchronous signal TE for video image. Images are updated without causing flicker on the panel by writing display data in synchronization with this TE signal.”		
			2. External Display Interface : TE interface deleted.		
		13	Pin Function, Table 4: VPP1, VPP2, VPP3A Unused pin OPEN → AGND		
			Note 1, 2 added.		
		14	Table 5 Bus Interface → Table 5 Bus Interface (Amplitude: IOVCC ~ GND). CSX Added “Make sure to connect to host processor. Follow AC timing to control the signal.”. IM0-2 Type C (3-/ 4- line) → Type C (Option 1 / Option 3)		
		15	Table 6 External EEPROM interface → Table 6 External EEPROM interface (Amplitude: VCC-GND)		
		17	Table 8: Added VCOMOL and VCOMOR pins.		
		18	Changed VGLDMY 1-4 description.		
			VPP3B, 3C: Leave open → Connect to AGND. Unused OPEN → -		
		19	Pad arrangement (rev0.02) added.		
		20	Alignment mark: Coordinates specified.		
		21-29	Pad coordinates added.		
		30	Bump arrangement: VCOML/R added		

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	32	Title: Command → System Interface (Display Bus Interface, DBI)		
		Figure 4 added.		
	38	Data Transfer Mode: Two methods are available for writing data to the frame memory in the R61516; 16-bit color/pixel or 18-bit color/pixel. → Two methods are available for writing data to the frame memory in the R61516.		
	39-46	"DBI Type C interface", "DBI data format" inserted.		
	47-54	"Display Pixel Interface (DPI)", "DPI Data Format" inserted.		
	31-35 in rev0.02	"RAM access" Deleted.		
	57	Command list (Manufacturer Command) B1h: W→ W/R, E0h: 1→ 2		
	59	Note: Command may be written → Command may be accessed		
	61	Note: Command may be written → Command may be accessed		
	63	Error correction 44h STS[9:0] → [8:0]		
	65	B3h 4th parameter: EPF added.		
	66	C1h, C2h, C3h: Error correction. DIVx[1:0] = 2'h0 → 2'h1.		
		D0h 2nd parameter: Deleted VCLE, VGLE. 3rd parameter: 8'h9F → 8'hDF.		
		D2h, D3h, D4h: Error correction. DC1x[2:0]= 3'h0 → 3'h2, DC0x [2:0]=3'h0 → 3'h5		
	69	soft_reset (01h) description, restriction rewritten. Figure in Restriction deleted.		
	74	get_pixel_format (0Ch), Description: Bit D[6:4] – DPI Pixel Format (RGB Interface Color Format) → Bit D[6:4] – DPI Pixel Format (RGB Interface Color Format Selection). Note changed.		
	81	enter_sleep_mode (10h) Restriction rewritten. Figure deleted.		
	82	exit_sleep_mode (11h): Description rewritten. Figure deleted.		
	84	enter_partial_mode (12h), Restriction: Added "This command causes scrolling function disabled."		
	87	enter_invert_mode (21h) Description, Figure: Color changed		
	101	set_scroll_area (33h): Description, figures: Error correction: VFA → VSA		
	106	Set_tear_on (35h): Restriction figure: Error correction. (TE output off → TE output on. M→ TELOM.		
	118	set_tear_scanline (44h): STS[9] deleted. Restriction: Added "Make sure that STS [8:0] ≤ NL (number of line) +		

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		1."		
	120	read_DDB_start (A1h) Flow chart: Error correction.		
	121	read_DDB_continue (A8h): binary code corrected.		
	123	Low Power Mode Control (B1h): DSTB description "See Deep Standby Mode EXIT Sequence in Power Supply Setting Sequence" → "See Deep Standby Mode IN/EXIT Sequence in "State and Command Sequence"."		
		Flow chart: Error correction.		
	124-126	Frame Memory Access and Interface setting (B3h) HWM description: Note 2 added. EPE [1:0] added. RIM bit table: Error correction.		
	136	PCDIVH/PCDIVL description: Setting example deleted. "See "Display Pixel Interface" for details in setting." added.		
	137	Display Timing Setting for Idle Mode (C3h) binary code: Error correction.		
	140-141	Display Timing Setting (C1h-C3h) FPn[7:0], BPn[7:0] table changed. Rrestriction: FP ≥ 2 lines → FP ≥ 3 lines.		
	143	Source/VCOM/Gate Driving Timing Setting (C4h) MCP bit: the source output changing position→ the VCOM output changing position		
	151	Power Setting (Common Setting) (D0h): VCLE, VGLE deleted.		
	157-158	Power Setting (D2h – D4h): DC1x, DC0x Table changed. Calculation $2^{(N+1)}$ → 2^N (DC1x), 2^N → $2^{(N-1)}$ (DC0x).		
	159	Waveform figure inserted.		
	161	NV Memory Access Control (E0h) NVAD table: 3'h3 (LS byte)→ 3'h2 (LS byte)		
	164	EEPROM Write Enable (E8h) Description: "This command is used to enable write to and erase from the EEPROM." → "This command is used to enable write to the EEPROM."		
	165	EEPROM Write Disable (E9h) Description: "This command is used to disable write to and erase from the EEPROM." → "This command is used to disable write to the EEPROM."		
	169	State Transition Diagram: CS x 6 → CS x 1 (to cancel deep standby mode). DPI operation added.		
	170-172	State and Command Sequence inserted.		
	173	Reset: Table 22(INPUT/OUTPUT Pin Initial State) VCIOUT deleted. VCOMOL / VCOMOR added.		
	174-178	"EEPROM Serial Interface" inserted.		
	179-181	"EEPROM Data Load Function" inserted.		
	188	Table 25 changed.		
	192-194	"High Speed Frame Memory Write Function" inserted.		

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	195-196	"Self-diagnostic Functions" inserted.		
	199	I.2 C0h → C1h		
	203	TE waveform (44h): Error correction. Restriction added.		
	206	Liquid Crystal Panel Interface Timing: Note 2 added.		
	207	Figure 58: Waveform changed. Note added.		
	209	γ Correction Registers: I. 2 which is determined by GammaSet A setting → which is determined by the red bit. Table 28: Error correction.		
	210	Table 29: Error correction.		
	211	Table 30: Error correction. Table 31: Error correction.		
	212	Table 32: Error correction.		
	213	Table 33: Note changed.		
	214	Error correction. (Source output level → Grayscale Voltage)		
	215	Power supply circuit connection example 1: Diode connection changed. Note 2 added.		
	216	Power supply circuit connection example 2: Diode connection changed. Note 2 added.		
	217	Table 36 (Shottky diode) Changed. Note 1 to Table 37 added.		
	218	Figure 62 Voltage Setting Pattern Diagram: Voltage values deleted. Note 1: Deleted "Make sure that output voltage levels in operation do not conflict with the following conditions: (DDVDH – VREG) > 0.5V, (VCOM – VCL) > 0.5V. Also make sure VGH-VGL ≤ 28V, VCI-VCL ≤ 6V." Note 2 deleted.		
	183-184 (in rev0.02)	"Power Supply Setting Sequences" deleted.		
	219	"NVM Control" description added.		
	220	Description added. Figure 64 NVM Read Data Sequence: Wait 1ms → Wait 1ms or more.		
	221-222	NVM Write Sequence revised.		
	223-224	NVM Erase Sequence revised.		
	226-228	Table 39 (DC characteristics): Items added. Symbols corrected. Test conditions changed. Min. and Max. values changed. Note 5 added.		
	229	Table 40 (Step-up Circuit Characteristics) Test condition changed.		
	230	Table 42 (Power Supply Voltage Range), Table 43 (Output Voltage Range) added.		
	231	Table 44 (Clock Characteristics) Test condition changed.		
		Table 45 (DBI Type B Timing Characteristics) Items, Min. and Max. values changed and added.		
	232	Table 46 (DBI Type B Timing Characteristics) Items, Min.		

Rev.	Date	Page No	Contents of Modification	Drawn by	Approved by
			and Max. values changed and added.		
		233	Figure A (DBI Type B timing): Error correction. VIH→ VIH1, VIL→ VIL1, VOH→ VOH1, VOL→ VOL1. Note 1 Other than RESX: IOVCC x 30%, 70% → Other than RESX: IOVCC x 20%, 80%		
		234	Figure B (DBI Type C timing): Error correction. VIH→ VIH1, VIL→ VIL1, VOH→VOH1, VOL→ VOL1. SCL→ WRX_SCL.		
		235	Table 48 Vsync → VSYNC, Hsync→ HSYNC. Min. values changed. Figure C (DPI timing) Error correction. VIH→ VIH1, VIL→ VIL1, VOH→VOH1, VOL→ VOL1.		
		236	Figure D (Reset Timing) VIL2, VIH2 added.		
		237	Table 50 (Liquid Crystal Driver Output Characteristics) Test condition changed.		
		238	Table 51 (EEPROM Interface) Min., Max. values changed.		
			Figure F (EEPROM Interface) Error correction. VIH→VOH3, VIL→ VOL3		
0.04	2007/07/12	151	Power Setting (D0h): Error correction. 3rd parameter's DB6 bit "0" → "1"		
		230	Table 43 Error correction. (DDVDH→ VLOUT3, VGH → VLOUT2, VGL → VLOUT3)		