

SED1520 Series

Dot Matrix LCD Controller Driver

- Ultra Low Power Consumption
- Built-in Video RAM

■ DESCRIPTION

The SED1520 family of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.

The drivers are available in two configurations

The SED1520 family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.

These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

- The SED1520 which is able to drive two lines of twelve characters each.
- The SED1521 which is able to drive 80 segments for extension.
- The SED1522 which is able to drive one line of thirteen characters each.

■ FEATURES

- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- Many command set
- Total 80 (segment + common) drive sets
- Low power — 30 μ W at 2 kHz external clock
- Wide range of supply voltages
 - V_{DD} – V_{SS}: –2.4 to –7.0 V
 - V_{DD} – V₅: –3.5 to –13.0 V
- Low-power CMOS

■ LINE-UP

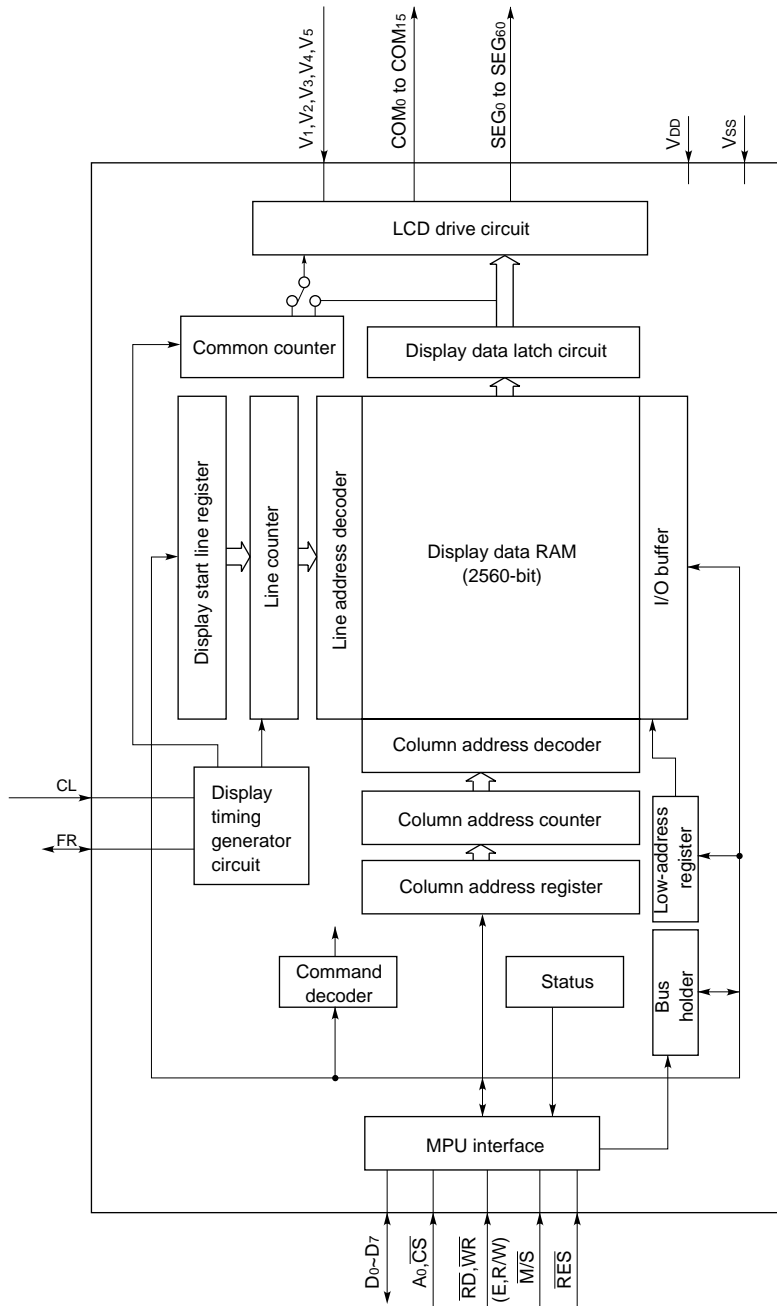
Product Name	Clock Frequency		Applicable Driver	Number of SEG Drivers	Number of CMOS Drivers	Duty
	On-Chip	External				
SED1520*0*	18 kHz	18 kHz	SED1520*0*, SED1521*0*	61	16	1/16, 1/32
SED1521*0*	—	18 kHz	SED1520*0*, SED1522*0*	80	0	1/8 to 1/32
SED1522*0*	18 kHz	18 kHz	SED1522*0*, SED1521*0*	69	8	1/8, 1/16
SED1520*A*	—	2 kHz	SED1520*A*, SED1521*A*	61	16	1/16, 1/32
SED1521*A*	—	2 kHz	SED1520*A*, SED1522*A*	80	0	1/8 to 1/32
SED1522*A*	—	2 kHz	SED1522*A*, SED1521*A*	69	8	1/8, 1/16

- Package code (For example SED1520)
 - SED1520T
 - SED1520F** : PKG
 - └ QFP5-100pin (plastic): SED1520F*A
 - └ QFP15-100pin (plastic): SED1520F*C
 - SED1520D** : Die form
 - └ Al pad: SED1520D*A
 - └ Au bump: SED1520D*B

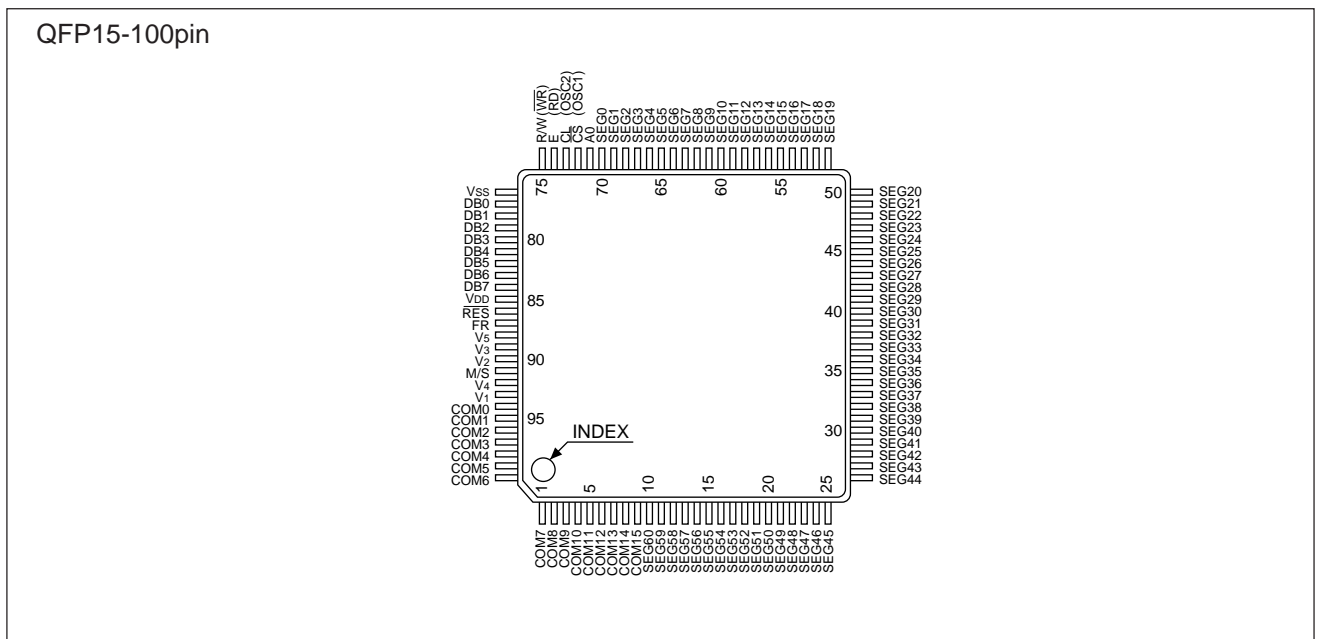
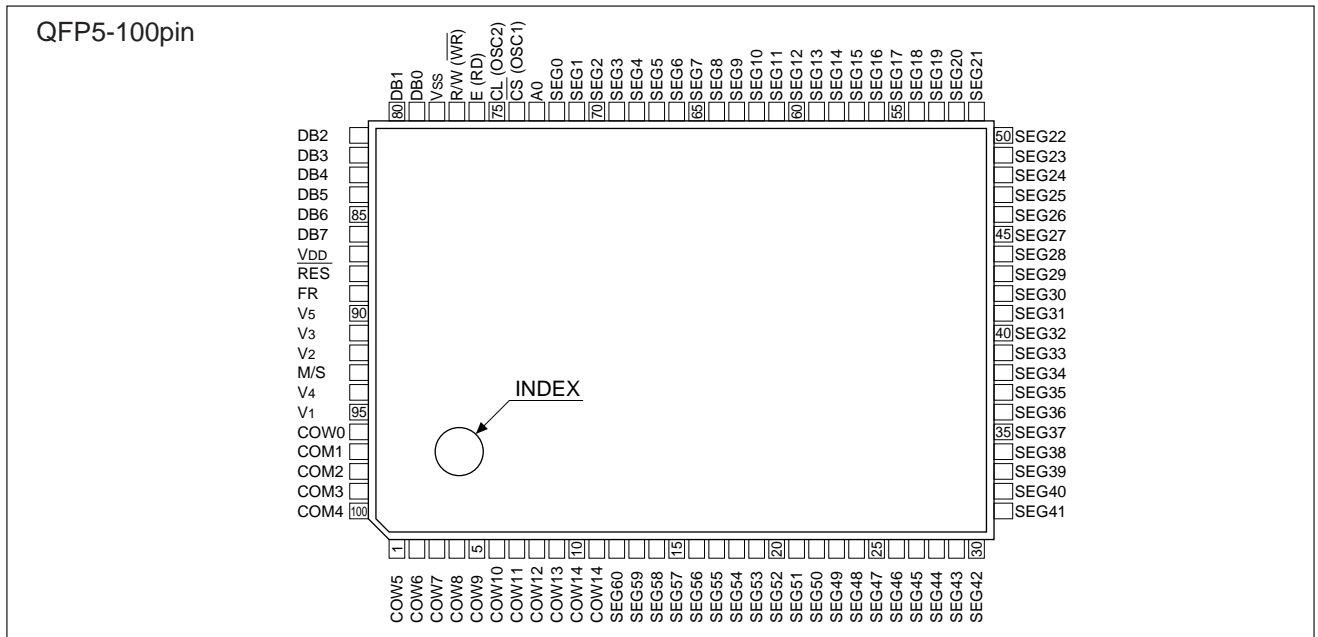
SED1520 Series

■ BLOCK DIAGRAM

An example of SED1520*AA:



PACKAGE CONFIGURATION



Note: This is an example of SED1520F pin assignment. The modified pin names are given below.

Product Name	Pin/Pad Number					
	74	75	96 to 100, 1 to 11	93	94	95
SED1520F0A	OSC1	OSC2	COM0 to COM15*	M/S	V4	V1
SED1521F0A	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
SED1522F0A	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V4	V1
SED1520FAA	CS	CL	COM0 to COM15*	M/S	V4	V1
SED1521FAA	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
SED1522FAA	CS	CL	COM0 to 7, SEG68 to 61	M/S	V4	V1

SED1520: Common outputs COM0 to COM15 of the master LSI correspond to COM31 to COM16 of the slave LSI.

SED1522: Common outputs COM0 to COM15 of the master LSI correspond to COM15 to COM8 of the slave LSI.

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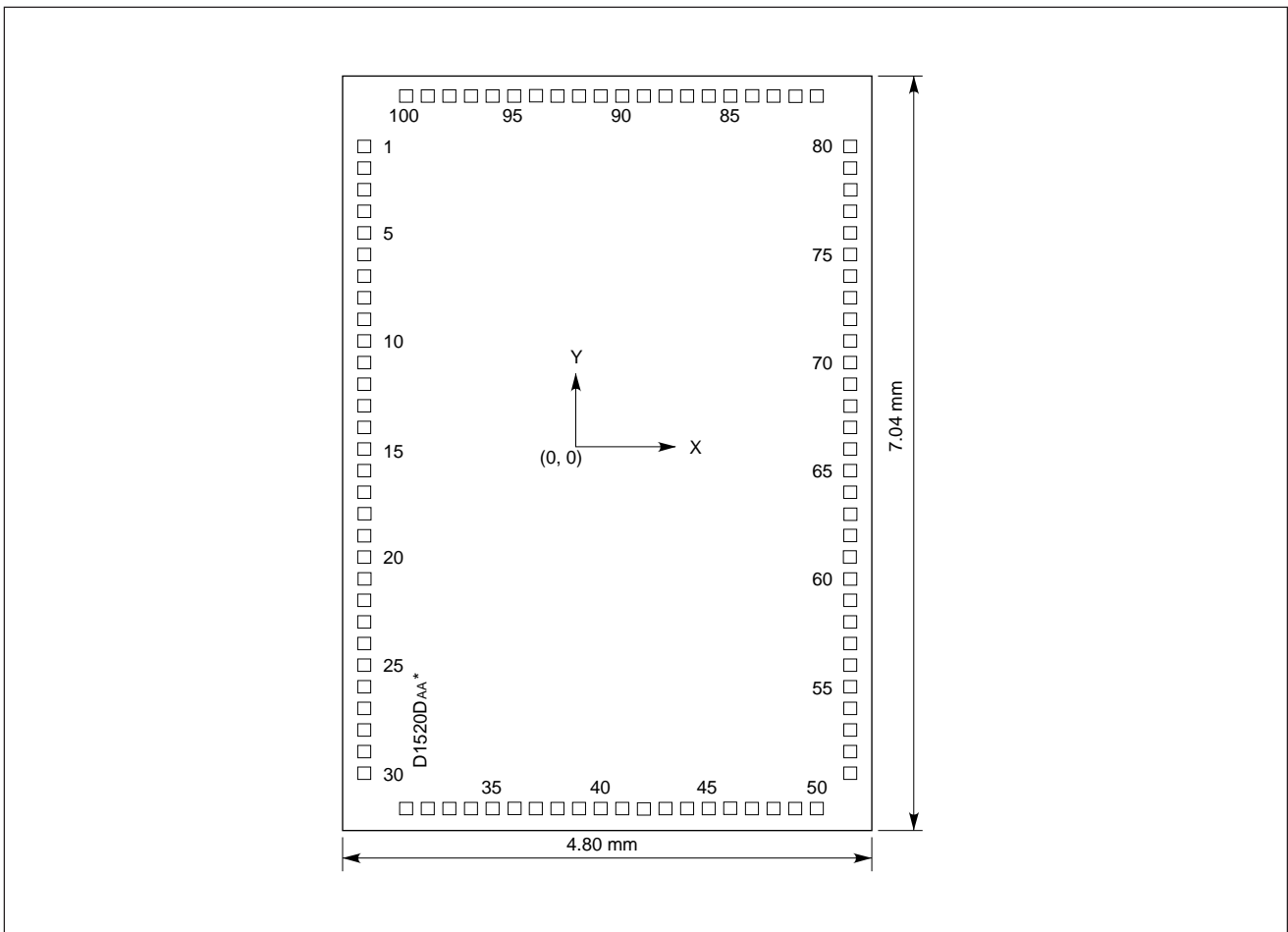
■ PAD LAYOUT

Chip specifications of AL pad package

Chip size: 4.80×7.04×0.400 mm
Pad pitch: 100×100 μm

Chip specifications of gold bump package

Chip size: 4.80×7.04×0.525 mm
Bump pitch: 199 μm (Min.)
Bump height: 22.5 μm (Typ.)
Bump size: 132×111 μm (±20 μm) for mushroom model
116×92 μm (±4 μm) for vertical model



Note: An example of SED1520DAA die numbers is given. These numbers are the same as the bump package.

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■ PAD ARRANGEMENT

An example of SED1520DA* pin names is given. The asterisk (*) can be A for AL pad package or B for gold bump package.

SED1520DAB Pad Center Coordinates

Pad No.	Pin Name	X	Y	Pad No.	Pin Name	X	Y	Pad No.	Pin Name	X	Y
1	COM5	159	6507	35	SEG37	1302	159	69	SEG3	4641	4148
2	COM6	159	6308	36	SEG36	1502	159	70	SEG2	4641	4347
3	COM7	159	6108	37	SEG35	1701	159	71	SEG1	4641	4547
4	COM8	159	5909	38	SEG34	1901	159	72	SEG0	4641	4789
5	COM9	159	5709	39	SEG33	2100	159	73	A0	4641	5048
6	COM10	159	5510	40	SEG32	2300	159	74	CS	4641	5247
7	COM11	159	5310	41	SEG31	2499	159	75	CL	4641	5447
8	COM12	159	5111	42	SEG30	2699	159	76	E (RD)	4641	5646
9	COM13	159	4911	43	SEG29	2898	159	77	R/W (WR)	4641	5846
10	COM14	159	4712	44	SEG28	3098	159	78	Vss	4641	6107
11	COM15	159	4512	45	SEG27	3297	159	79	DB0	4641	6307
12	SEG60	159	4169	46	SEG26	3497	159	80	DB1	4641	6506
13	SEG59	159	3969	47	SEG25	3696	159	81	DB2	4295	6884
14	SEG58	159	3770	48	SEG24	3896	159	82	DB3	4095	6884
15	SEG57	159	3570	49	SEG23	4095	159	83	DB4	3896	6884
16	SEG56	159	3371	50	SEG22	4295	159	84	DB5	3696	6884
17	SEG55	159	3075	51	SEG21	4641	482	85	DB6	3497	6884
18	SEG54	159	2876	52	SEG20	4641	681	86	DB7	3297	6884
19	SEG53	159	2676	53	SEG19	4641	881	87	VDD	3098	6884
20	SEG52	159	2477	54	SEG18	4641	1080	88	RES	2898	6884
21	SEG51	159	2277	55	SEG17	4641	1280	89	FR	2699	6884
22	SEG50	159	2078	56	SEG16	4641	1479	90	V5	2499	6884
23	SEG49	159	1878	57	SEG15	4641	1679	91	V3	2300	6884
24	SEG48	159	1679	58	SEG14	4641	1878	92	V2	2100	6884
25	SEG47	159	1479	59	SEG13	4641	2078	93	M/S	1901	6884
26	SEG46	159	1280	60	SEG12	4641	2277	94	V4	1701	6884
27	SEG45	159	1080	61	SEG11	4641	2477	95	V1	1502	6884
28	SEG44	159	881	62	SEG10	4641	2676	96	COM0	1302	6884
29	SEG43	159	681	63	SEG9	4641	2876	97	COM1	1103	6884
30	SEG42	159	482	64	SEG8	4641	3075	98	COM2	903	6884
31	SEG41	504	159	65	SEG7	4641	3275	99	COM3	704	6884
32	SEG40	704	159	66	SEG6	4641	3474	100	COM4	504	6884
33	SEG39	903	159	67	SEG5	4641	3674				
34	SEG38	1103	159	68	SEG4	4641	3948				

The other SED1520 series packages have the different pin names as shown.

Package/Pad No.	74	75	96 to 100, 1 to 11	93	94	95
SED1520D0*	OSC1	OSC2	COM0 to COM15 *	M/S	V4	V1
SED1522D0*	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V4	V1
SED1522DA*	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V4	V1
SED1521D0*	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
SED1521DA*	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77

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■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage (1)	V _{SS}	-8.0 to +0.3	V
Supply voltage (2)	V ₅	-16.5 to +0.3	V
Supply voltage (3)	V ₁ , V ₄ , V ₂ , V ₃	V ₅ to +0.3	V
Input voltage	V _{IN}	V _{SS} -0.3 to +0.3	V
Output voltage	V _O	V _{SS} -0.3 to +0.3	V
Power dissipation	P _D	250	mW
Operating temperature	T _{opr}	-40 to +85	°C
Storage temperature	T _{stg}	-65 to +150	°C
Soldering temperature time at lead	T _{sol}	260, 10	°C, sec

- Notes:
- All voltages are specified relative to V_{DD} = 0 V.
 - The following relation must be always hold
V_{DD} ≥ V₁ ≥ V₂ ≥ V₃ ≥ V₄ ≥ V₅
 - Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
 - Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

● DC Characteristics

(T_a = -20 to 75 °C, V_{DD} = 0 V unless stated otherwise)

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pin	
Operating voltage (1) *1.	Recommended	V _{SS}		-5.5	-5.0	-4.5	V	V _{SS}	
	Allowable			-7.0	—	-2.4			
Operating voltage (2)	Recommended	V ₅		-13.0	—	-3.5	V	V ₅ *10.	
	Allowable			-13.0	—	—			
	Allowable	V ₁ , V ₂		0.6×V ₅	—	V _{DD}	V	V ₁ , V ₂	
	Allowable	V ₃ , V ₄		V ₅	—	0.4×V ₅	V	V ₃ , V ₄	
High-level input voltage		V _{IHT}		V _{SS} +2.0	—	V _{DD}	V	*2, *3	
		V _{IHC}		0.2×V _{SS}	—	V _{DD}			
		V _{IHT}	V _{SS} = -3 V	0.2×V _{SS}	—	V _{DD}			
		V _{IHC}	V _{SS} = -3 V	0.2×V _{SS}	—	V _{DD}			
Low-level input voltage		V _{ILT}		V _{SS}	—	V _{SS} +0.8	V	*2, *3	
		V _{ILC}		V _{SS}	—	0.8×V _{SS}			
		V _{ILT}	V _{SS} = -3 V	V _{SS}	—	0.85×V _{SS}			
		V _{ILC}	V _{SS} = -3 V	V _{SS}	—	0.8×V _{SS}			
High-level output voltage		V _{OHT}	I _{OH} = -3.0 mA	V _{SS} +2.4	—	—	V	OSC2 *4, *5	
		V _{OHC1}	I _{OH} = -2.0 mA	V _{SS} +2.4	—	—			
		V _{OHC2}	I _{OH} = -120 μA	0.2×V _{SS}	—	—			
		V _{OHT}	V _{SS} = -3 V	I _{OH} = -2 mA	0.2×V _{SS}	—	—	V	*4, *5 OSC2
		V _{OHC1}	V _{SS} = -3 V	I _{OH} = -2 mA	0.2×V _{SS}	—	—		
		V _{OHC2}	V _{SS} = -3 V	I _{OH} = -50 μA	0.2×V _{SS}	—	—		

(continued)

● DC Characteristics (Cont'd)

(Ta = -20 to 75 °C, VDD = 0 V unless stated otherwise)

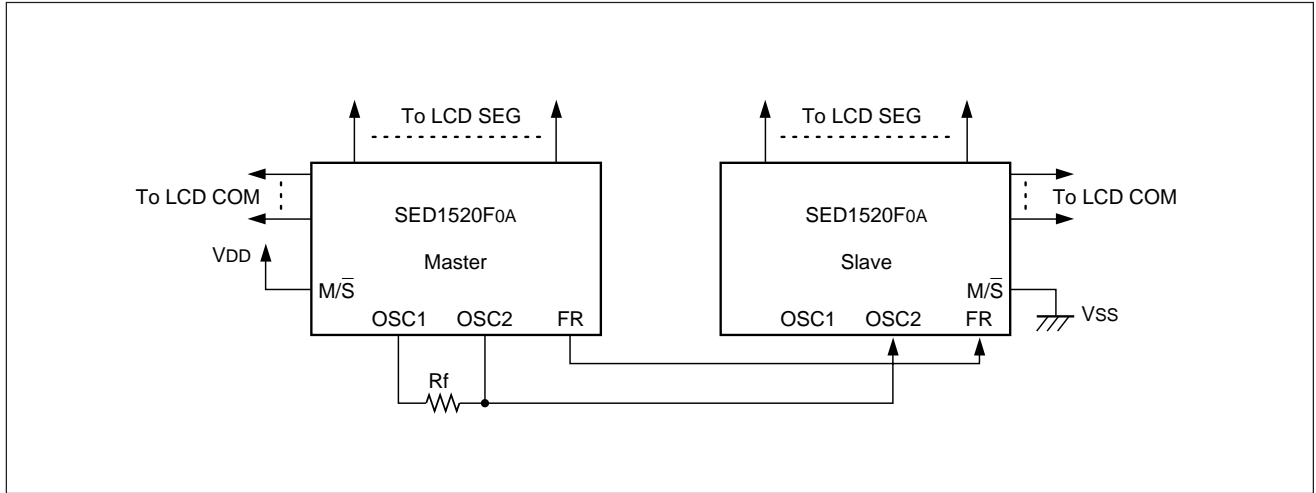
Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable Pin
Low-level output voltage	VOLT	IOL = 3.0 mA		—	—	VSS+0.4	V	OSC2 *4, *5
	VOLC1	IOL = 2.0 mA		—	—	VSS+0.4		
	VOLC2	IOL = 120 μA		—	—	0.8×VSS		
	VOLT	VSS = -3 V	IOL = 2 mA			0.8×VSS	V	*4, *5 OSC2
	VOLC1	VSS = -3 V	IOL = 2 mA			0.8×VSS		
	VOLC2	VSS = -3 V	IOL = 50 μA			0.8×VSS		
Input leakage current	ILI			-1.0	—	1.0	μA	*6
Output leakage current	ILO			-3.0	—	3.0	μA	*7
LCD driver ON resistance	RON	Ta = 25 °C	V5 = -5.0 V	—	5.0	7.5	kΩ	SEG0 to 79, COM0 to 15, *11
			V5 = -3.5 V	—	10.0	50.0		
Static current dissipation	IDDQ	CS = CL = VDD		—	0.05	1.0	μA	VDD
Dynamic current dissipation	IDD (1)	During display V5 = -5.0 V	fCL = 2 kHz	—	2.0	5.0	μA	VDD *12, *13, *14
			Rf = 1 MΩ	—	9.5	15.0		
			fCL = 18 kHz	—	5.0	10.0		
	IDD (2)	During access t _{cy} = 200 kHz VSS = -3V, During access t _{cy} = 200 kHz	fCL = 2 kHz		1.5	4.5	μA	VDD *12, *13
			Rf = 1 MΩ		6.0	12.0		
Input pin capacitance	CIN	Ta = 25 deg. C, f = 1 MHz		—	5.0	8.0	pF	All input pins
				15	18	21		
Oscillation frequency	fOSC	Rf = 1.0 MΩ ±2%, VSS = -5.0 V		15	18	21	kHz	*9
		Rf = 1.0 MΩ ±2%, VSS = -3.0 V		11	16	21		
Reset time	t _R			1.0	—		μS	RES *15

- Notes: *1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
- *2. A0, D0 to D7, E (or \overline{RD}), $\overline{R/W}$ (or \overline{WR}) and \overline{CS}
- *3. CL, FR, $\overline{M/S}$ and \overline{RES}
- *4. D0 to D7
- *5. FR
- *6. A0, E (or \overline{RD}), $\overline{R/W}$ (or \overline{WR}), \overline{CS} , CL, $\overline{M/S}$ and \overline{RES}
- *7. When D0 to D7 and FR are high impedance.
- *8. During continual write access at a frequency of t_{cy}. Current consumption during access is effectively proportional to the access frequency.
- *9. See figure below for details
- *10. See figure below for details
- *11. For a voltage differential of 0.1 V between input (V1, ..., V4) and output (COM, SEG) pins. All voltages within specified operating voltage range.
- *12. SED1520*_A* and SED1521*_A* and SED1522*_A* only. Does not include transient currents due to stray and panel capacitances.
- *13. SED1520*₀* and SED1522*₀* only. Does not include transient currents due to stray and panel capacitances.
- *14. SED1521*₀* only. Does not include transient currents due to stray and panel capacitances.
- *15. t_R (Reset time) represents the time from the RES signal edge to the completion of reset of the internal circuit. Therefore, the SED1520 series enters the normal operation status after this t_R.

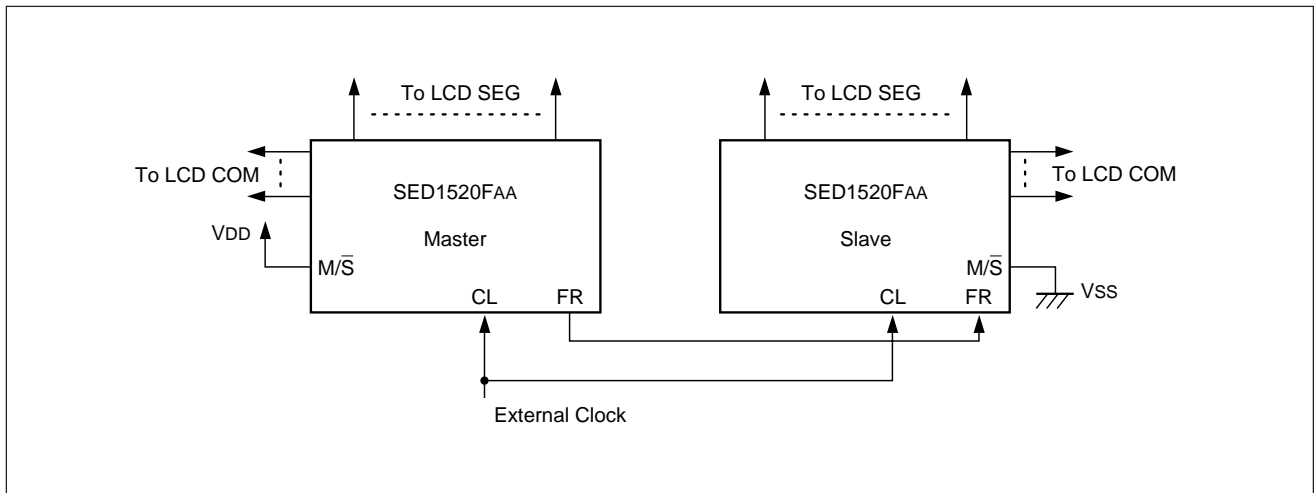
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■ LCD PANEL CONNECTION EXAMPLE

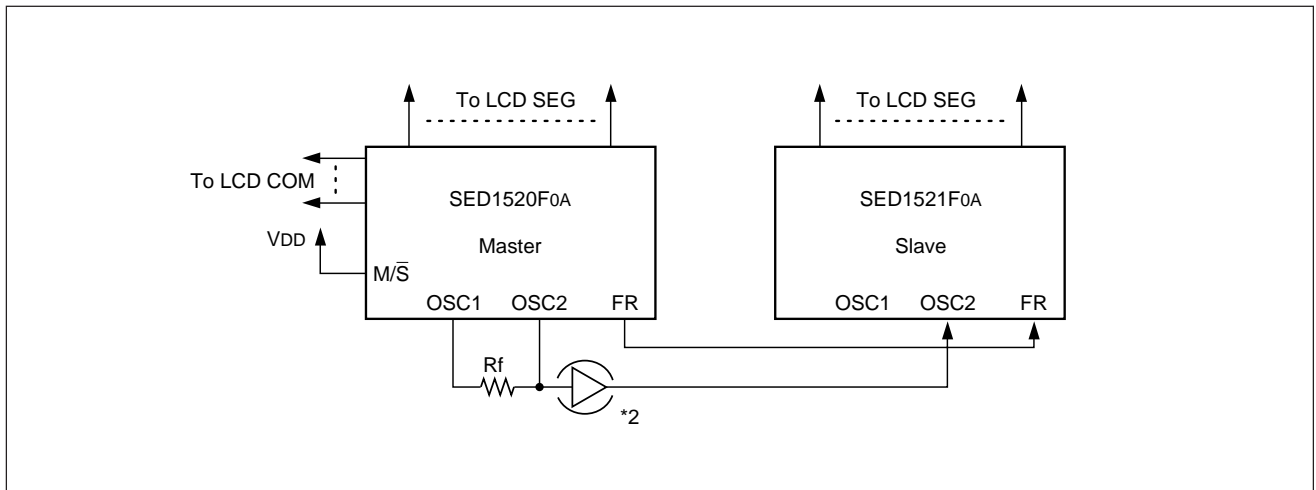
● SED1520F0A–SED1520F0A/SED1522F0A–SED1522F0A



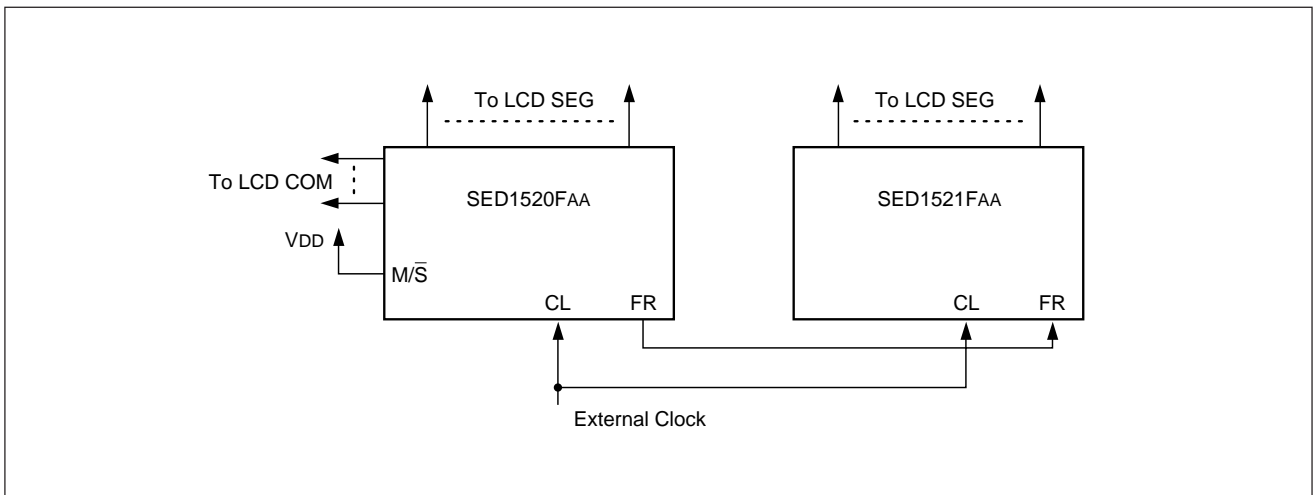
● SED1520FAA–SED1520FAA/SED1522FAA–SED1522FAA



● SED1520F0A/SED1522F0A–SED1521F0A (See note 1)



● SED1520FAA–SED1521FAA



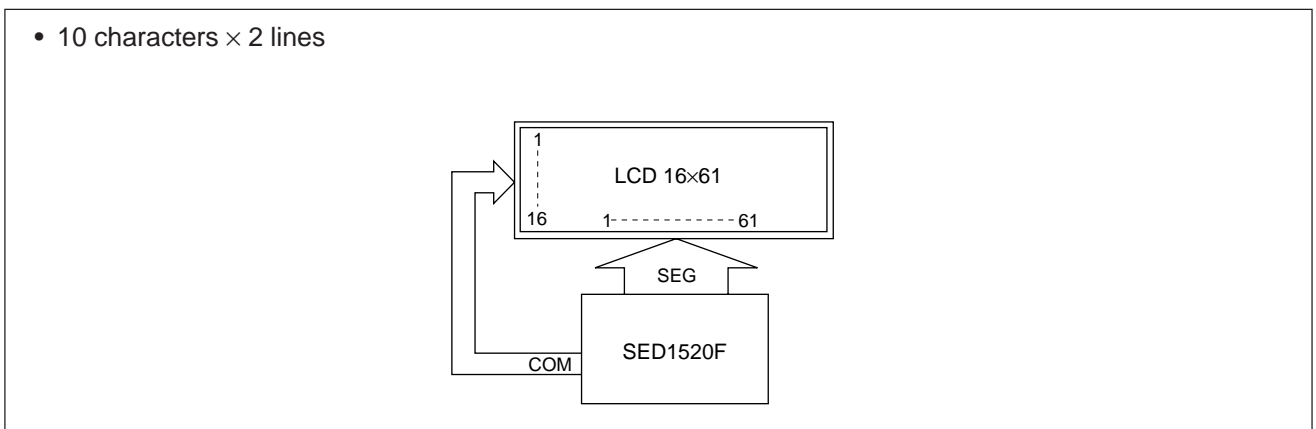
- Notes: 1. The duty cycle of the slave must be the same as that for the master.
2. If a system has two or more slave drivers a CMOS buffer will be required.

■ LCD PANEL CONNECTION EXAMPLE

(The full-dot LCD panel displays a character in 6×8 dots.)

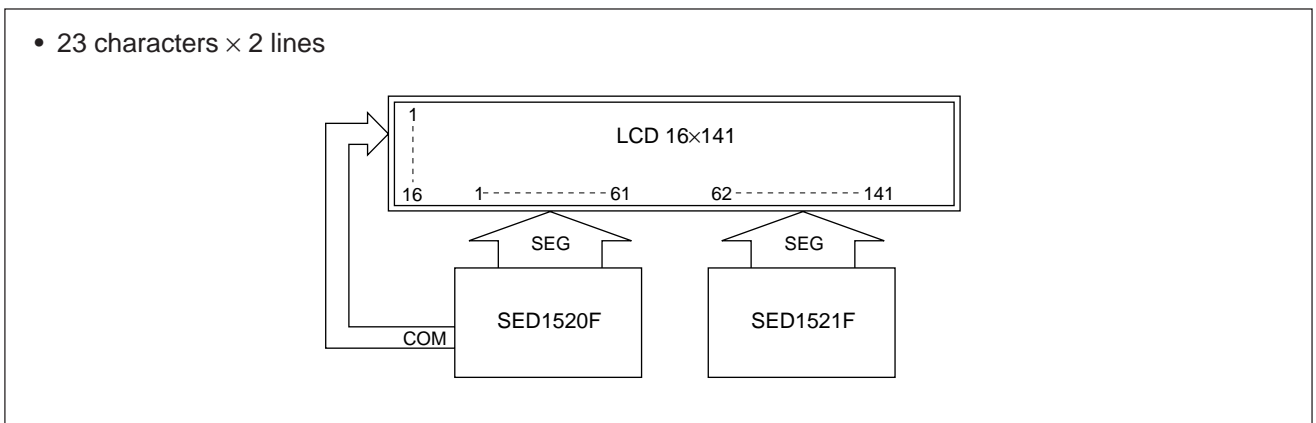
● 1/16 duty:

- 10 characters × 2 lines



● 1/16 duty:

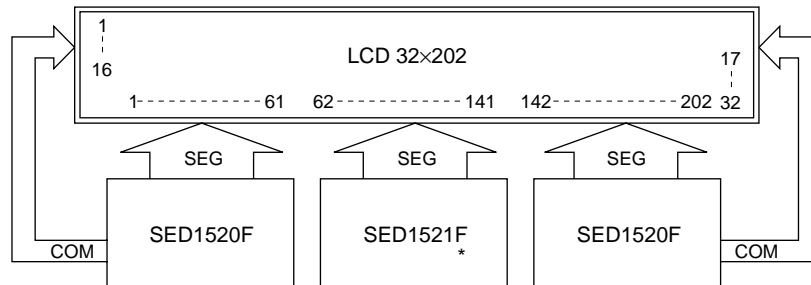
- 23 characters × 2 lines



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● 1/32 duty:

- 33 characters × 4 lines



* The SED1521F can be omitted (the 32×122-dot display mode is selected).

Note: A combination of AB or AA type chip (that uses internal clocks) and 0B or 0A type chip (that uses external clocks) is NOT allowed.

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