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**SPECIFICATION
FOR
LCD MODULE**

**MODULE NO: AMC2002C-I2C
REVISION NO: 00**

Customer's Approval:

| |
|--|
| |
|--|

| | SIGNATURE | DATE |
|---------------------------|-----------|------|
| PREPARED BY (RD ENGINEER) | | |
| CHECKED BY | | |
| APPROVED BY | | |

DOCUMENT REVISION HISTORY:

| DATE | PAGE | DESCRIPTION |
|--------|------|---------------|
| 2013.2 | - | First release |

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1. Module Classification Information

A M C 1 6 0 2 A R - B - B 6 W T D W - S P

1 2 3 4 5 6 7 8 9 10 11 12 13

| | | |
|----|---|--|
| 1 | Brand : ORIENT DISPLAY | |
| 2 | Display Type : C→ Character Type, G→ Graphic Type, NONE→ Custom-made | |
| 3 | Display Font : Characters X Lines / Rows X Columns /Others | |
| 4 | Model serials no. | |
| 5 | RoHS compliant: R→YES NONE→ NO | |
| 6 | IC Package Type: | M→ SMT Type B→ COB Type T→ TAB Type G→ COG Type F→ COF Type S→ Special |
| 7 | LCD Mode: | P→TN Positive N→TN Negative Y→ STN Positive, Yellow Green B→ STN Negative, Blue G→ STN Positive, Gray W→ FSTN Positive T→ FSTN Negative F→ FFSTN Negative S→ Special |
| 8 | Viewing direction | 6→ 6:00, 12→12:00, S→Special |
| 9 | Temperature range | N → Normal Temperature W→ Wide Temperature S→ Special |
| 10 | LCD Polarizer Type | R→ Reflective T→ Transmissive F→ Transflective S→ Special |
| 11 | Backlight Type | N→ None D→ LED E→ EL F→ CCFL S→ Special |
| 12 | Backlight Color | Y→ Yellow-green B→ Blue A→ Amber W→ White G→ Green R→ Red S→ Special |
| 13 | Internal Code | |

2. Precautions in use of LCD Modules

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

3. General Specification

| Item | Dimension | Unit |
|---------------------------------------|----------------------------------|-------------|
| Number of Characters | 20 characters x 2 Lines | — |
| Module dimension (With LED Backlight) | 116.0 x 37.0 x 13.5 (MAX) | mm |
| View area | 83.0 x 18.6 | mm |
| Active area | 73.50 x 11.50 | mm |
| Dot size | 0.60 x 0.65 | mm |
| Dot pitch | 0.65 x 0.70 | mm |
| Character size | 3.20 x 5.55 | mm |
| Character pitch | 3.70 x 5.95 | mm |
| LCD type | STN, Transflective | |
| Duty | 1/16 | |
| View direction | 6 o'clock | |
| Backlight Type | Yellow-green/White LED backlight | |

4. Absolute Maximum Ratings

| Item | | Symbol | Min | Max | Unit |
|--------------------------|-----------------|---------------------------------|---------|---------|------|
| Input Voltage | | V_I | -0.3 | VDD+0.3 | V |
| Supply Voltage For Logic | | VDD-V _{SS} | -0.3 | 5.5 | V |
| Supply Voltage For LCD | | V _{DD} -V ₀ | Vdd-7.0 | Vdd+0.3 | V |
| Wide Temperature LCM | Operating Temp. | Top | -20 | 70 | °C |
| | Storage Temp. | Tstr | -30 | 80 | °C |

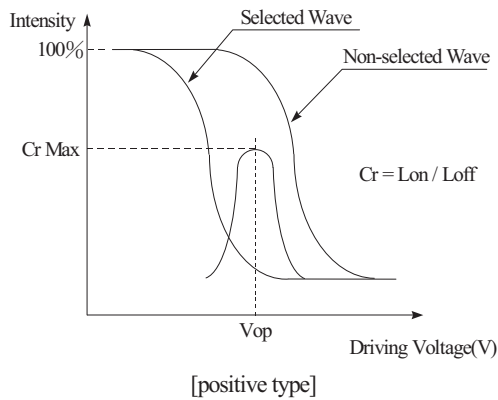
5. Electrical Characteristics

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|--|----------------------------------|---|---------------------|-----|---------------------|------|
| Supply Voltage For Logic | V _{DD} -V _{SS} | — | 4.5 | 5.0 | 5.5 | V |
| Supply Voltage For LCD | V _{DD} -V ₀ | Ta=25°C | 4.2 | 4.7 | 5.3 | V |
| Input High Volt. | V _{IH} | — | 0.7 V _{DD} | — | V _{DD} | V |
| Input Low Volt. | V _{IL} | — | V _{SS} | — | 0.3 V _{DD} | V |
| Supply Current | I _{DD} | V _{DD} =5V | 0.8 | 1.2 | 2.0 | mA |
| Supply Voltage of Yellow-green backlight | V _{LED} | Forward current =210 mA Number of LED die 2x21= 42 | 3.8 | 4.1 | 4.3 | V |
| Supply Voltage of White backlight | V _{LED} | Forward current =60 mA Number of LED die 2x2= 4 | 2.9 | 3.1 | 3.3 | V |

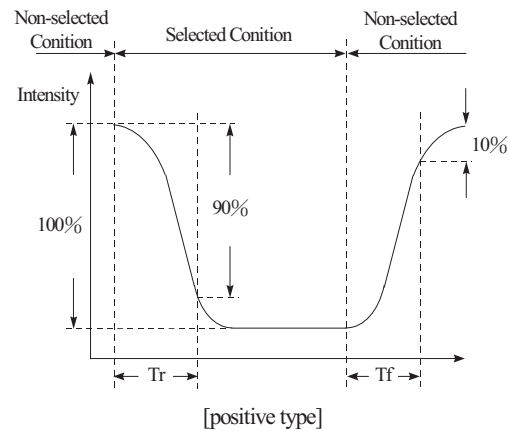
6. Optical Characteristics

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|----------------|---------------|-------------|-----|-----|-----|------|
| View Angle | (V) θ | $CR \geq 2$ | -20 | — | 35 | deg |
| | (H) φ | $CR \geq 2$ | -30 | — | 30 | deg |
| Contrast Ratio | CR | — | — | 3 | — | — |
| Response Time | T rise | — | — | — | 250 | ms |
| | T fall | — | — | — | 250 | ms |

Definition of Operation Voltage (Vop)



Definition of Response Time (Tr, Tf)



Conditions:

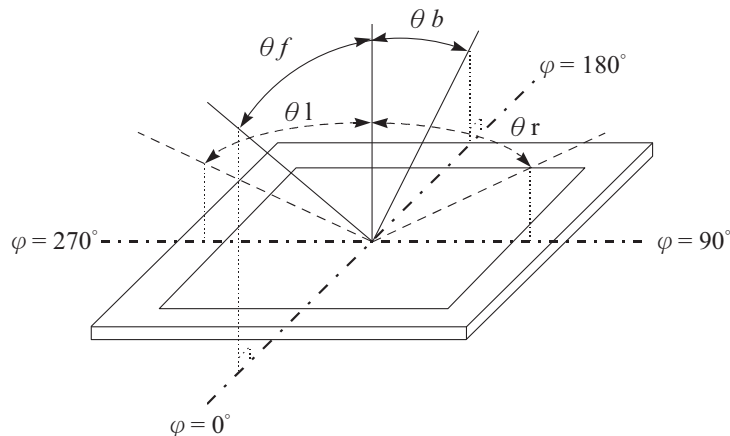
Operating Voltage: Vop

Viewing Angle (θ , φ): 0° , 0°

Frame Frequency: 64 HZ

Driving Waveform: 1/N duty, 1/a bias

Definition of viewing angle ($CR \geq 2$)

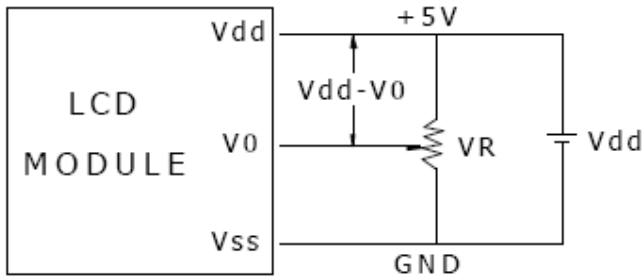


7. Interface Pin Function

| Pin No. | Symbol | Level | Description |
|----------------|-----------------|--------------|---------------------------|
| 1 | LED(+) | | Anode of LED Backlight |
| 2 | LED(-) | | Cathode of LED Backlight |
| 3 | V _{SS} | 0V | Ground |
| 4 | V _{DD} | 5.0V | Supply Voltage for logic |
| 5 | SDA | H/L | Serial Data |
| 6 | SCL | H/L | Serial Clock |
| 7 | V ₀ | (Variable) | Operating voltage for LCD |
| 8 | NC | | No Connection |
| 9 | NC | | No Connection |
| 10 | NC | | No Connection |

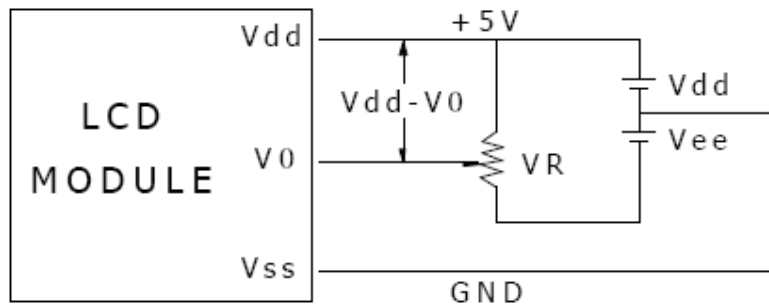
8. Power Supply

SINGLE SUPPLY VOLTAGE TYPE



Vdd-V0: LCD Driving Voltage
VR: 10K - 20K

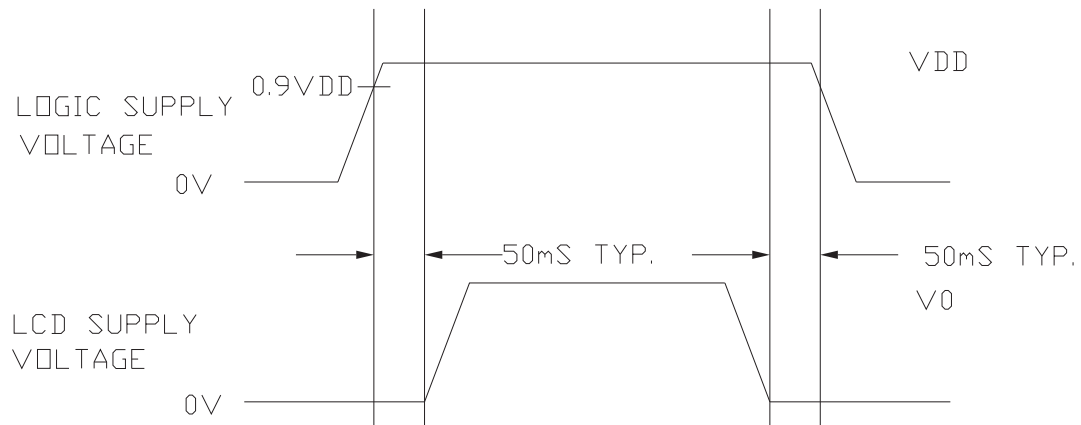
DUAL SUPPLY VOLTAGE TYPE



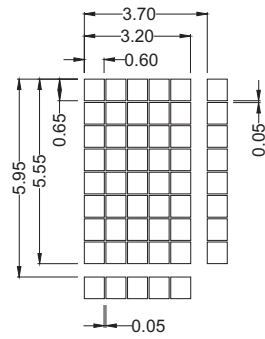
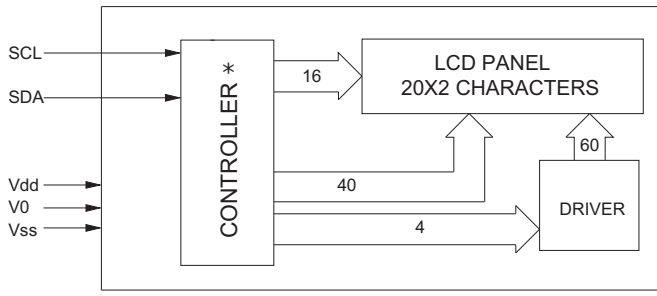
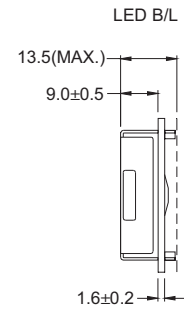
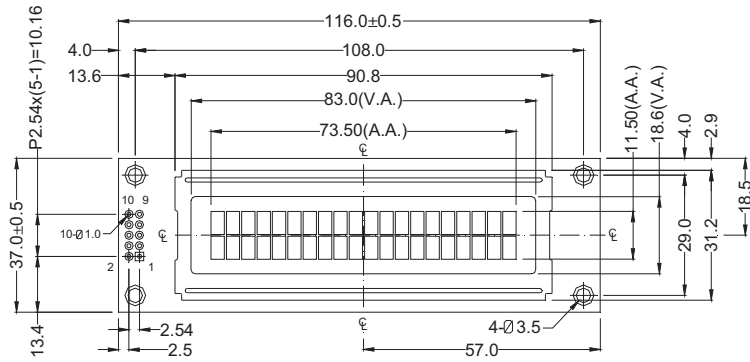
Vdd-V0: LCD Driving Voltage
VR: 10K - 20K

Timing Diagram of VDD Against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.



9. Contour Drawing & Block Diagram



10. Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

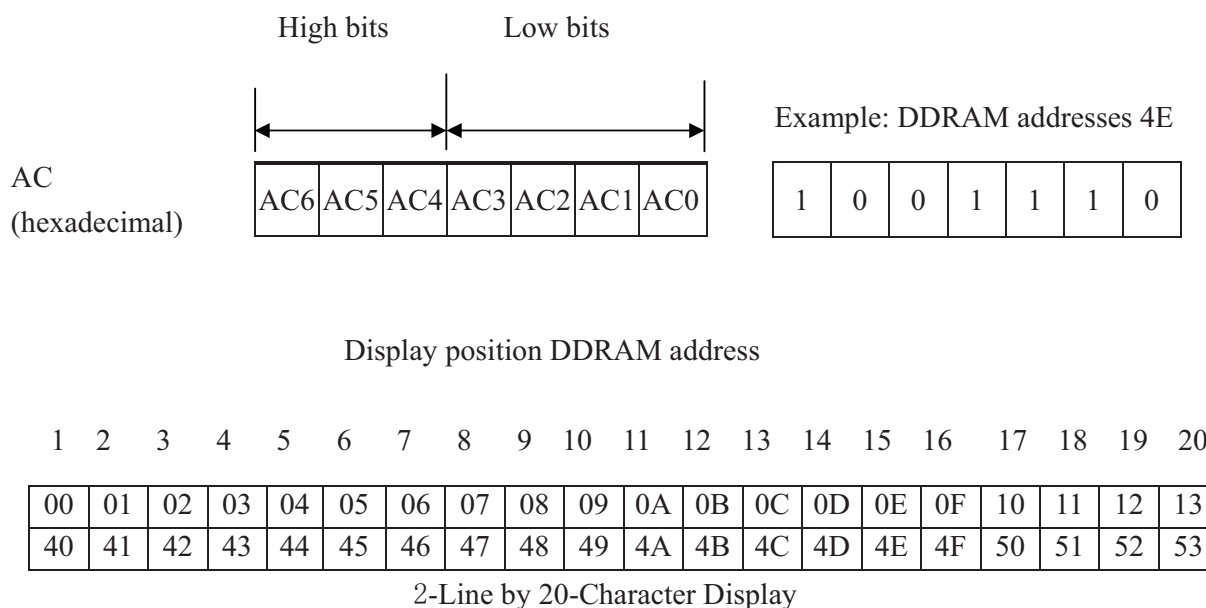
The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM.

Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.



Character Generator ROM (CGROM)

The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See Table 2.

Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns

can be written, and for 5×10 dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns

Table 1

For 5 * 8 dot character patterns

| Character Codes (DDRAM data) | | CGRAM Address | | Character Patterns (CGRAM data) | | | | |
|------------------------------|-------|---------------|-------|---------------------------------|--|-------------------------|-------|----------------|
| 7 6 5 4 3 2 1 0 | | 5 4 3 2 1 0 | | 7 6 5 4 3 2 1 0 | | | | |
| High Low | | High Low | | High Low | | | | |
| 0 0 0 0 * 0 0 0 | | 0 0 0 | 0 0 0 | * * * | | Character pattern (1) | | |
| | | | 0 0 1 | * * * | | | 0 0 0 | Cursor pattern |
| | | | 0 1 0 | * * * | | | 0 0 0 | |
| | | | 0 1 1 | * * * | | | 0 0 0 | |
| | | | 1 0 0 | * * * | | | 0 0 0 | |
| | | | 1 0 1 | * * * | | | 0 0 0 | |
| | | | 1 1 0 | * * * | | | 0 0 0 | |
| | | | 1 1 1 | * * * | | | 0 0 0 | |
| | | | 0 0 0 | * * * | | | 0 0 0 | |
| | | | 0 0 1 | * * * | | | 0 0 0 | |
| 0 1 0 | * * * | 0 0 0 | | | | | | |
| 0 1 1 | * * * | 0 0 0 | | | | | | |
| 1 0 0 | * * * | 0 0 0 | | | | | | |
| 1 0 1 | * * * | 0 0 0 | | | | | | |
| 1 1 0 | * * * | 0 0 0 | | | | | | |
| 1 1 1 | * * * | 0 0 0 | | | | | | |
| 0 0 0 | * * * | 0 0 0 | | | | | | |
| 0 0 1 | * * * | 0 0 0 | | | | | | |
| 0 0 0 0 * 1 1 1 | | 1 1 1 | 1 0 0 | * * * | | | | |
| | | | 1 0 1 | | | | | |
| | | | 1 1 0 | | | | | |
| | | | 1 1 1 | | | | | |

For 5 * 10 dot character patterns

| Character Codes (DDRAM data) | | CGRAM Address | | Character Patterns (CGRAM data) | | | | |
|------------------------------|-------|---------------|---------|---------------------------------|-----------|-------------------|---------|----------------|
| 7 6 5 4 3 2 1 0 | | 5 4 3 2 1 0 | | 7 6 5 4 3 2 1 0 | | | | |
| High Low | | High Low | | High Low | | | | |
| 0 0 0 0 * 0 0 0 | | 0 0 | 0 0 0 0 | * * * | | Character pattern | | |
| | | | 0 0 0 1 | * * * | | | 0 0 0 0 | Cursor pattern |
| | | | 0 0 1 0 | * * * | | | 0 0 0 0 | |
| | | | 0 0 1 1 | * * * | | | 0 0 0 0 | |
| | | | 0 1 0 0 | * * * | | | 0 0 0 0 | |
| | | | 0 1 0 1 | * * * | | | 0 0 0 0 | |
| | | | 0 1 1 0 | * * * | | | 0 0 0 0 | |
| | | | 0 1 1 1 | * * * | | | 0 0 0 0 | |
| | | | 1 0 0 0 | * * * | | | 0 0 0 0 | |
| | | | 1 0 0 1 | * * * | | | 0 0 0 0 | |
| 1 0 1 0 | * * * | 0 0 0 0 | | | | | | |
| | | | 1 1 1 1 | * * * | * * * * * | | | |

■ : " High "

11. Character Generator ROM Pattern

| b7=4 b3=0 | | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|--------------|-------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | CG RAM [00] | | | 0 | a | P | ^ | P | | | | | 一 | 9 | 3 | 0 | P |
| 0001 | CG RAM [01] | | ! | 1 | A | Q | a | 9 | | | . | 7 | 7 | 4 | a | 9 | |
| 0010 | CG RAM [02] | | " | 2 | B | R | b | r | | | 7 | 7 | 7 | 7 | 7 | P | P |
| 0011 | CG RAM [03] | | # | 3 | C | S | c | s | | | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| 0100 | CG RAM [04] | | \$ | 4 | D | T | d | t | | | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| 0101 | CG RAM [05] | | % | 5 | E | U | e | u | | | = | 7 | 7 | 7 | 7 | 7 | 7 |
| 0110 | CG RAM [06] | | & | 6 | F | V | f | v | | | 9 | 9 | 9 | 9 | 9 | 9 | 9 |
| 0111 | CG RAM [07] | | ' | 7 | G | W | g | w | | | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| 1000 | CG RAM [00] | | (| 8 | H | X | h | x | | | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| 1001 | CG RAM [01] | |) | 9 | I | Y | i | y | | | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| 1010 | CG RAM [02] | | * | | J | Z | j | z | | | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| 1011 | CG RAM [03] | | + | | K | | k | | | | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| 1100 | CG RAM [04] | | , | < | L | | l | | | | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| 1101 | CG RAM [05] | | - | = | M | | m | | | | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| 1110 | CG RAM [06] | | . | > | N | | n | | | | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| 1111 | CG RAM [07] | | / | ? | O | | o | | | | 7 | 7 | 7 | 7 | 7 | 7 | 7 |

12. Instruction Table

| Instruction | Instruction Code | | | | | | | | | | Description | Execution time (fosc=210Khz) |
|-------------------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|---------------------------------|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM and set DDRAM address to "00H" from AC | 1.98ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | — | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.98ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | SH | Assign cursor moving direction and enable the shift of entire display. | 48μs |
| Display ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Set display (D), cursor (C), and blinking of cursor (B) on/off control bit. | 48μs |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | — | — | Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data. | 48μs |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | F | — | — | Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5×11 dots/5×8 dots) | 48μs |
| Set CGRAM Address | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter. | 48μs |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter. | 48μs |
| Write Data to RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM/CGRAM). | 48μs |

* "—" : N/A

➤ SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.9.3

- Transmitter: the device, which sends the data to the bus
- Receiver: the device, which receives the data from the bus
- Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

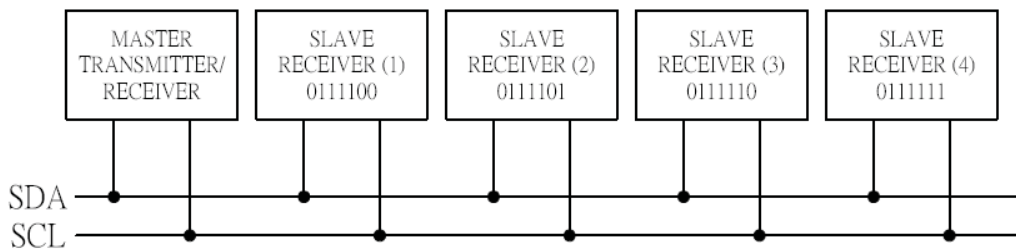
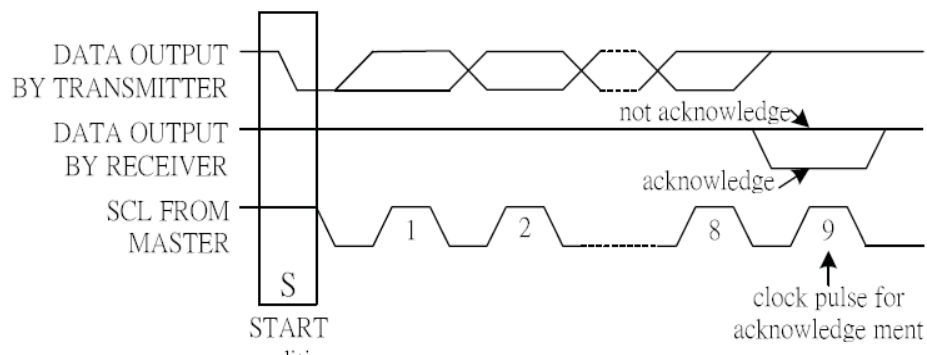


Fig .9.3 System configuration

➤ ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an Acknowledge after the reception of each byte. A master receiver must also generate an Acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the Acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an Acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I2C Interface is illustrated in Fig.9.4



Slave Address Option:

J8,J10 short,J7,J9open, SA1=0,SA0=0(default setting);

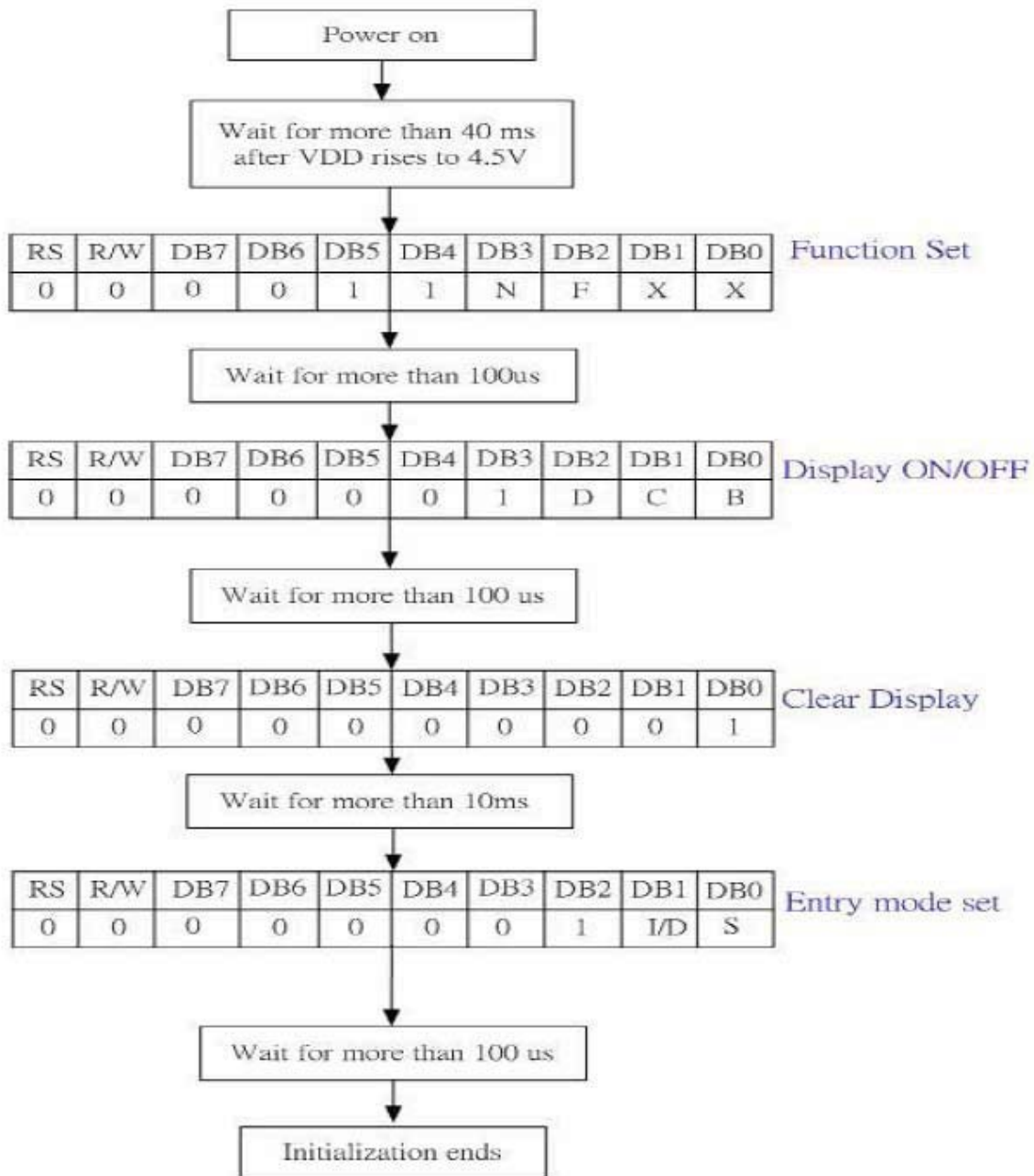
J8,J9 short,J7,J10open, SA1=0,SA0=1;

J7,J10 short,J8,J9open, SA1=1,SA0=0;

J7,J9 short,J8,J10open, SA1=1,SA0=1;

DB5(CSB)is connected to Vss by short J6.

14. Initializing of LCM



Initial Code:

```
void WriteData(BYTE byData)
```

```
{  
    I2C_Start();  
    I2C_Send(0x78);  
    I2C_Ack();  
    I2C_Send(0x40);  
    I2C_Ack();  
    I2C_Send(byData);  
    I2C_Ack();  
    I2C_Stop();  
}
```

```
void WriteInst(BYTE byInst)
```

```
{  
    I2C_Start();  
    I2C_Send(0x78);  
    I2C_Ack();  
    I2C_Send(0x00);  
    I2C_Ack();  
    I2C_Send(byInst);  
    I2C_Ack();  
    I2C_Stop();  
}
```

```
void InitRW1063(void)
```

```
{  
    WriteInst (0x38); //DL=1: 8 bits; N=1: 2 line; F=0: 5 x 8dots  
    WriteInst (0x0c); // D=1, display on; C=B=0; cursor off; blinking off;  
    WriteInst (0x06); // I/D=1: Increment by 1; S=0: No shift  
}
```

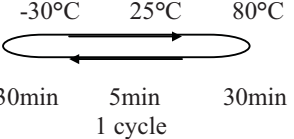
15. Quality Assurance

Screen Cosmetic Criteria

| Item | Defect | Judgment Criterion | Partition | | | | | | | | | | | | | | | | | | | | |
|--------------------|--------------------------------------|--|-------------------|--------------------------------------|--------------|-----------|--------------------|---|--------------------|---|-----------|---|-------------------|--------------------------------------|--------------|-----------|--------------------|---|--------------------|---|-----------|---|-------|
| 1 | Spots | <p>A)Clear</p> <table border="0"> <tr> <td><u>Size: d mm</u></td> <td><u>Acceptable Qty in active area</u></td> </tr> <tr> <td>$d \leq 0.1$</td> <td>Disregard</td> </tr> <tr> <td>$0.1 < d \leq 0.2$</td> <td>6</td> </tr> <tr> <td>$0.2 < d \leq 0.3$</td> <td>2</td> </tr> <tr> <td>$0.3 < d$</td> <td>0</td> </tr> </table> <p>Note: Including pin holes and defective dots which must be within one pixel size.</p> <p>B)Unclear</p> <table border="0"> <tr> <td><u>Size: d mm</u></td> <td><u>Acceptable Qty in active area</u></td> </tr> <tr> <td>$d \leq 0.2$</td> <td>Disregard</td> </tr> <tr> <td>$0.2 < d \leq 0.5$</td> <td>6</td> </tr> <tr> <td>$0.5 < d \leq 0.7$</td> <td>2</td> </tr> <tr> <td>$0.7 < d$</td> <td>0</td> </tr> </table> | <u>Size: d mm</u> | <u>Acceptable Qty in active area</u> | $d \leq 0.1$ | Disregard | $0.1 < d \leq 0.2$ | 6 | $0.2 < d \leq 0.3$ | 2 | $0.3 < d$ | 0 | <u>Size: d mm</u> | <u>Acceptable Qty in active area</u> | $d \leq 0.2$ | Disregard | $0.2 < d \leq 0.5$ | 6 | $0.5 < d \leq 0.7$ | 2 | $0.7 < d$ | 0 | Minor |
| <u>Size: d mm</u> | <u>Acceptable Qty in active area</u> | | | | | | | | | | | | | | | | | | | | | | |
| $d \leq 0.1$ | Disregard | | | | | | | | | | | | | | | | | | | | | | |
| $0.1 < d \leq 0.2$ | 6 | | | | | | | | | | | | | | | | | | | | | | |
| $0.2 < d \leq 0.3$ | 2 | | | | | | | | | | | | | | | | | | | | | | |
| $0.3 < d$ | 0 | | | | | | | | | | | | | | | | | | | | | | |
| <u>Size: d mm</u> | <u>Acceptable Qty in active area</u> | | | | | | | | | | | | | | | | | | | | | | |
| $d \leq 0.2$ | Disregard | | | | | | | | | | | | | | | | | | | | | | |
| $0.2 < d \leq 0.5$ | 6 | | | | | | | | | | | | | | | | | | | | | | |
| $0.5 < d \leq 0.7$ | 2 | | | | | | | | | | | | | | | | | | | | | | |
| $0.7 < d$ | 0 | | | | | | | | | | | | | | | | | | | | | | |
| 2 | Bubbles in Polarizer | <table border="0"> <tr> <td><u>Size: d mm</u></td> <td><u>Acceptable Qty in active area</u></td> </tr> <tr> <td>$d \leq 0.3$</td> <td>Disregard</td> </tr> <tr> <td>$0.3 < d \leq 1.0$</td> <td>3</td> </tr> <tr> <td>$1.0 < d \leq 1.5$</td> <td>1</td> </tr> <tr> <td>$1.5 < d$</td> <td>0</td> </tr> </table> | <u>Size: d mm</u> | <u>Acceptable Qty in active area</u> | $d \leq 0.3$ | Disregard | $0.3 < d \leq 1.0$ | 3 | $1.0 < d \leq 1.5$ | 1 | $1.5 < d$ | 0 | Minor | | | | | | | | | | |
| <u>Size: d mm</u> | <u>Acceptable Qty in active area</u> | | | | | | | | | | | | | | | | | | | | | | |
| $d \leq 0.3$ | Disregard | | | | | | | | | | | | | | | | | | | | | | |
| $0.3 < d \leq 1.0$ | 3 | | | | | | | | | | | | | | | | | | | | | | |
| $1.0 < d \leq 1.5$ | 1 | | | | | | | | | | | | | | | | | | | | | | |
| $1.5 < d$ | 0 | | | | | | | | | | | | | | | | | | | | | | |
| 3 | Scratch | In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable. | Minor | | | | | | | | | | | | | | | | | | | | |
| 4 | Allowable Density | Above defects should be separated more than 30mm each other. | Minor | | | | | | | | | | | | | | | | | | | | |
| 5 | Coloration | Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only. | Minor | | | | | | | | | | | | | | | | | | | | |

16. Reliability

Content of Reliability Test

| Environmental Test | | | |
|--------------------------------------|--|---|---------------------|
| Test Item | Content of Test | Test Condition | Applicable Standard |
| High Temperature storage | Endurance test applying the high storage temperature for a long time. | 80°C 96hrs | — |
| Low Temperature storage | Endurance test applying the high storage temperature for a long time. | -30°C 96hrs | — |
| High Temperature Operation | Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time. | 70°C 96hrs | — |
| Low Temperature Operation | Endurance test applying the electric stress under low temperature for a long time. | -20°C 96hrs | — |
| High Temperature/ Humidity Storage | Endurance test applying the high temperature and high humidity storage for a long time. | 80°C, 90%RH 96hrs | — |
| High Temperature/ Humidity Operation | Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time. | 70°C, 90%RH 96hrs | — |
| Temperature Cycle | Endurance test applying the low and high temperature cycle.  | -30°C → 80°C 10 cycles | — |
| Mechanical Test | | | |
| Vibration test | Endurance test applying the vibration during transportation and using. | 10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs | — |
| Shock test | Constructional and mechanical endurance test applying the shock during transportation. | 50G Half sign wave 11 msdc 3 times of each direction | — |

***Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25°C